ROHM Switching Regulator Solutions

Evaluation Board: Step-down Switching Regulator With Built-in Power MOSFET

BD9328EFJ / BD9329AEFJ (12V | 2A / 3A Output)

No.0000000014

●Introduction

This application note will provide the steps necessary to operate and evaluate ROHM's step-down switching regulator using the BD9328EFJ/BD9329AEFJ evaluation boards. Component selection, board layout recommendations, operation procedures and application data is provided.

●Description

This evaluation board has been developed for ROHM's step-down switching regulator customers evaluating BD9328EFJ and/or BD9329AEFJ. While accepting a wide power supply of 4.2-18V, a step down output of 3.3V or any external resistor defined voltage can be produced. The ICs have two integrated low resistance N-channel MOSFETs and a fixed synchronization frequency of 380 kHz. A Soft Start circuit prevents in-rush current during startup along with UVLO (low voltage error prevention circuit) and TSD (thermal shutdown detection) protection circuits. An EN pin allows for simple ON/OFF control of the IC to reduce standby current consumption.

●Applications

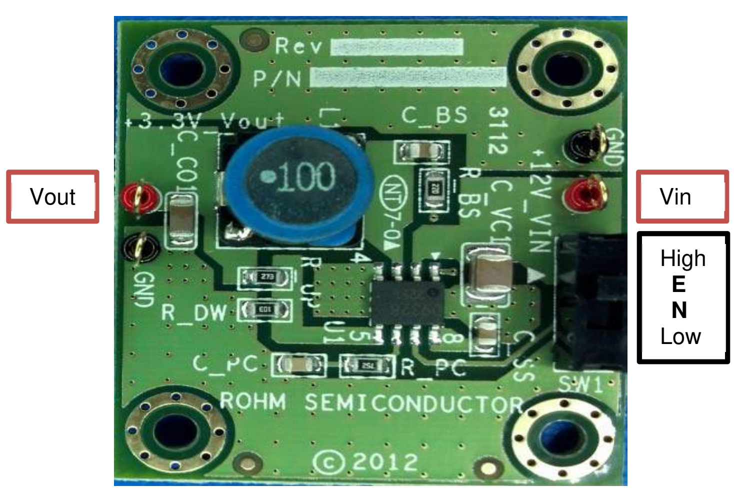
Distributed Power Systems
Pre-regulator for linear regulators

●Evaluation Board Operating Limits and Absolute Maximum Ratings

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Supply Voltage							
	BD9328EFJ	VCC	4.2	12	18	V	
	BD9329AEFJ	VCC	4.2	12	18	V	
Output Voltage / Current							
	BD9328EFJ	VOUT	-	3.3V	-	V	
	BD9329AEFJ	VOUT	-	3.3V	-	V	
	BD9328EFJ	IOUT	-	-	2	A	
	BD9329AEFJ	IOUT	-	-	3	A	

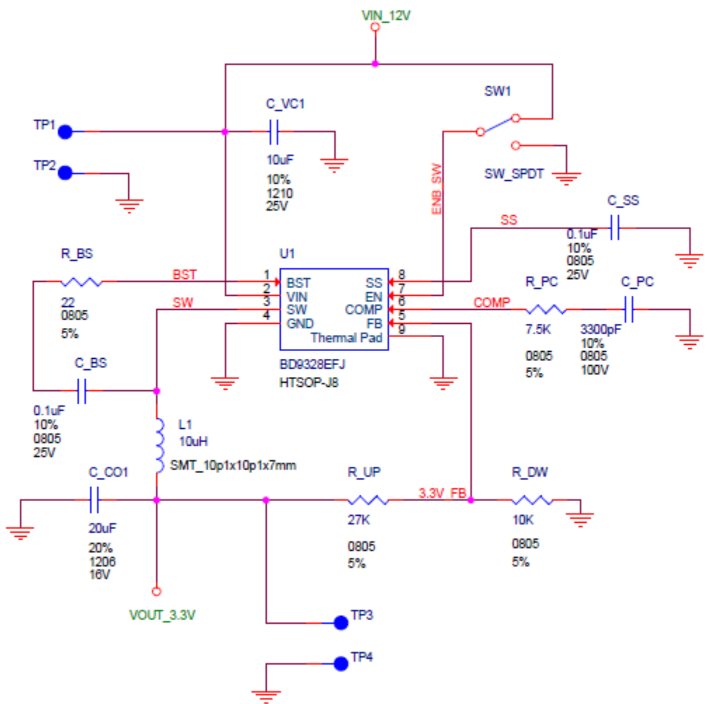
●Evaluation Board

Below is the evaluation board with the BD9328EFJ. BD9329AEFJ eval board uses the same components and board layout



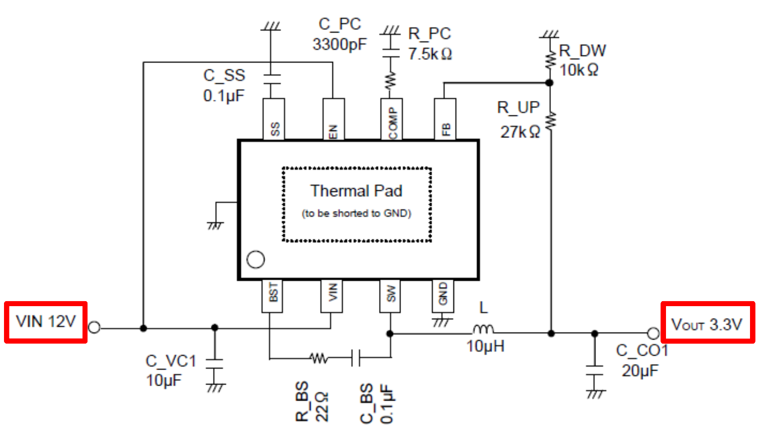
●Evaluation Board Schematic

Below is the evaluation board schematic for BD9328EFJ. BD9329AEFJ eval board uses the same schematic



●Evaluation Board I/O

Below is the reference application circuit that shows the inputs (Vin and EN) and the output (SW and FB)



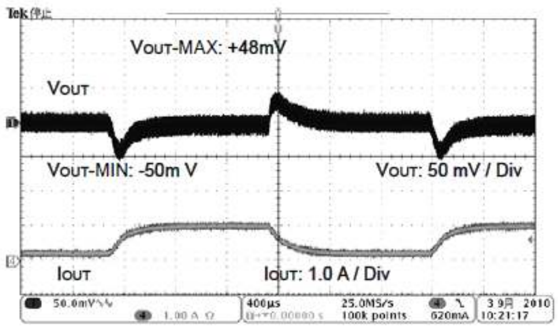
●Evaluation Board Operation Procedures

Below is the procedure to operate the evaluation board

1. Connect GND to a GND pin on the evaluation board
2. Connect Vin to the +12V_Vin pin. This will provide Vin to the Vin pin of the IC
    i. Note: EN pin is pulled high as when SW1 is high (white arrow)
3. Now output power can be measured from the +3.3V_Vout pin on the evaluation board with a load attached

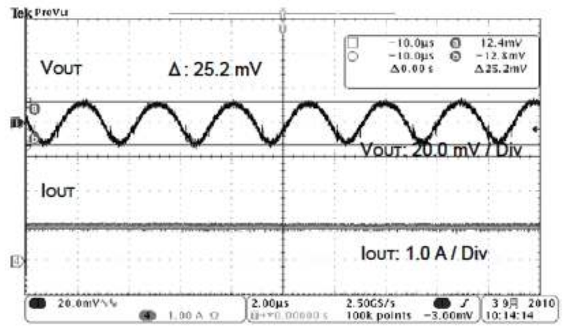
●Reference Graphs Application Data for BD9328EFJ

Below graphs shows load characteristics, transient responses and efficiency of the BD9328/9 eval board.



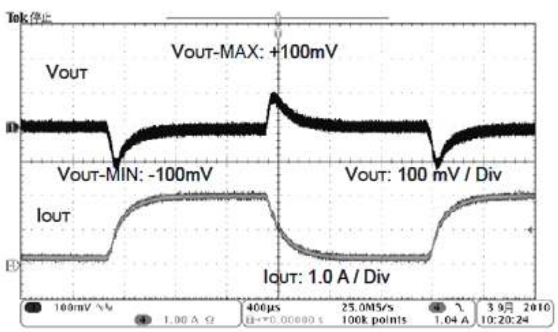
Transient Response

(VIN= 12V VOUT= 3.3V L= 10μH Cout =20μF Iout= 0.2-1.0A)



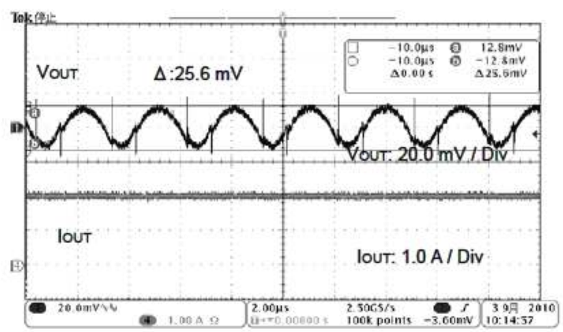
Output Ripple Voltage

(VIN= 12V VOUT= 3.3V L= 10μH Cout =20μF I out= 1.0A)



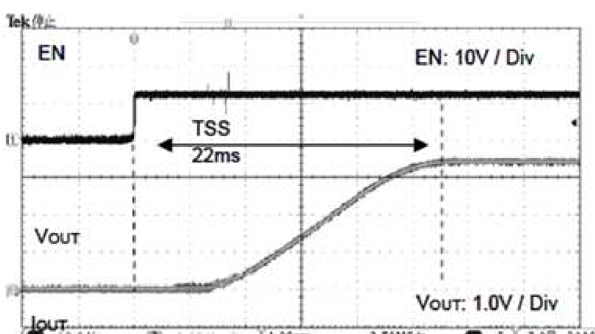
Transient Response

(VIN= 12V VOUT= 3.3V L= 10μH Cout =20μF Iout= 0.2-2.0A)



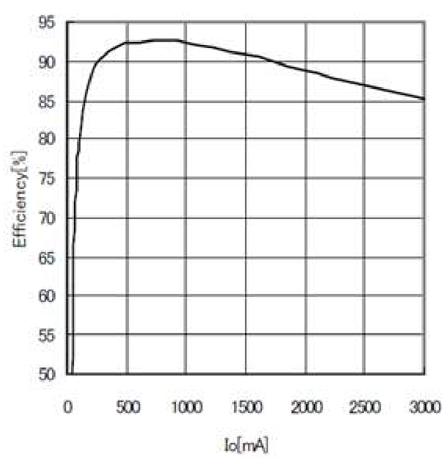
Output Ripple Voltage

(VIN= 12V VOUT= 3.3V L= 10μH Cout =20μF I out= 2.0A)



Start Up waveform

(VIN= 12V VOUT= 3.3V L= 10μH Css= 0.1μF)

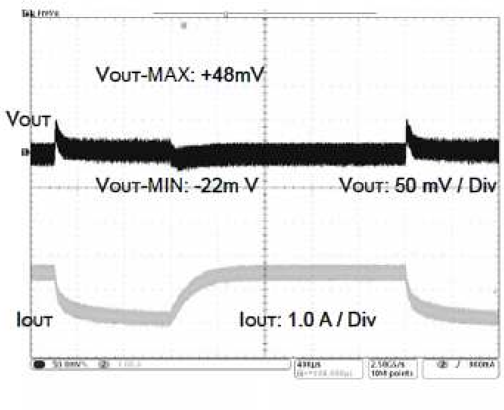


STEP Down Efficiency

(VIN= 12V VOUT= 3.3V L=10μH)

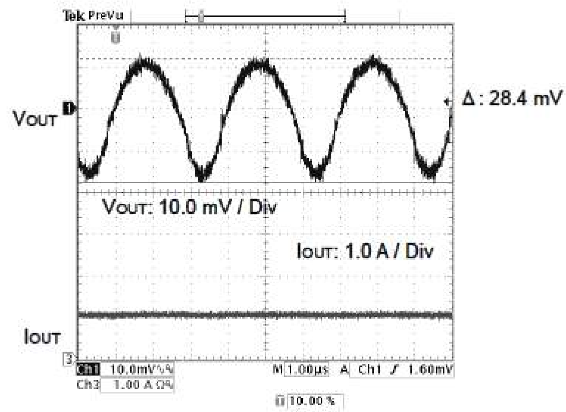
●Reference Graphs Application Data for BD9329AEFJ

Below graphs shows the load characteristics, transient responses and efficiency of the BD9329AEFJ eval board.



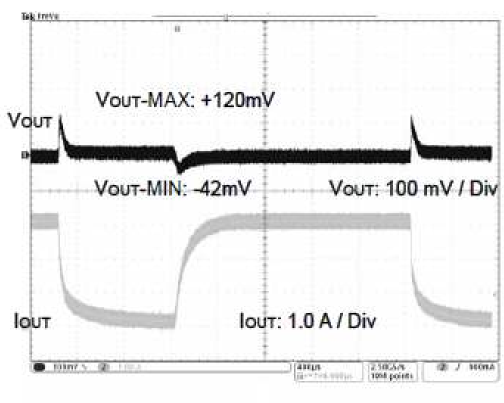
Transient Response

(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF Iout= 0.2-1.0A)



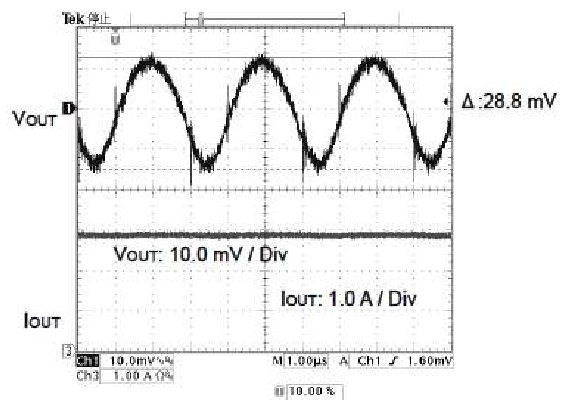
Output Ripple Voltage

(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF I out= 1.0A)



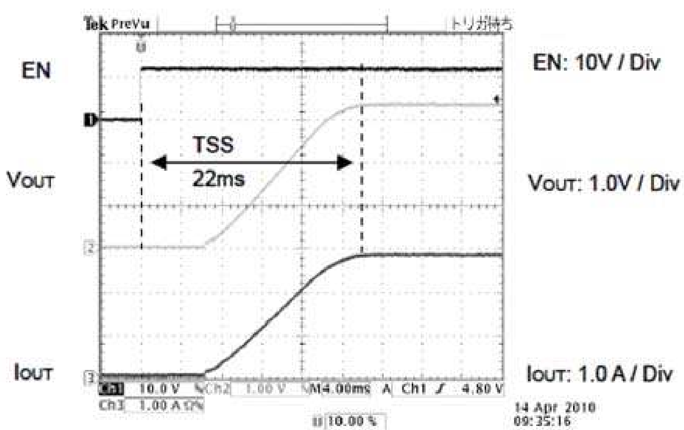
Transient Response

(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF Iout= 0.2-3.0A)



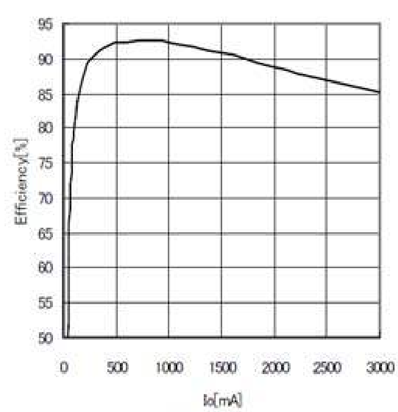
Output Ripple Voltage

(VIN= 12V VOUT= 3.3V L= 10μH Cout =22μF I out= 3 .0A)



Start Up waveform

(VIN= 12V VOUT= 3.3V L= 10μH CSS= 0.1μF)



STEP Down Efficiency

(VIN= 12V VOUT= 3.3V L=10μH)

●Evaluation Board Layout Guidelines

Below are the guidelines that have been followed and recommended for BD9328EFJ and BD9329AEFJ designs

Two high pulsing current flowing loops exist in the buck regulator system. The first loop, when FET is ON, starts from the input capacitors, to the VIN terminal, to the SW terminal, to the inductor, to the output capacitors, and then returns to the input capacitor through GND. The second loop, when FET is OFF, starts from the low FET, to the inductor, to the output capacitor, and then returns to the low FET through GND. To reduce the noise and improve the efficiency, please minimize these two loop area. Especially input capacitor, output capacitor and low FET should be connected to GND plain. PCB Layout may affect the thermal performance, noise and efficiency greatly. So please take extra care when designing PCB Layout patterns.

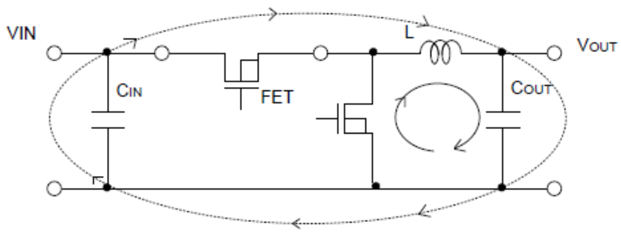


Fig.25 Current loop in Buck regulator system

- The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.
- The input capacitors should be connected as close as possible to the VIN terminal.
- Keep sensitive signal traces such as trace connected FB and COMP away from SW pin.
- The inductor and the output capacitors should be placed close to SW pin as much as possible.

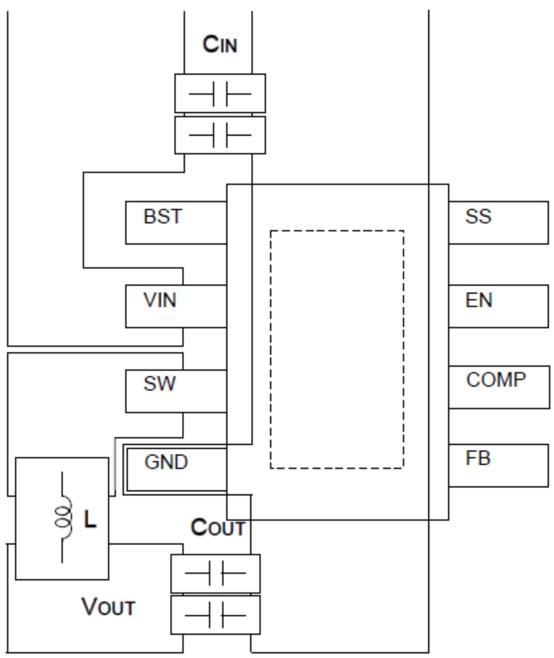


Fig.26 The example of PCB layout pattern

Note:

For applications operating at or near maximum voltage conditions (20V max.), additional precautions regarding heat dissipation need to be considered during board layout. The provided evaluation board is a 2-layer board meant for evaluation purposes only. At maximum conditions, the IC's internal thermal shutdown detection circuit will be potentially initiated and the output disabled until the junction temperature falls. For final designs operating near these conditions, we recommend using one of the below PCB options for better heat dissipation of the IC.

1) Use of a 4-layer PCB with internal GND planes connected to the IC GND pins
2) Use of a 2-layer PCB with a heat sink attached to the IC package
3) Use of a 2-layer PCB with a copper plane (>1oz) attached to the IC

●Selecting Application Components

(1) Output LC filter constant selection (Buck Converter)

The Output LC filter is required to supply constant current to the output load. A larger value inductance at this filter results in less inductor ripple current(ΔI_L) and less output ripple voltage. However, the larger value inductors tend to have less fast load transient-response, a larger physical size, a lower saturation current and higher series resistance. A smaller value inductance has almost opposite characteristics above. So Choosing the Inductor ripple current(ΔI_L) between 20 to 40% of the averaged inductor current (equivalent to the output load current) is a good compromise.

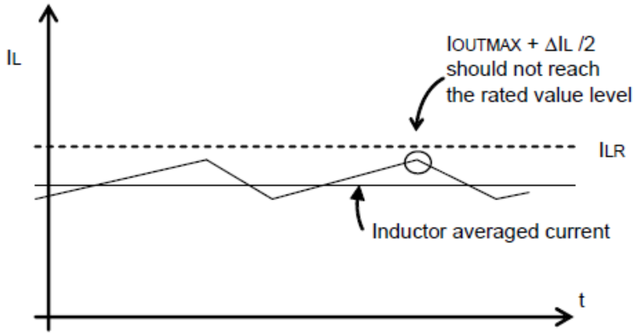


Fig.18

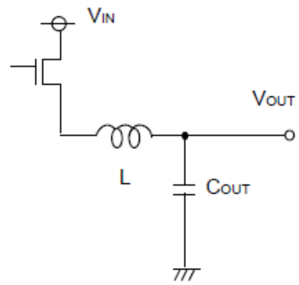


Fig.19

Setting ΔI_L = 30% x Averaged Inductor current (2A) = 0.6 [A]

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 10\mu\,[H]$$

Where V_{IN}= 12V, V_{OUT}= 3.3V, F_{OSC}= 380 kHz,
; F_{OSC} is a switching frequency

Also the inductor should have the higher saturation current than $I_{OUTMAX} + \Delta I_L / 2$.

The output capacitor C_{OUT} affects the output ripple-voltage. Choose the large capacitor to achieve the small ripple-voltage enough to meet the application requirement.

Output ripple voltage ΔV_{RPL} is calculated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}} \right) \quad [V]$$

Where R_{ESR} is a parasitic series resistance in output capacitor.

Setting C_{OUT} = 20μF, R_{ESR} = 10mΩ

ΔV_{RPL} = 0.6 x (10m + 1 / (8 x 20μ x 380k)) = 15.8mV

(2) Loop Compensation
Choosing compensation capacitor C_{CMP} and resistor R_{CMP}

The current-mode buck converter has 2-poles and 1-zero system. Choosing the compensation resistor and capacitor is important for a good load-transient response and good stability.
The example of DC/DC converter application bode plot is shown below.

The compensation resistor R_{CMP} will decides the cross over frequency F_{CRS} (the frequency that the total DC-DC loop-gain falls to 0dB).
Setting the higher cross over frequency achieves good response speed, however less stability. While setting the lower cross over frequency shows good stability but worse response speed.
The 1/10 of switching frequency for the cross over frequency shows a good performance at most applications.

(i) Choosing phase compensation resistor R_{CMP}
The compensation resistor R_{CMP} can be on following formula.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} \quad [\Omega]$$

Where
V_{OUT} ; Output voltage, **F_{CRS}** ; Cross over frequency, **C_{OUT}** ; Output Capacitor,
V_{FB} ; internal feedback voltage (**0.9V**(TYP)), **G_{MP}** ; Current Sense Gain (**7.8A/V**(TYP)) ,
G_{MA} ; Error Amplifier Trans-conductance (**300μA/V**(TYP))

Setting V_{OUT}= 3.3V, F_{CRS}= 38kHz, C_{OUT}= 20μF;

$$R_{CMP} = \frac{2\pi \times 3.3 \times 38k \times 20u}{0.9 \times 7.8 \times 300u} = 7.48k \simeq 7.5k \quad [\Omega]$$

(ii) Choosing phase compensation capacitor CCMP
For the stability of DC/DC converter, canceling the phase delay that derives from output capacitor C_{OUT} and resistive load R_{OUT} by inserting the phase advance.
The phase advance can be added by the zero on compensation resistor R_{CMP} and capacitor C_{CMP}.
Making Fz= F_{CRS} / 6 gives a first-order estimate of C_{CMP}.

$$\text{Compensation Capacitor} \quad C_{CMP} = \frac{1}{2\pi \times R_{CMP} \times Fz} \quad [F]$$

Setting Fz= F_{CRS}/6 = 6.3kHz;

$$\text{Compensation Capacitor} \quad C_{CMP} = \frac{1}{2\pi \times 7.5k \times 6.3k} = 3.54n \simeq 3.3n \quad [F]$$

(iii) The condition of the loop compensation stability
The stability of DC/DC converter is important. To secure the operating stability, please check the loop compensation has the enough phase-margin. For the condition of loop compensation stability, the phase-delay must be less than 150 degree where Gain is 0 dB.
Feed forward capacitor C_{RUP} boosts phase margin over a limited frequency range and is sometimes used to improve loop response. C_{RUP} will be more effective if R_{UP} >> R_{UP}||R_{DW}

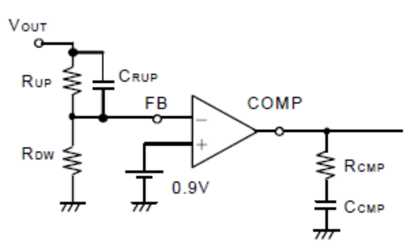


Fig.20

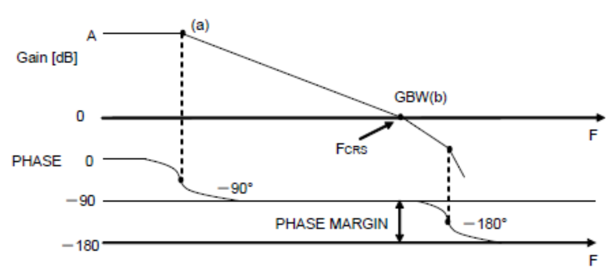


Fig.21

(3) Design of Feedback Resistance constant

Set the feedback resistance as shown below.

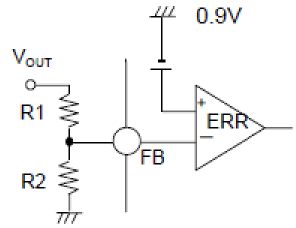


Fig.22

$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.9 \quad [V]$$

● **Evaluation Board BOM**

Below is a table with the build of materials. Part numbers and supplier references are provided.

Item	Qty	Ref	Description	Manufacturer	Part Number	Digikey P/N
1	1	C_CO1	CAP CER 22UF 16V 20% 1206	TDK Corporation	C3216X6S1C226M	445-8044-6-ND
2	1	C_PC	CAP CER 3300PF 100V 10% X7R 0805	TDK Corporation	C2012X7R2A332K	445-4431-2-ND
3	1	C_VC1	CAP CER 10UF 25V 10% 1210	TDK Corporation	C3225JB1E106K	445-3946-6-ND
4	1	L1	INDUCTOR SHIELD PWR 10UH SMD	TDK Corporation	C3225Y5V1H106Z	445-6478-6-ND
5	2	Css, Cbs	CAP CER 0.1UF 25V 10% X7R 0805	TDK Corporation	C2012X7R1E104K/1.25	445-1351-2-ND
6	1	RBS	RES 22 OHM 1/8W 5% 0805 SMD	ROHM Semiconductor	MCR10EZHJ220	RHM22ATR-ND
7	1	RDW	RES 10K OHM 1/8W 5% 0805 SMD	ROHM Semiconductor	MCR10ERTJ103	RHM10KCLTR-ND
8	1	RPC	RES 7.5K OHM 1/8W 5% 0805 SMD	ROHM Semiconductor	MCR10EZPJ752	RHM7.5KARTR-ND
9	1	RUP	RES 27K OHM 1/8W 5% 0805 SMD	ROHM Semiconductor	MCR10EZHJ273	RHM27KATR-ND
10	1	U1	IC REG BUCK SYNC ADJ 2A 8HTSOP	ROHM Semiconductor	**BD9328EFJ-E2**	BD9328EFJ-E2TR-ND
11	1	U1	IC REG BUCK SYNC ADJ 3A 8HTSOP	ROHM Semiconductor	**BD9329AEFJ-E2**	BD9329AEFJ-E2TR-ND

※ Note: In this example, the nominal resistance values of R1 and R2 were selected to set a 3.3 V output.

Notes

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/