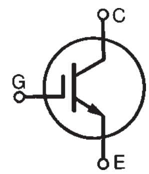
HiPerFAST™ IGBT ISOPLUS247™

IXGR 120N60B

(Electrically Isolated Back Surface)

V_{CES} = 600 V
I_{C25} = 156 A
$V_{CE(sat)}$ = 2.1 V



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	600	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	156	A
I_{C110}	T_C = 110°C	102	A
$I_{L(RMS)}$	External lead limit	76	A
I_{CM}	T_C = 25°C, 1 ms	300	A
SSOA (RBSOA)	V_{GE} = 15 V, T_{VJ} = 125°C, R_G = 2.4 Ω Clamped inductive load	I_{CM} = 200 @ 0.8 V_{CES}	A
P_C	T_C = 25°C	520	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C
V_{ISOL}	50/60 Hz, RMS, t = 1minute leads-to-tab	2500	V
Weight		5	g

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{CES}	I_C = 1 mA, V_{GE} = 0 V	600			V
$V_{GE(th)}$	I_C = 1 mA, V_{CE} = V_{GE}	2.5		5.5	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0 V; T_J = 25°C			200	µA
	T_J = 150°C			2	mA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V			±400	nA
$V_{CE(sat)}$	I_C = 100A, V_{GE} = 15 V (see note 1)			2.1	V

ISOPLUS 247

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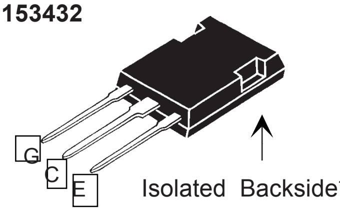


G = Gate, C = Collector
E = Emitter

* Patent pending

Features

- DCB Isolated mounting tab
- Meets TO-247AD package Outline
- High current handling capability
- Latest generation HDMOS™ process
- MOS Gate turn-on
  - drive simplicity

Applications

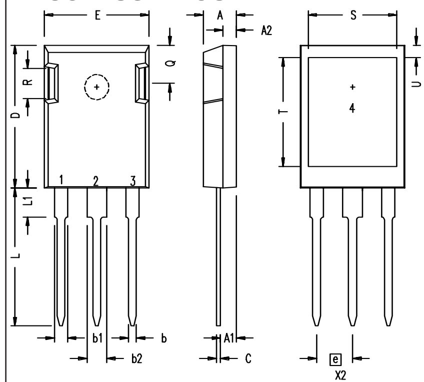
- Uninterruptible power supplies (UPS)
- Switched-mode and resonant-mode power supplies
- AC motor speed control
- DC servo and robot drives
- DC choppers

Advantages

- Easy assembly
- High power density
- Very fast switching speeds for high frequency applications

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	I_C = 60A; V_{CE} = 10 V, Pulse test, t ≤ 300 µs, duty cycle ≤ 2 %	50	75		S
C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		11000		pF
C_{oes}			680		pF
C_{res}			190		pF
Q_g	I_C = 100A, V_{GE} = 15 V, V_{CE} = 0.5 V_{CES}		350		nC
Q_{ge}			72		nC
Q_{gc}			131		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		60		ns
t_{ri}	I_C = 100A, V_{GE} = 15 V		45		ns
E_{on}	V_{CE} = 0.8 • V_{CES}, R_G = R_{off} = 2.4 Ω		2.4		mJ
$t_{d(off)}$	Remarks: Switching times may increase for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G		200	360	ns
t_{fi}			160	280	ns
E_{off}			5.5	9.6	mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**		60		ns
t_{ri}	I_C = 100A, V_{GE} = 15 V		60		ns
E_{on}	V_{CE} = 0.8 • V_{CES}, R_G = R_{off} = 2.4 Ω		4.8		mJ
$t_{d(off)}$	Remarks: Switching times may increase for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G		290		ns
t_{fi}			250		ns
E_{off}			8.7		mJ
R_{thJC}				0.3	K/W
R_{thCK}			0.15		K/W

ISOPLUS 247 OUTLINE



1 Gate, 2 Drain (Collector)
3 Source (Emitter)
4 no connection

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	.244
R	4.32	4.83	.170	.190

Fig. 1. Output Characteristics @ 25 ºC

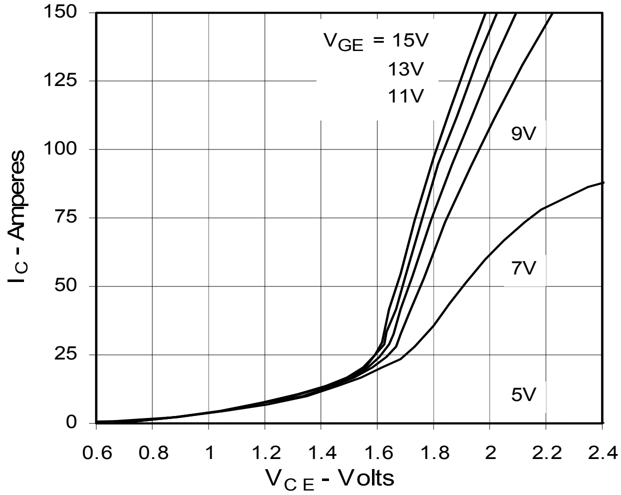


Fig. 2. Extended Output Characteristics @ 25 ºC

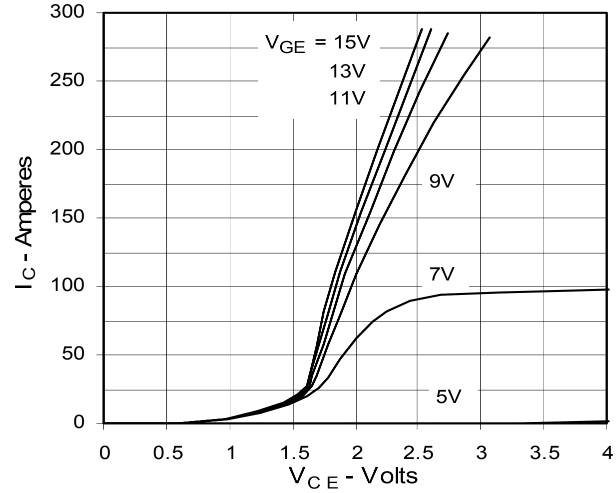


Fig. 3. Output Characteristics @ 125 ºC

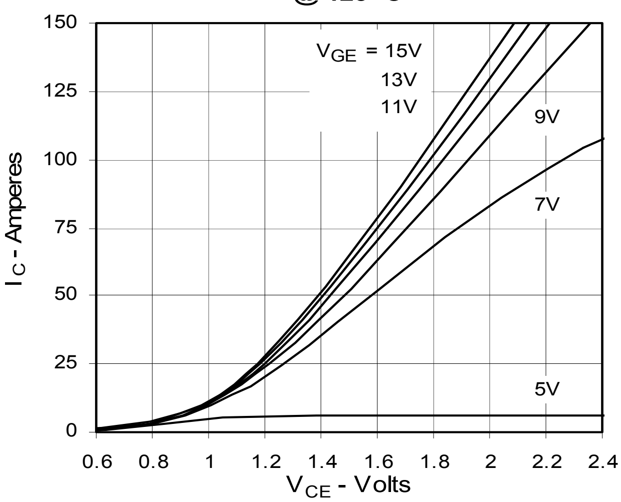


Fig. 4. Dependence of $V_{CE(sat)}$ on Temperature

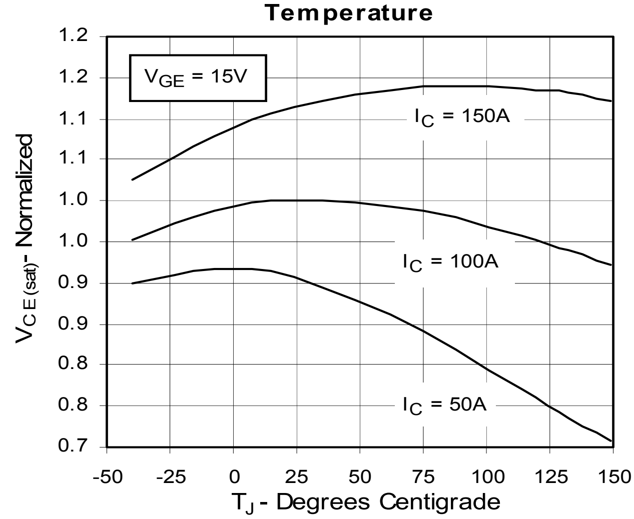


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter voltage

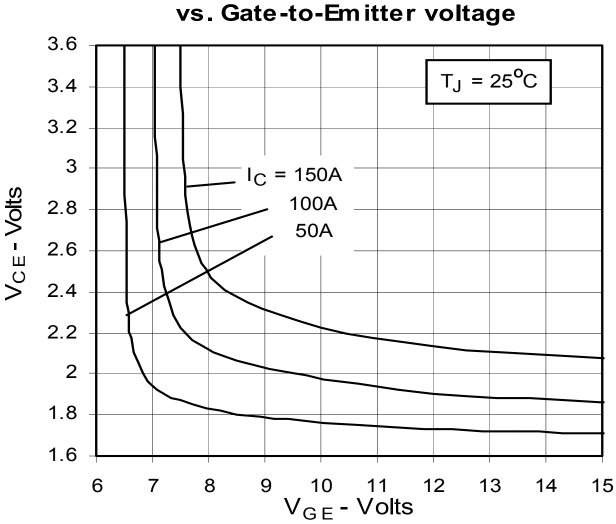


Fig. 6. Input Admittance

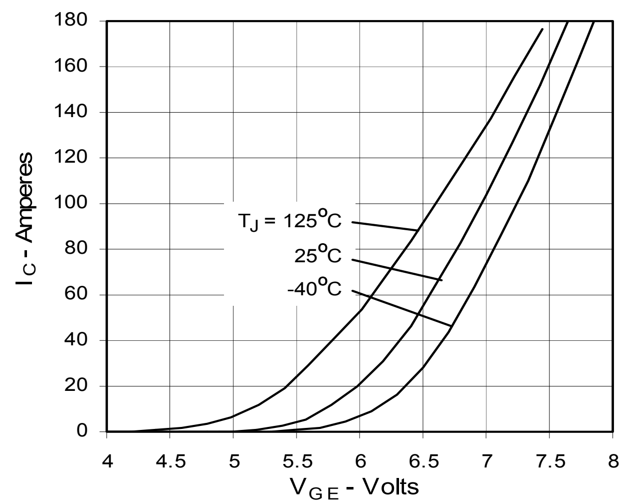


Fig. 7. Transconductance

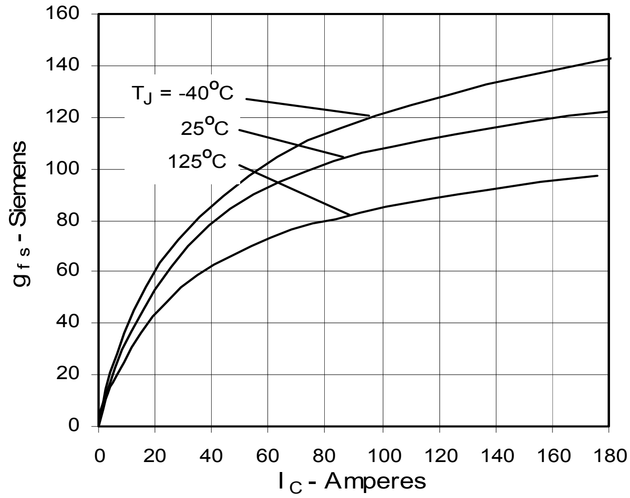


Fig. 8. Dependence of Turn-off Energy Loss on R_G

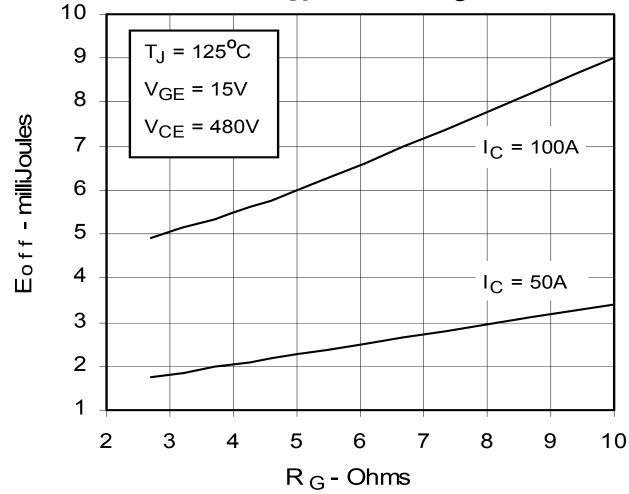


Fig. 9. Dependence of Turn-Off Energy Loss on I_C

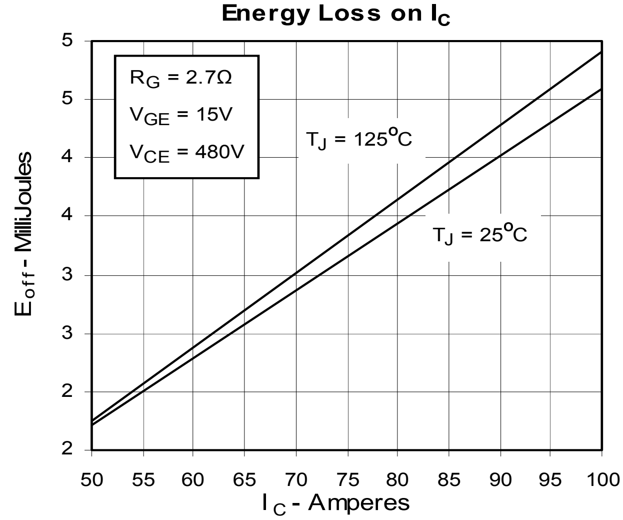


Fig. 10. Dependence of Turn-off Energy Loss on Temperature

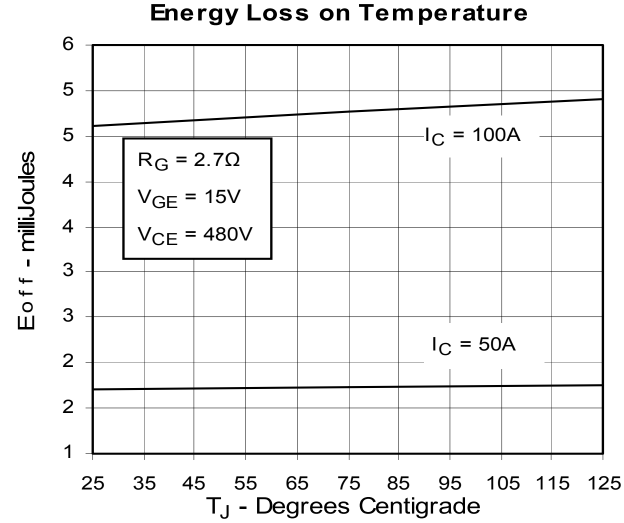


Fig. 11. Dependence of Turn-off Switching Time on R_G

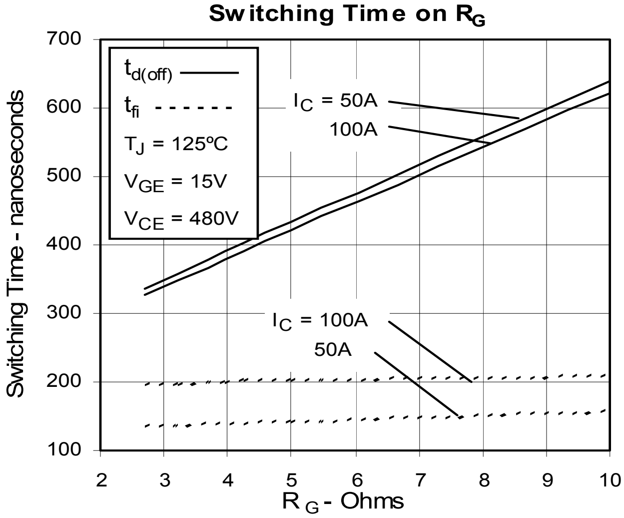


Fig. 12. Dependence of Turn-off Switching Time on I_C

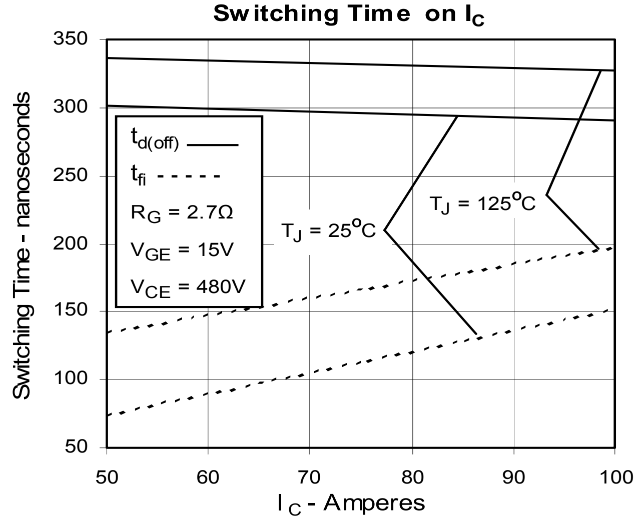


Fig. 13. Dependence of Turn-off Switching Time on Temperature

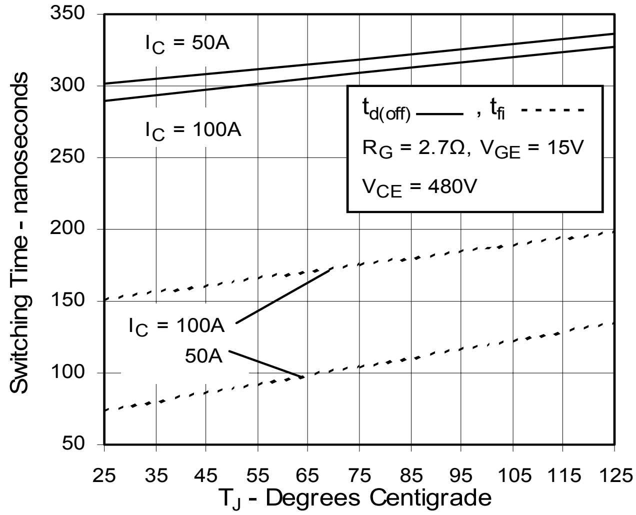


Fig. 14. Gate Charge

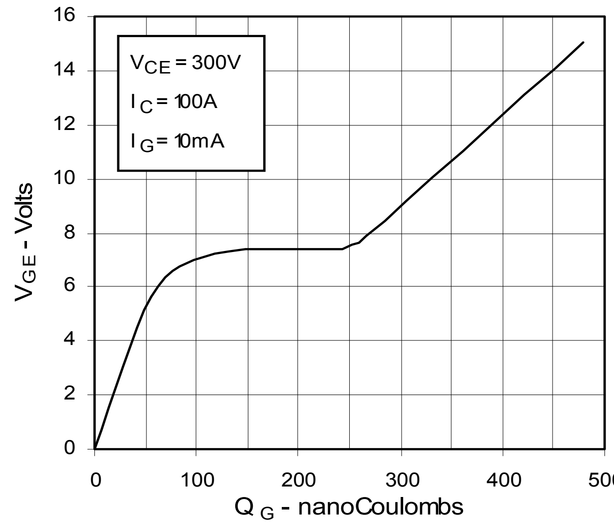


Fig. 15. Capacitance

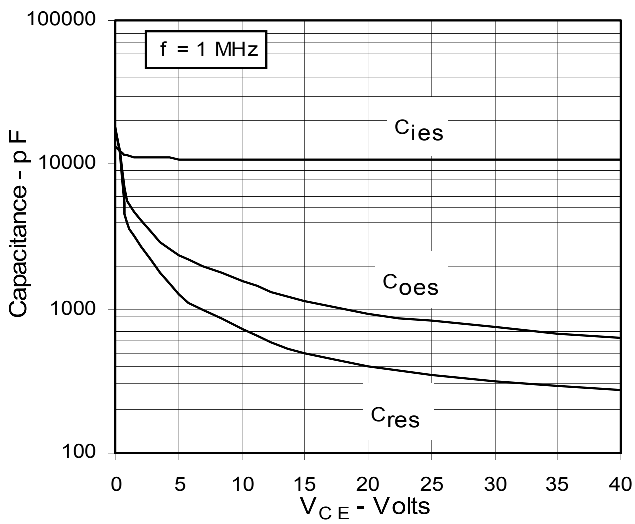


Fig. 16. Reverse-Bias Safe Operating Area

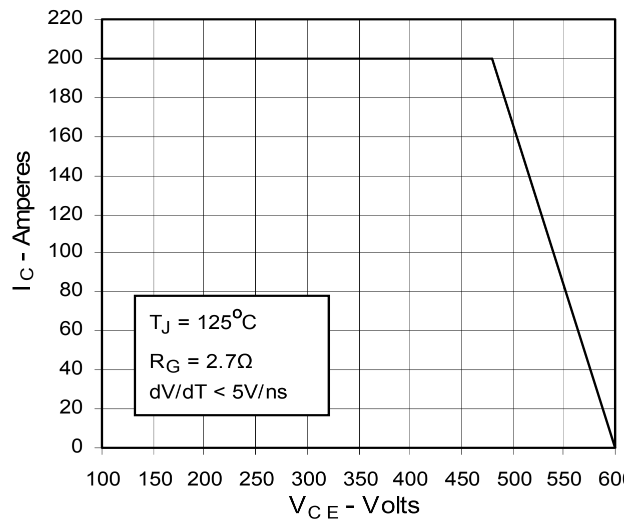


Fig. 17. Maximum Transient Thermal Resistance