VIPER26K

1050 V high voltage converter for ultra-wide input

Datasheet - production data

Features

- 1050 V avalanche-rugged power MOSFET
- allowing ultra-wide VAC input range to be covered
- Embedded HV startup and sense-FET
- Current mode PWM controller
- Drain current limit protection:
- -500 mA (VIPER265K)
- -700 mA (VIPER267K)
- Jittered switching frequency reduces the EMI filter cost: 60 kHz ± 4kHz
- Standby power < 30 mW at 230 VAC
- Embedded E/A with 3.3 V reference
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown
- Built-in soft-start for improved system reliability

Applications

- SMPS for energy metering
- Auxiliary power supplies for 3-phase input industrial systems
- LED lighting
- Air conditioning

Description

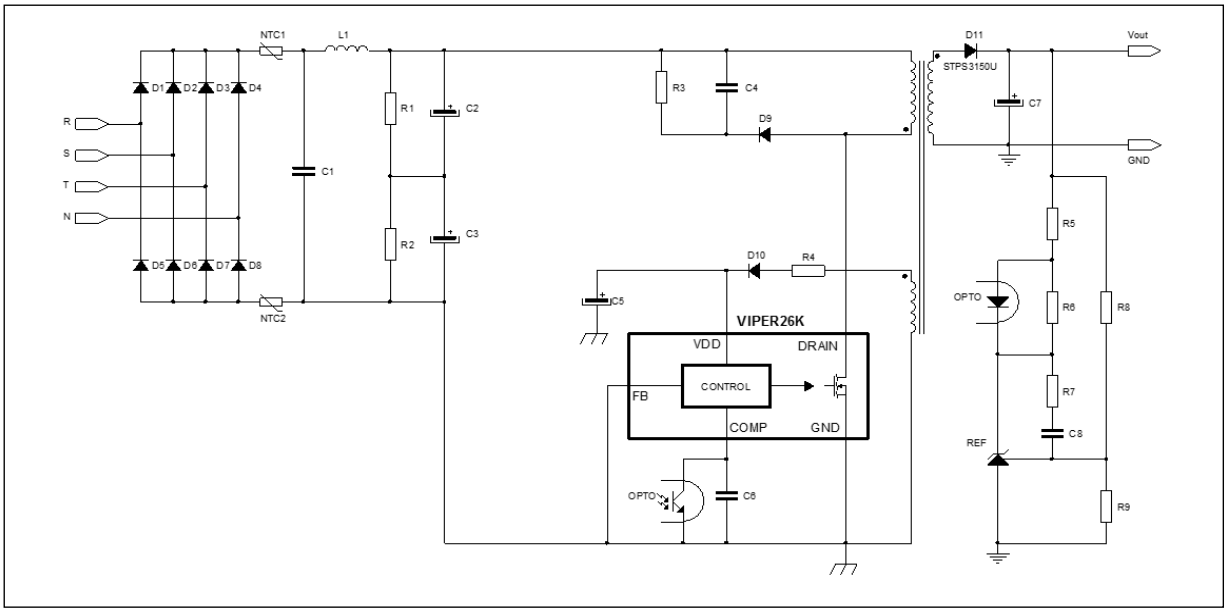
The device is a high voltage converter smartly integrating a 1050 V avalanche-rugged power section, with a PWM current mode control. The 1050 V-BV power MOSFET allows to extend input voltage range, and reduce the size of the DRAIN snubber circuit. This IC meets the most stringent energy-saving standards as it has very low consumption and operates in burst mode under light load.

The integrated HV startup, sense-FET, error amplifier and oscillator with jitter allow a complete application to be designed with the minimum number of components.

The VIPer26K supports the most common SMPS topologies such as: isolated flyback with optocoupler, primary-side regulation, non-isolated flyback with resistive feedback, buck, and buck boost.

This is information on a product in full production. www.st.com

Figure 1. Basic application schematic



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1 Pin setting

Figure 2. Connection diagram

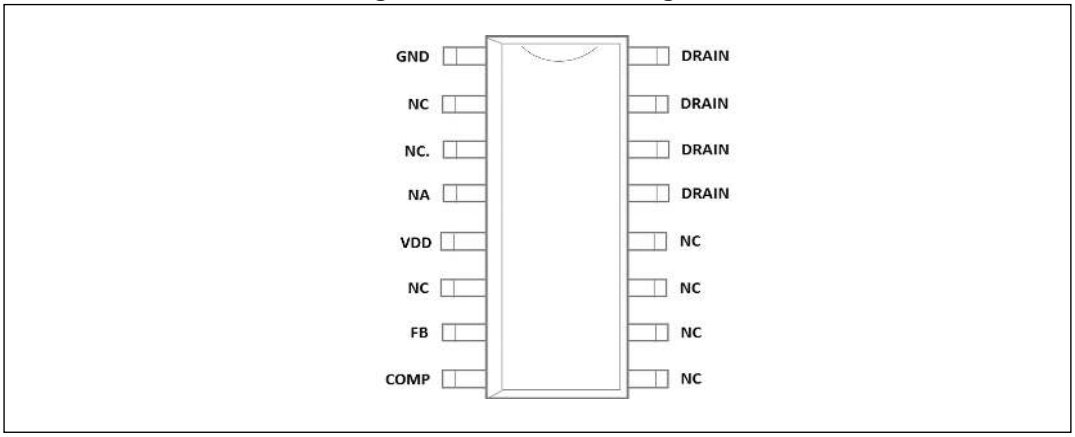


Table 1. Pin description

SO16 N	Name	Function
1	GND	**Ground.** Connected to the source of the internal power MOSFET and controller ground reference.
2, 3	N.C	**Not internally connected.** It can be connected to GND (pin 1) or left floating.
4	N.A.	**Not available for user.** This pin is mechanically connected to the controller die pad of the frame. It is highly recommended to connect it to GND (pin 1).
5	VDD	**Supply voltage of the control section.** This pin provides the charging current of the external capacitor.
6	N.C.	**Not available for user.** It is highly recommended to connect it to GND (pin 1).
7	FB	**Inverting input of the internal trans-conductance error amplifier.** Connecting the converter output to this pin through a single resistor results in an output voltage equal to the error amplifier reference voltage. An external resistors divider is required for higher output voltages.
8	COMP	**Output of the internal trans conductance error amplifier.** The compensation network has to be placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop. The pin is used also to directly control the PWM with an optocoupler. The linear voltage range extends from V_{COMPL} to V_{COMPH}.
9-12	N.C.	**Not internally connected.** It has to be left floating.
13-16	DRAIN	**High voltage drain pin.** The built-in high voltage switched start-up bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

2 Electrical and thermal ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter[1],[2]	Value		Unit
			Min.	Max.	
V_{DRAIN}	13-16	Drain-to-source (ground) voltage		1.05	KV
I_{DRAIN}		Pulse drain current (limited by T_J = 150 °C)		3	A
V_{DD}	5	Supply voltage	-0.3	Internally limited	V
I_{DD}	5	Input current		20	mA
V_{FB}	7	Feedback pin voltage	-0.3	4.8	V
V_{COMP}	8	Input pin voltage	-0.3	3.5	V
P_{TOT}		Power dissipation at T_A < 60 °C		1.05[3]	W
T_J		Operating junction temperature range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C

1. Stresses beyond those listed absolute maximum ratings may cause permanent damage to the device.
2. Exposure to absolute-maximum-rated conditions for extended periods may affect the device reliability.
3. When mounted on a standard single side FR4 board with 100 mm² (0.1552 inch) of Cu (35 µm thick).

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
R_{TH-JC}	Thermal resistance junction to case [1] (Dissipated power = 1 W)	10	°C/W
R_{TH-JC}	Thermal resistance junction to case [2] (Dissipated power = 1 W)	5	°C/W
R_{TH-JA}	Thermal resistance junction ambient [1] (Dissipated power = 1 W)	120	°C/W
R_{TH-JA}	Thermal resistance junction ambient [2] (Dissipated power = 1 W)	85	°C/W

1. When mounted on a standard, single side FR4 board with minimum copper area.
2. When mounted on a standard, single side FR4 board with 100 mm2 of Cu (35 µm thick).

Figure 3. R_{thJA}

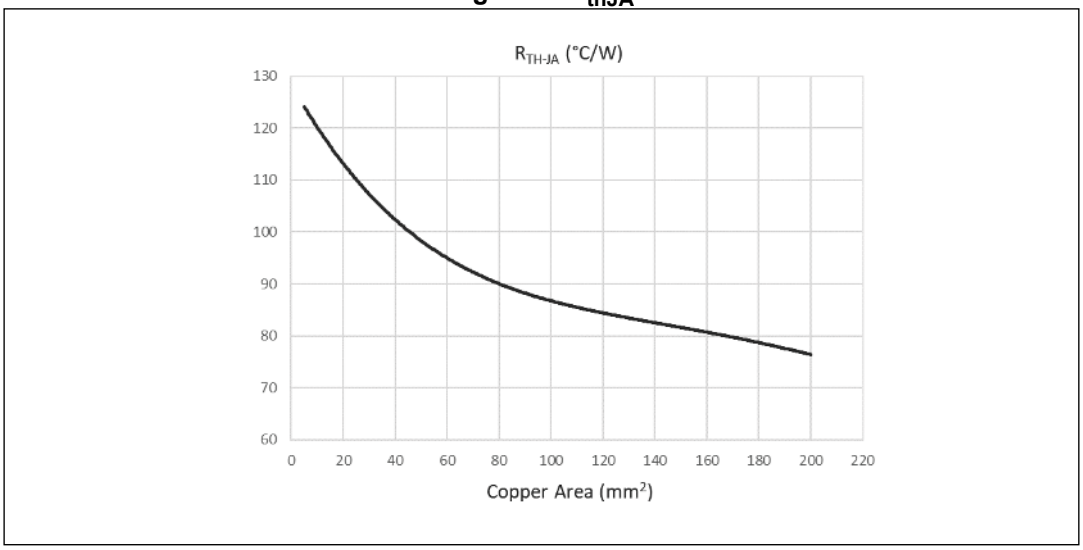


Table 4. Avalanche characteristics

Symbol	Pin	Parameter	Value		Unit
			Min.	Max.	
I_{AR}		Repetitive avalanche current (limited by T_J = 150 °C)		1	A
E_{AV}		Repetitive avalanche energy (limited by T_J = 150 °C)		3	mJ

3 Electrical characteristics

(T_J = -40 to 125°C, VDD = 14V; unless otherwise specified.)

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
V_{BVDSS}	Breakdown voltage	I_D = 1 mA, V_{COMP} = GND, T_J = 25°C	1.05			kV
I_{DSS}	Drain-source leakage current	V_{DRAIN} = 1050V, V_{COMP} = GND, T_J = 25°C			29	µA
$R_{DS(on)}$	Drain-Source ON state resistance	I_{DRAIN} = 0.2 A; T_J = 25 °C			7	Ω
		I_{DRAIN} = 0.2 A; T_J = 125 °C			14	

Table 6. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
High voltage start-up current source						
V_{VDSS_SU}	Startup breakdown drain-source voltage	I_D = 1 mA, V_{COMP} = GND, T_J = 25°C	1.05			kV
V_{HV_START}	Drain-source start voltage		38		60	V
I_{DDch1}	Charging current during startup	V_{DRAIN} = 50 V to 1.05 kV, V_{DD} = 4 V	-0.6		-1.8	mA
I_{DDch2}	Charging current in self-supply	V_{DRAIN} = 50 V to 1.05 kV, V_{DD} = 9 V falling edge	-7		-13	mA
IC supply and consumptions						
V_{DD}	Operating voltage range		11.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 15 mA	23.5			V
V_{DDon}	V_{DD} start up threshold		12	13	14	V

Table 6. Supply section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DDCSon}	V_{DDon} internal high voltage current generator threshold		9.5	10.5	11.5	V
V_{DDoff}	V_{DD} under voltage shutdown threshold		7	8	9	V
I_{DD0}	Operating supply current, not switching	F_{OSC} = 0 kHz, V_{COMP} = GND			0.6	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V, F_{OSC} = 60 kHz			2	mA
I_{DDoff}	Operating supply current with VDD < VDDoff	$V_{DD} < V_{DDoff}$			0.35	mA
I_{DDol}	Open loop failure current threshold	$V_{DD} = V_{DDclamp}$ V_{COMP} = 3.3 V	4			mA

Table 7. Controller section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E/A						
V_{REF_FB}	Input voltage		3.2	3.3	3.4	V
$I_{FB\_PULL\ UP}$	Pull-up current			-1		µA
G_M	Transconductance			2		mA/V
Compensation pin (Comp)						
V_{COMPH}	Upper saturation limit	T_J = 25°C		3		V
V_{COMPL}	Burst mode threshold	T_J = 25°C	1	1.1	1.2	V
V_{HYS}	Burst mode hysteresis			40		mV
H_{COMP}	ΔVCOMP/ΔIDRAIN	T_J = 25°C	1.9	2.35	2.8	V/A
$R_{COMP(DYN)}$	Dynamic resistance	V_{FB} = GND		15		kΩ
I_{COMP}	Source / sink Current	V_{FB} > 100mV		150		µA
	Max. source current	V_{COMP} = GND, V_{FB} = GND		220		µA

Table 7. Controller section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Current limitation						
I_{DLIM}	Drain current limitation	VIPER267K V_{COMP} = 3.3V, T_J = 25°C	0.66	0.7	0.74	A
		VIPER265K V_{COMP} = 3.3V, T_J = 25°C	0.47	0.5	0.53	
t_{SS}	Soft-start time			8.5		ms
T_{ON-MIN}	Minimum turn ON time				480	ns
$I_{DLIM-BM}$	Burst mode current limitation	V_{COMP} = V_{COMPL}		127		mA
Overload						
t_{OVL}	Overload time			50		ms
$t_{RESTART}$	Restart time after fault			1		s
Oscillator						
F_{OSC}	Switching frequency	T_J = -25 to 125°C	54	60	66	kHz
		T_J = -40 to 125°C	44	60	66	
F_D	Modulation depth			±4		kHz
F_M	Modulating frequency			240		Hz
D_{MAX}	Maximum duty cycle		70		80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature		150	160		°C
T_{HYST}	Thermal shutdown hysteresis			30		°C

3.1 Typical electrical characteristics

Figure 4. I_{DLIM} vs. T_j

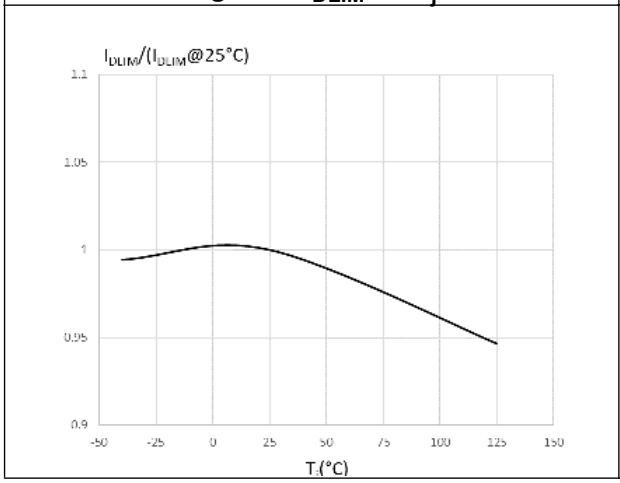


Figure 5. F_{OSC} vs. T_j

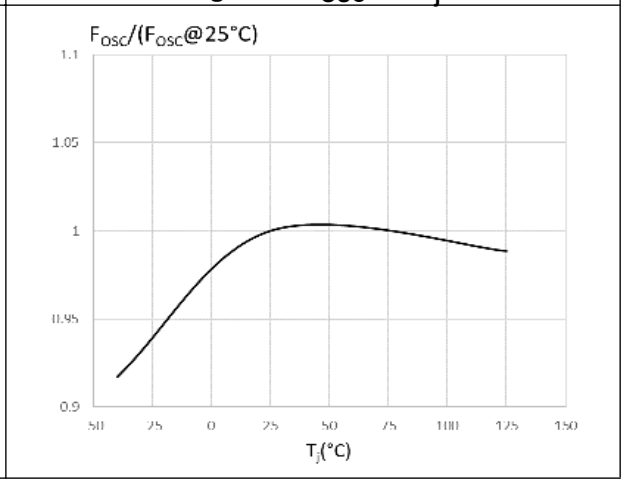


Figure 6. V_{HV_START} vs. T_j

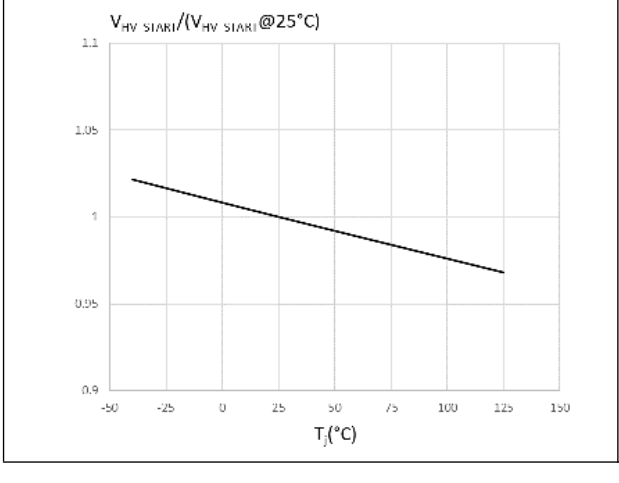


Figure 7. V_{REF_FB} vs. T_j

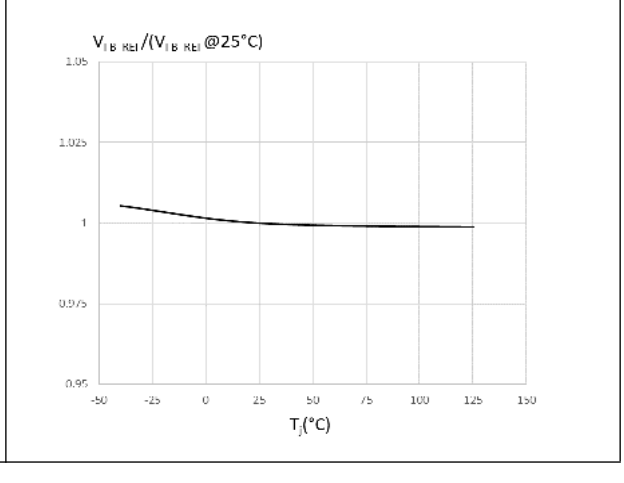


Figure 8. I_{DD0} vs. T_j

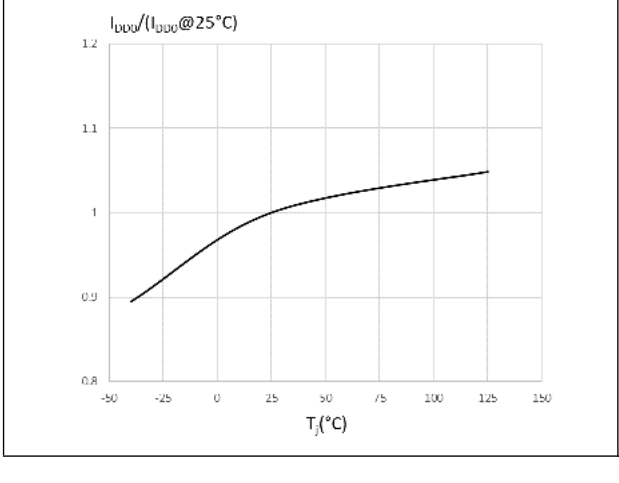


Figure 9. I_{DD1} vs. T_j

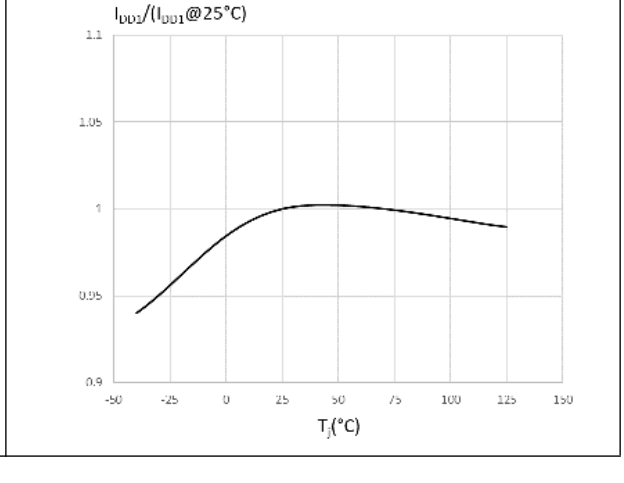


Figure 10. G_M vs. T_j

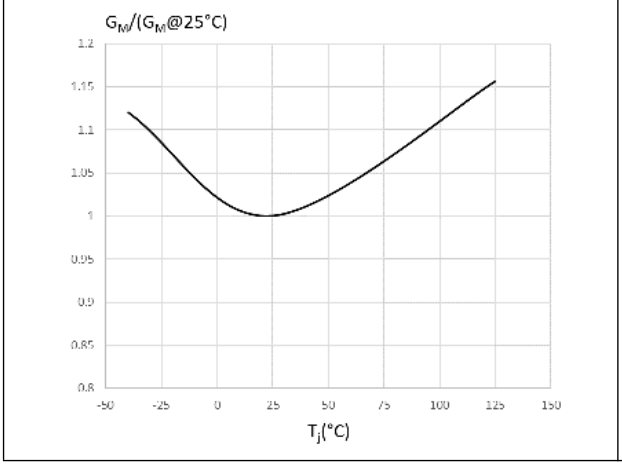


Figure 11. H_{COMP} vs. T_j

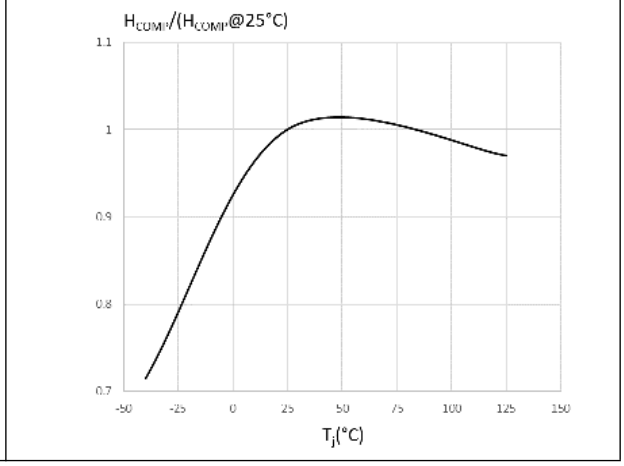


Figure 12. $I_{COMP(source/sink)}$ vs. T_j

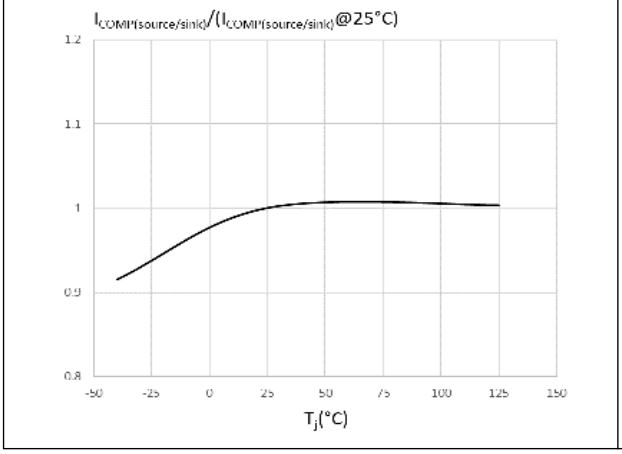


Figure 13. $I_{COMP(max\ source)}$ vs. T_j

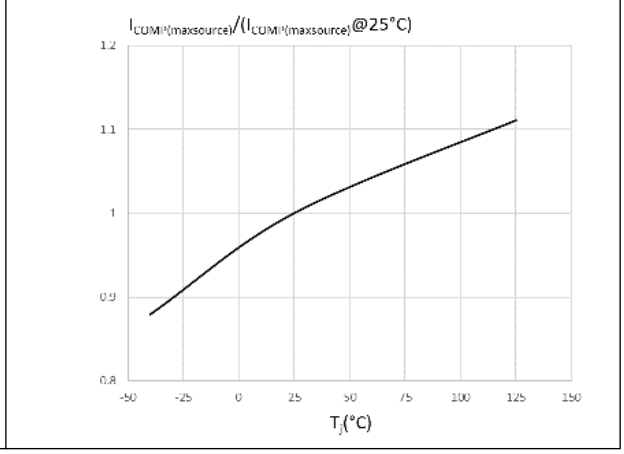


Figure 14. Power MOSFET capacitances variation vs. V_{DS} @ V_{GS}=0, f=1MHz

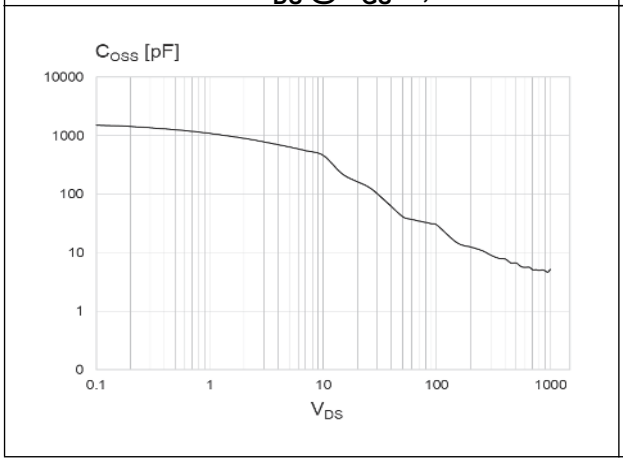


Figure 15. V_{BVDSS} vs. T_J

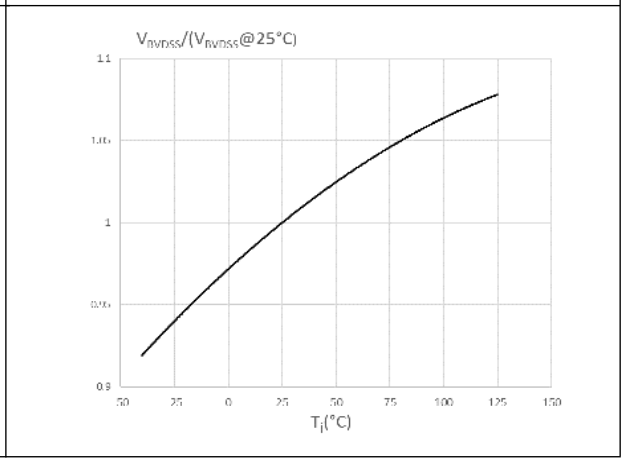


Figure 16. $R_{DS(on)}$ vs. T_j

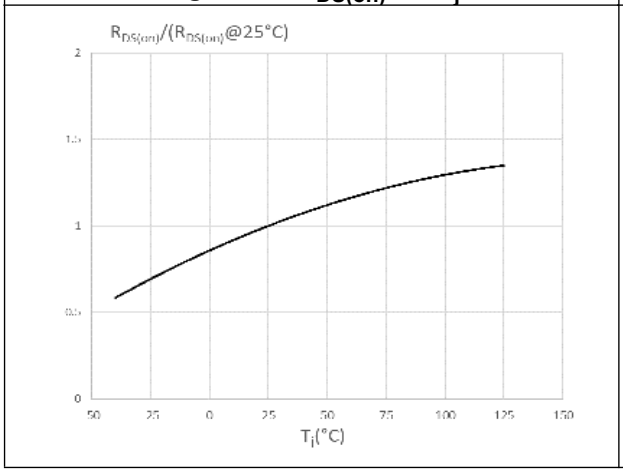


Figure 17. Maximum avalanche energy vs. T_j

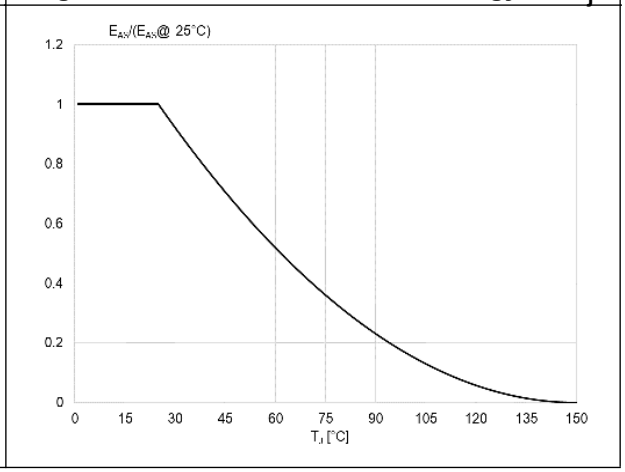
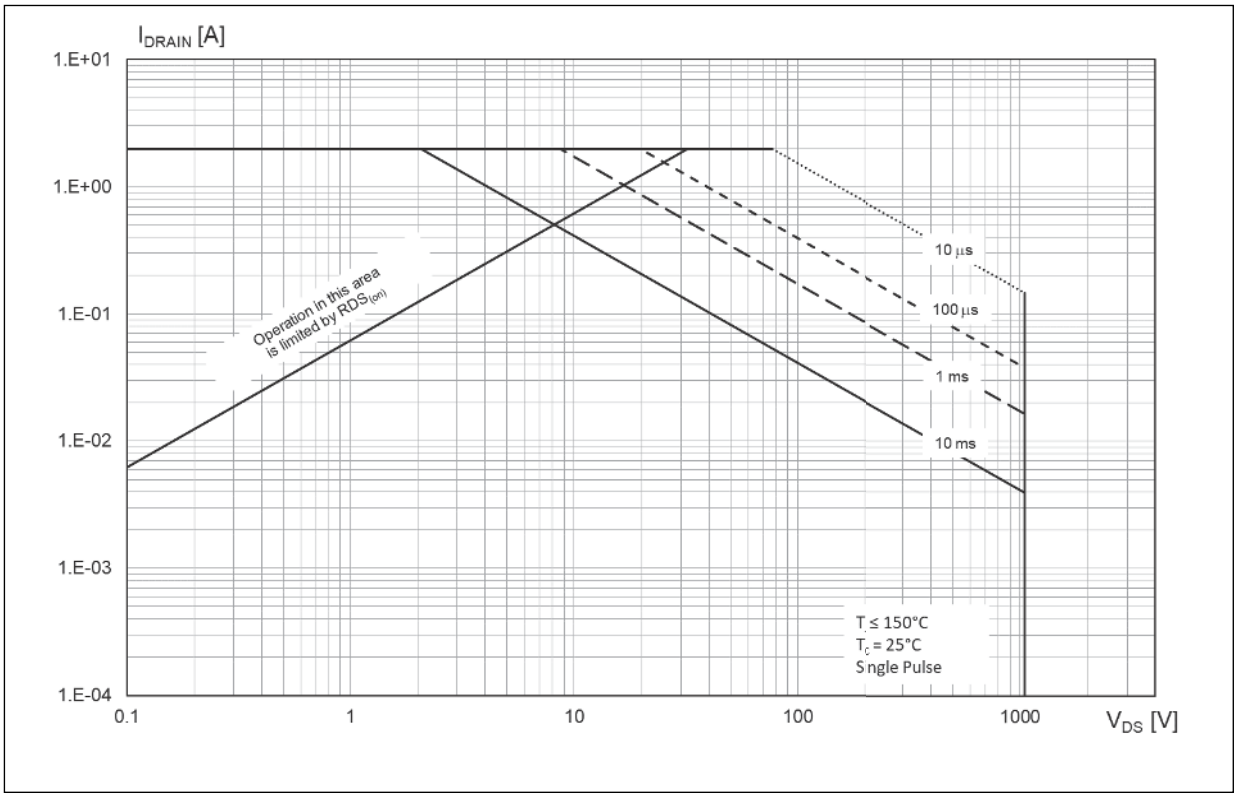


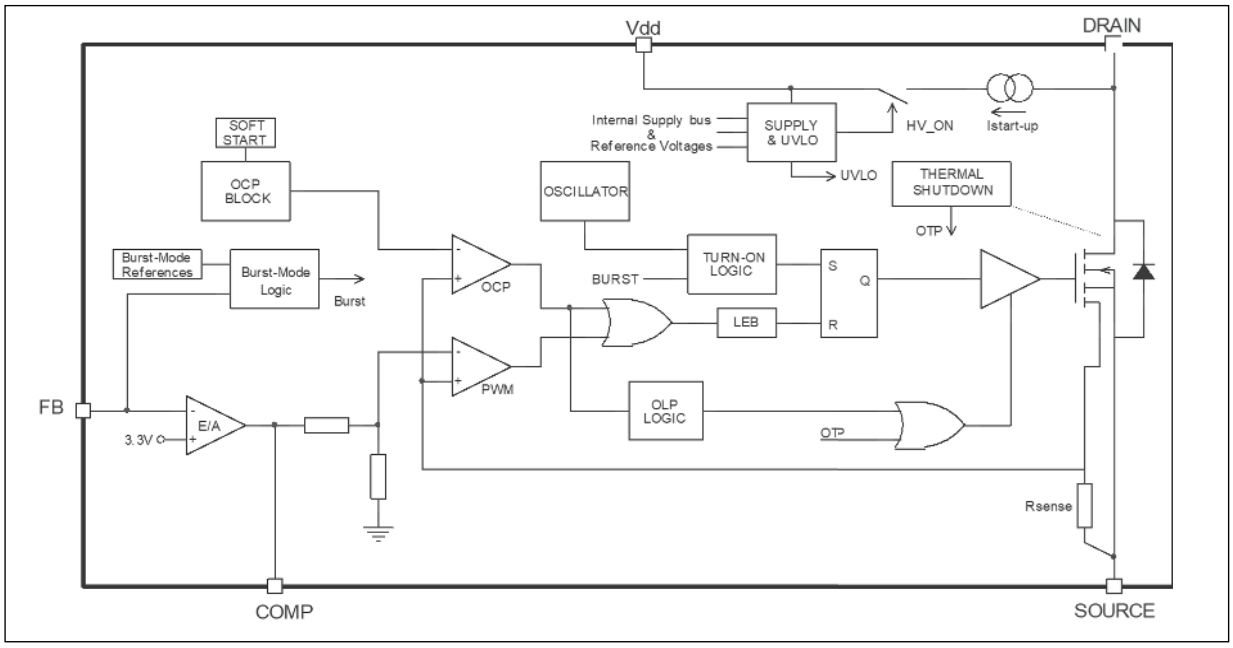
Figure 18. SOA SSOP10 package



4 General description

4.1 Block diagram

Figure 19. Block diagram



4.2 Typical power capability

Table 8. Typical power

Vin: 230 Vac		Vin: 85-265Vac		Vin: 85-440Vac	
Adapter(1)	**Open frame(2)**	**Adapter(1)**	**Open frame(2)**	**Adapter(1)**	**Open frame(2)**
16W	20W	10W	12W	10W	12W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heatsinking.

4.3 Primary MOSFET

The power section is implemented with an N-channel power MOSFET with a breakdown voltage of 1050 V min. and a maximum $R_{DS(ON)}$ of 7 Ω. It includes a sense-FET structure to allow a virtually lossless current sensing and the thermal sensor.

The gate driver of the power MOSFET is designed to supply a controlled gate current during both turn-ON and turn-OFF in order to minimize common mode EMI. During UVLO conditions, an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned ON accidentally.

4.4 High voltage startup

The high voltage current generator is supplied by the DRAIN pin. At the first startup of the converter, it is enabled when the voltage across the input bulk capacitor reaches the V_{DRAIN_START} threshold, sourcing the I_{DDch1} current; as the V_{DD} voltage reaches the V_{DDon} start-up threshold, the power section starts switching and the high voltage current generator is turned OFF. The VIPer26K is powered by the external source. After the startup, the auxiliary winding or the diode connected to the output voltage have to power the V_{DD} capacitor with voltage higher than the V_{DDCSon} threshold. During the switching, the internal current source is disabled and the consumptions are minimized.

In case of fault, the switching is stopped and the device is self-biased by the internal high voltage current source; it is activated between the levels V_{DDCSon} and V_{DDon}, delivering the current I_{DDch2} to the VDD capacitor during the MOSFET OFF time.

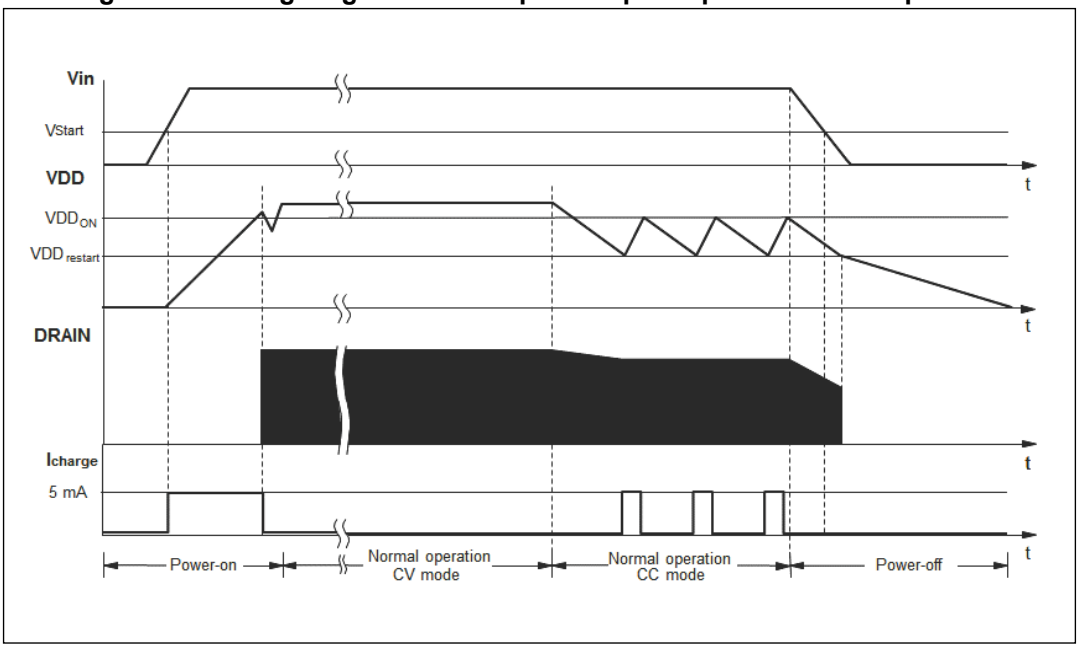
If a very low main input voltage is applied to the converter, it is strongly recommended to choose the V_{DD} capacitor value by the following formula:

Equation 1

$$C_{VDD} = \frac{I_{DDCH1} \cdot t_{OVL}}{V_{DD} - V_{DDoff}}$$

At converter power-down, the V_{DD} voltage drops and the converter activity stops as it falls below the V_{DDoff} threshold.

Figure 20. Timing diagram: normal power-up and power-down sequences



4.5 Oscillator

The switching frequency is internally fixed at 60 kHz.

The switching frequency is modulated by approximately ±4 kHz at 230 Hz (typical) rate, so that the resulting spread spectrum action distributes the energy of each harmonic of the switching frequency over a number of sideband harmonics having the same energy on the whole but smaller amplitudes.

4.6 Soft-start

During the converters' start-up phase, the soft-start function progressively increases the cycle-by-cycle drain current limit, up to the default value I_{DLIM}. In this way, the drain current is further limited and the output voltage is progressively increased reducing the stress on the secondary diode. The soft-start time is internally fixed to t_{SS}, and the function is activated for any attempt of converter startup and after a fault event.

This function helps prevent transformer saturation during startup and short-circuit.

4.7 Current limit set point

The VIPer26K includes a current mode PWM controller: cycle by cycle the drain current is sensed through the integrated resistor R_{SENSE} and the voltage is applied to the non-inverting input of the PWM comparator. As soon as the sensed voltage is equal to the voltage derived from the COMP pin, the power MOSFET is switched OFF.

In parallel with the PWM operations, the comparator OCP checks the level of the drain current and switches OFF the power MOSFET in case the current is higher than the threshold I_{Dlim}.

The IC is available with two different drain current limitations: the VIPer267K has a 700 mA (typical value), whereas the VIPer265K is available with 500 mA current limitation.

Both values are ensured with tolerance reported in *Table 3*.

4.8 FB pin and COMP pin

The device can be used both in non-isolated and in isolated topology. In the case of non-isolated topology, the feedback signal from the output voltage is applied directly to the FB pin as inverting input of the internal error amplifier having the reference voltage, V_{REF_FB}.

The output of the error amplifier sources and sinks the current, I_{COMP}, respectively to and from the compensation network connected on the COMP pin. This signal is then compared, in the PWM comparator, with the signal coming from the sense-FET; the power MOSFET is switched off when the two values are the same on a cycle-by-cycle basis.

When the power supply output voltage is equal to the error amplifier reference voltage, V_{REF_FB}, a single resistor has to be connected from the output to the FB pin. For higher output voltages the external resistor divider is needed. If the voltage on the FB pin is accidentally left floating, an internal pull-up protects the controller.

The output of the error amplifier is externally accessible through the COMP pin and it's used for the loop compensation: usually an RC network.

In the case of isolated power supply, the internal error amplifier has to be disabled (FB pin shorted to GND). In this case an internal resistor is connected between an internal reference voltage and the COMP pin.

The current loop has to be closed on the COMP pin through the optocoupler in parallel with the compensation network. The V_{COMP} dynamics range is between V_{COMPL} and V_{COMPH}.

When the voltage V_{COMP} drops below the voltage threshold V_{COMPL}, the converter enters burst mode.

When the voltage V_{COMP} rises above the V_{COMPH} threshold, the peak drain current will reach its limit, as well as the deliverable output power.

Figure 21. Feedback circuit

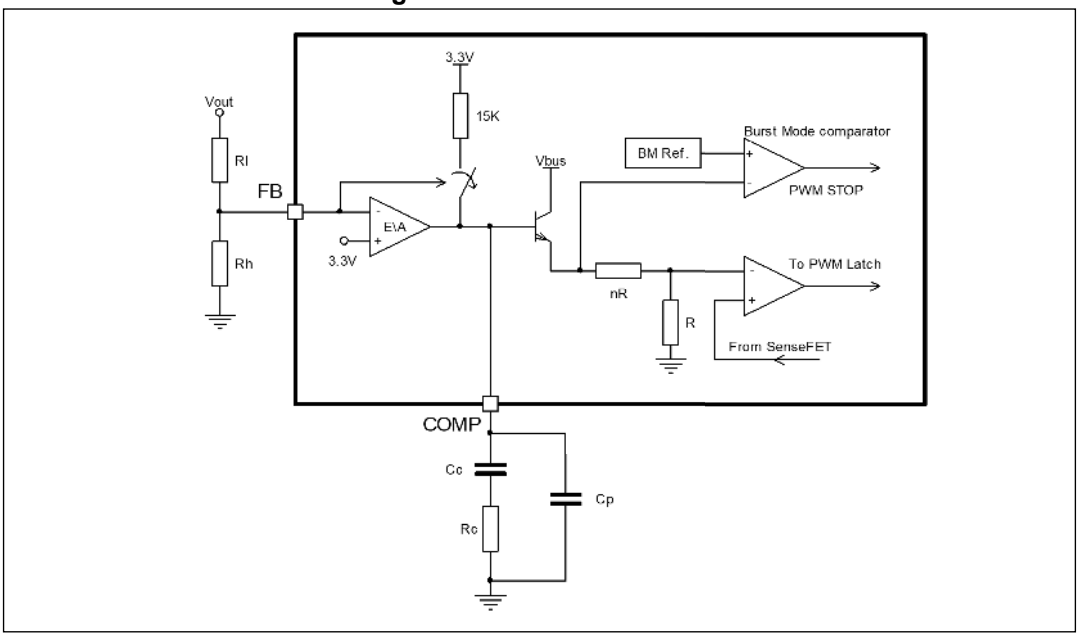
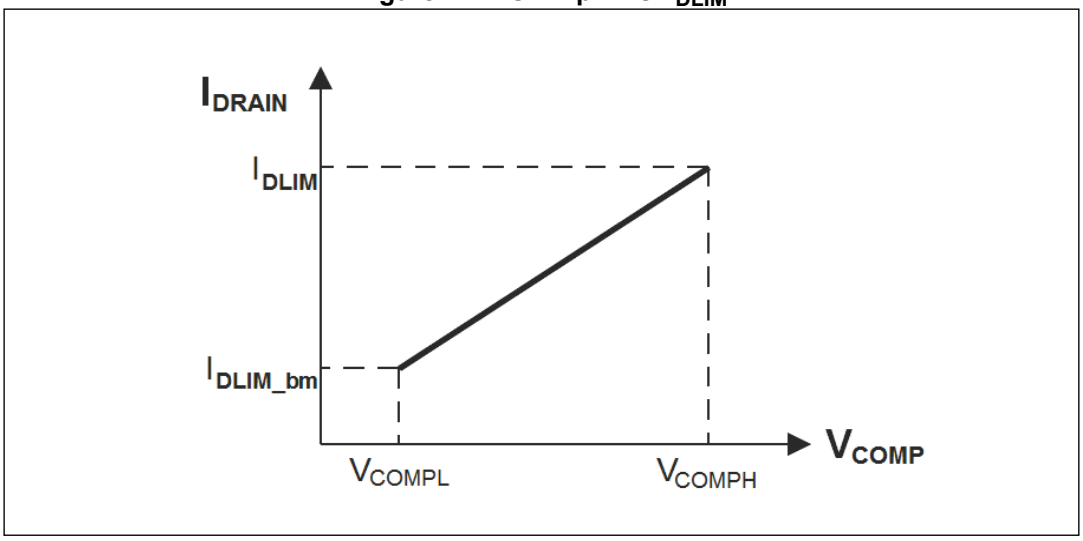


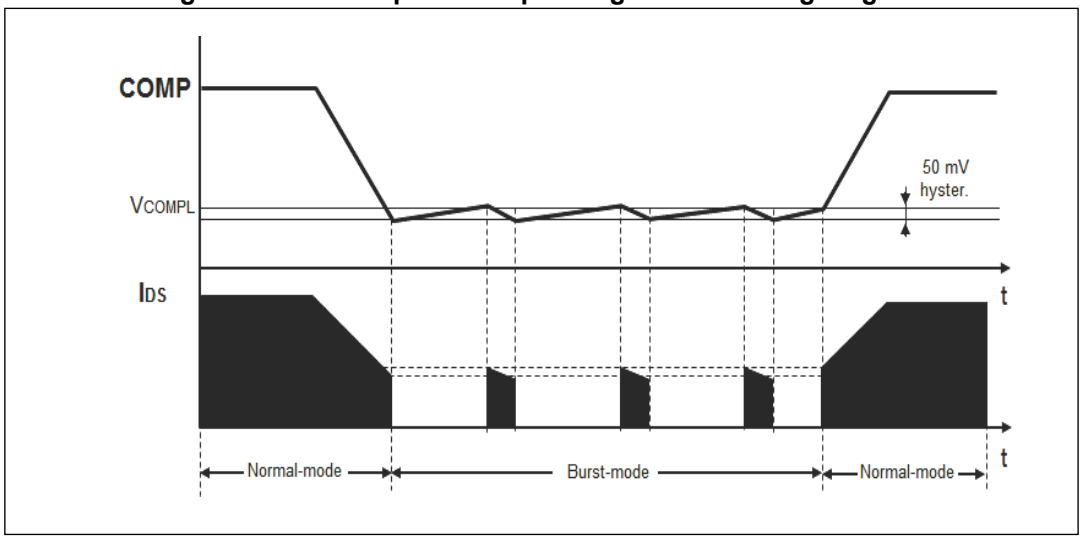
Figure 22. COMP pin vs. I_{DLIM}



4.9 Burst mode

When the voltage V_{COMP} drops below the threshold, V_{COMPL}, the power MOSFET is kept in the OFF state and the consumption is reduced to I_{DD0} current. As a reaction at the energy delivery stop, the V_{COMP} voltage increases and as soon as it exceeds the threshold V_{COMPL} + V_{COMPL_HYS}, the converter starts switching again with consumption level equal to I_{DD1} current. This ON-OFF operation mode, referred to as “burst mode” and reported in *Figure 4*, reduces the average frequency, which can go down even to a few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. During burst mode, the drain current limit is reduced to the value I_{DLIM_bm} in order to avoid the audible noise issue.

Figure 23. Load-dependent operating modes: timing diagram



4.10 Automatic auto restart after overload or short-circuit

The overload protection is implemented in an automatic way using the integrated up-down counter. Every cycle, it is incremented or decremented depending on whether the current logic detects the limit condition or not. The limit condition is the peak drain current, I_{DLIM}.

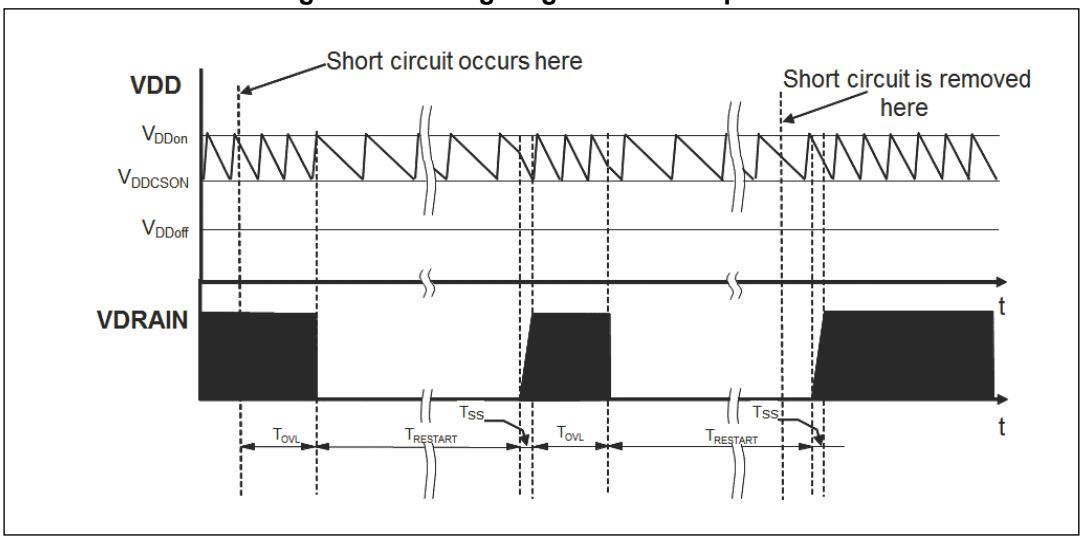
After the reset of the counter, if the peak drain current is continuously equal to the level I_{Dlim}, the counter will be incremented till the fixed time, t_{OVL}, after that the power MOSFET switch ON is disabled. It is activated again, through the soft-start, after the $t_{RESTART}$ time.

In the case of overload or a short-circuit event, the power MOSFET switching is stopped after a time that depends from the counter and that can be as maximum equal to t_{OVL}. The protection occurs in the same way until the overload condition is removed.

This protection ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoiding the IC overheating in case of repeated overload events.

If the overload is removed before the protection tripping, the counter is decremented cycle-by-cycle down to zero and the IC is not stopped.

Figure 24. Timing diagram: OLP sequence



4.11 Open loop failure protection

In case the power supply is built in flyback topology and the VIPer26K is supplied by an auxiliary winding, the converter is protected against feedback loop failure or accidental disconnections of the winding.

If R_H is opened or R_L is shorted, the VIPer26K works at its drain current limitation. The output voltage, V_{OUT}, increases and also the auxiliary voltage, V_{AUX}, which is coupled with the output through the secondary-to-auxiliary turns ratio.

As the auxiliary voltage increases up to the internal V_{DD} active clamp, $V_{DDclamp}$ and the clamp current injected on the V_{DD} pin exceeds the latch threshold, I_{DDol}, a fault signal is internally generated.

In order to distinguish an actual malfunction from a bad auxiliary winding design, both the above conditions (drain current equal to the drain current limitation and current higher than I_{DDol} through V_{DD} clamp) have to be verified to reveal the fault.

If R_L is opened or R_H is shorted, the output voltage, V_{OUT}, is clamped to the reference voltage V_{REF_FB} (in case of non-isolated flyback) or to the external TL voltage reference (in case of isolated flyback).

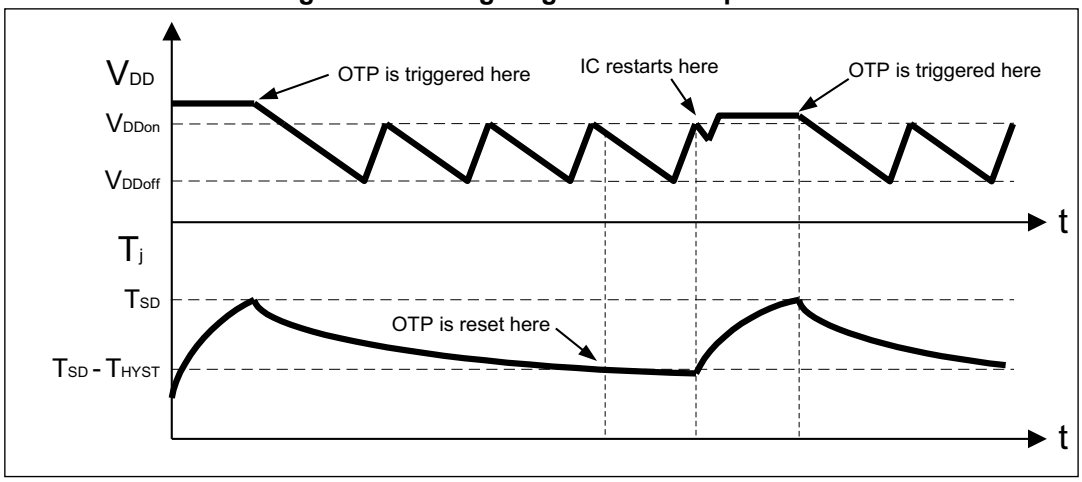
4.12 Thermal shutdown

When the controller temperature exceeds the shutdown threshold, T_{SD}, the device is shut down to prevent any dangerous overheating for the system and the VDD pin is continuously recycled between V_{DDon} and V_{DDoff} to keep the controller alive.

Once the $t_{RESTART}$ time is elapsed, when temperature falls T_{HYST} below the OTP threshold, the IC starts once it has reached again the V_{DDon}.

The OTP timing diagram is shown in *Figure 25*.

Figure 25. Timing diagram: OLP sequence



5 Application information

Figure 26. Typical isolated flyback configuration with secondary regulation

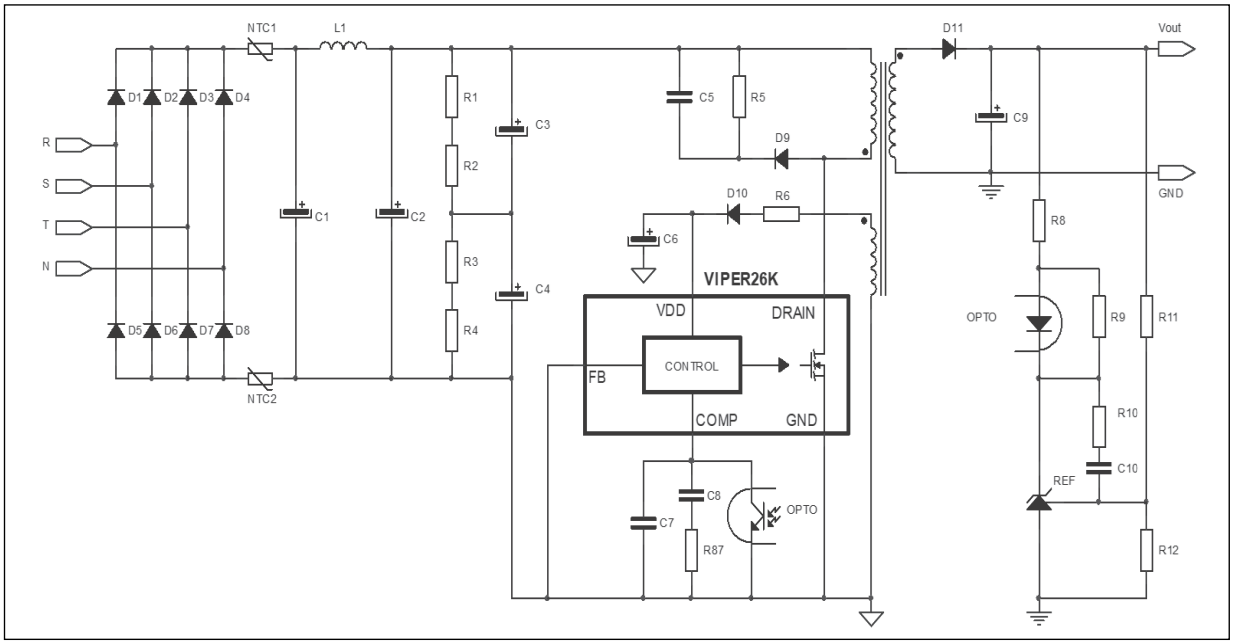


Figure 27. Typical isolated flyback configuration with primary regulation

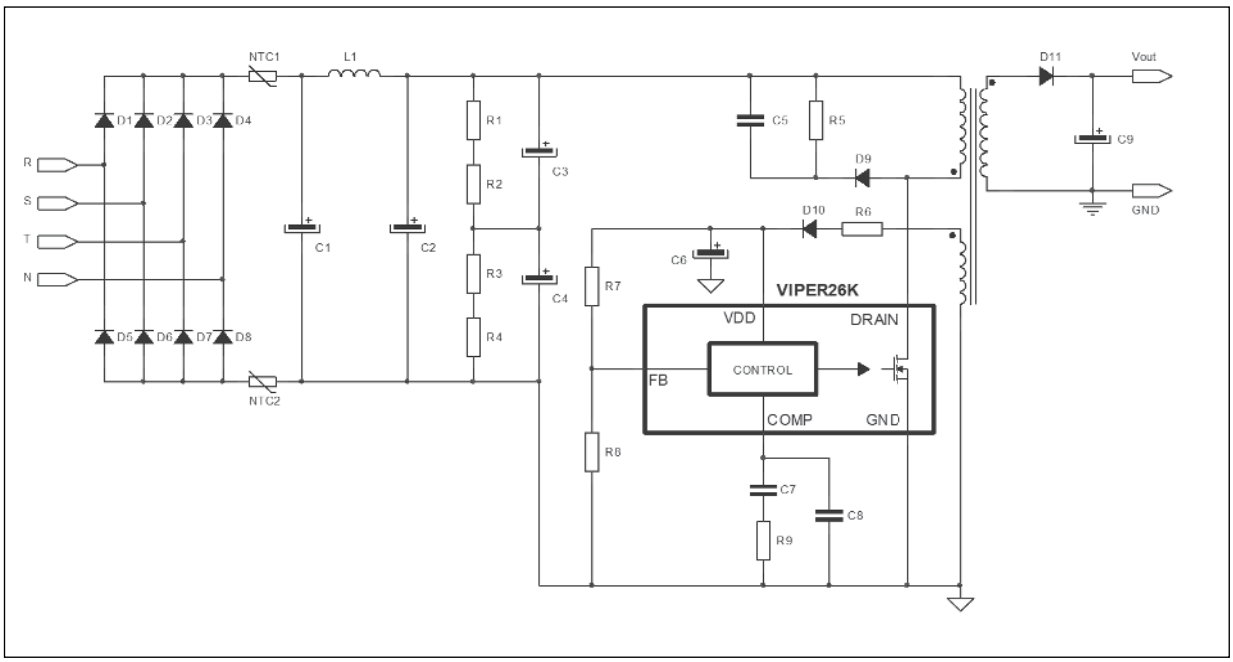


Figure 28. Typical non isolated flyback configuration

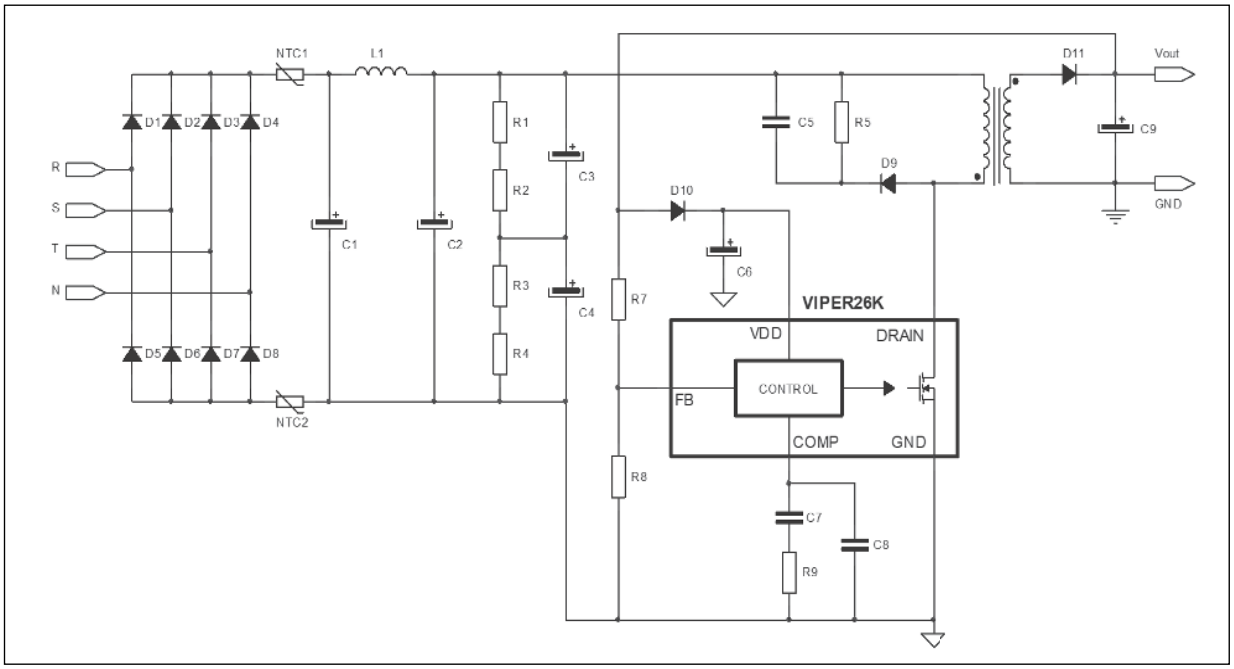
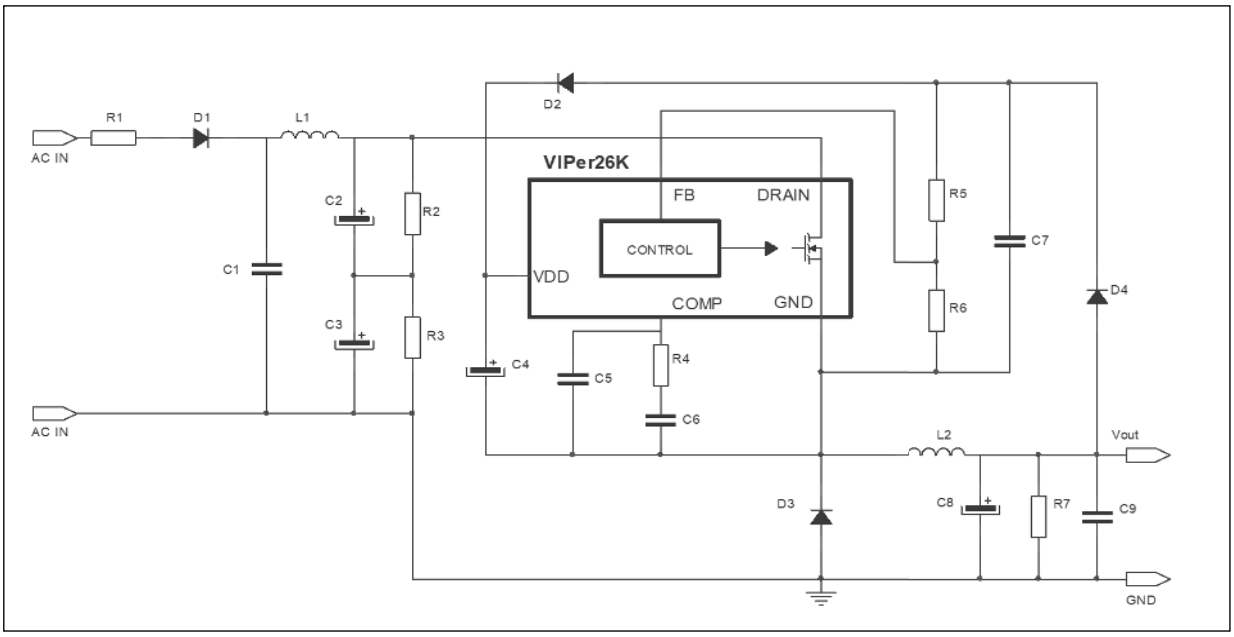


Figure 29. Ultra wide range Buck configuration



5.1 Layout guidelines and design recommendations

A proper printed circuit board layout ensures the correct operation of any switch-mode converter and this is also true for the VIPer. The main reasons to have a proper PCB layout are:

- Provides clean signals to the IC, ensuring good immunity against external and switching noises.
- Reduces the electromagnetic interferences, both radiated and conducted, to pass the EMC tests more easily.

If the VIPer is used to design an SMPS, the following basic rules should be considered:

- **Separate signal from power tracks**. Generally, traces carrying signal currents should run far from others carrying pulsed currents or with fast swinging voltages. Signal ground traces should be connected to the IC signal ground, GND, using a single “star point”, placed close to the IC. Power ground traces should be connected to the IC power ground, GND. The compensation network should be connected to the COMP, maintaining the trace to GND as short as possible. In the case of two-layer PCB, it is good practice to route signal traces on one PCB side and power traces on the other side.
- **Filter sensitive pins**. Some crucial points of the circuit need or may need filtering. A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor (a few hundreds pF up to 0.1 µF) should be connected across VCC and GND, placed as close as possible to the IC. With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.
- **Keep power loops as confined as possible**. The area circumscribed by current loops where high pulsed current flow should be minimized to reduce its parasitic self-inductance and the radiated electromagnetic field. As a consequence, the electromagnetic interferences produced by the power supply during the switching are highly reduced. In a flyback converter the most critical loops are: the one including the input bulk capacitor, the power switch, the power transformer, the one including the snubber, the one including the secondary winding, the output rectifier and the output capacitor. In a buck converter the most critical loop is the one including the input bulk capacitor, the power switch, the power inductor, the output capacitor and the freewheeling diode.
- **Reduce line lengths**. Any wire acts as an antenna. With the very short rise times exhibited by EFT pulses, any antenna can receive high voltage spikes. By reducing line lengths, the level of received radiated energy is reduced, and the resulting spikes from electrostatic discharges are lower. This also keeps both resistive and inductive effects to a minimum. In particular, all traces carrying high currents, especially if pulsed (tracks of the power loops) should be as short and wide as possible.
- **Optimize track routing**. As levels of pickup from static discharges are likely greater near the edges of the board, it is wise to keep any sensitive lines away from these areas. Input and output lines often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable. Since vias are to be considered inductive elements, it is recommended to minimize their number in the signal path and avoid them in the power path.
- **Improve thermal dissipation**. An adequate copper area has to be provided under the DRAIN pins as heatsink, while it is not recommended to place large copper areas on the GND.

Figure 30. Recommended routing for flyback converter

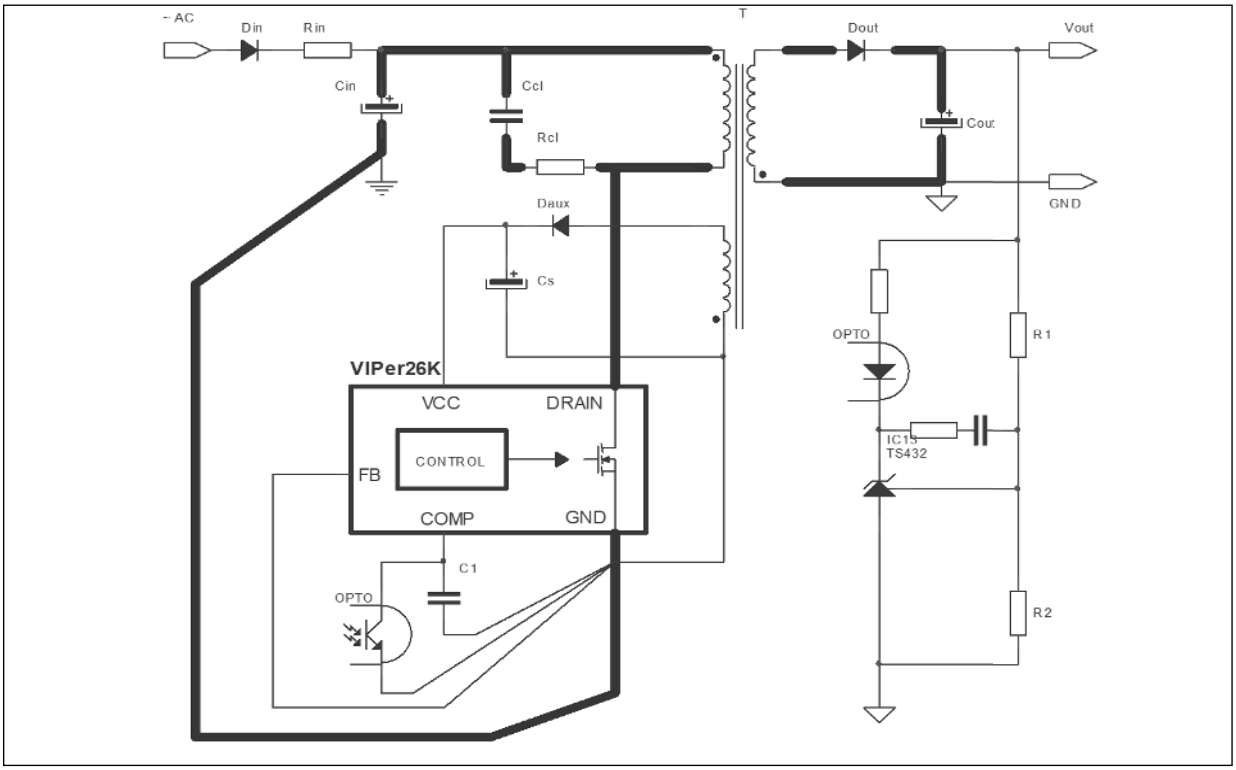
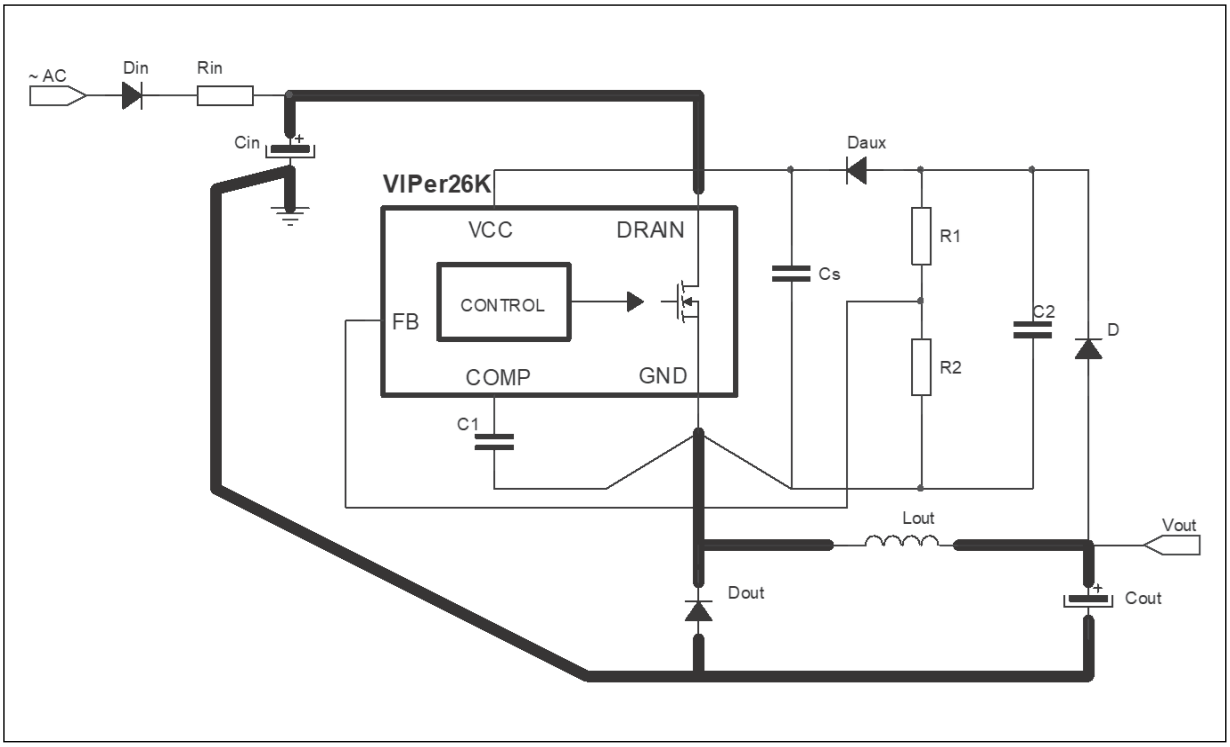


Figure 31. Recommended routing for Buck converter



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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6.1 SO16N package information

Figure 32. SO16N package outline

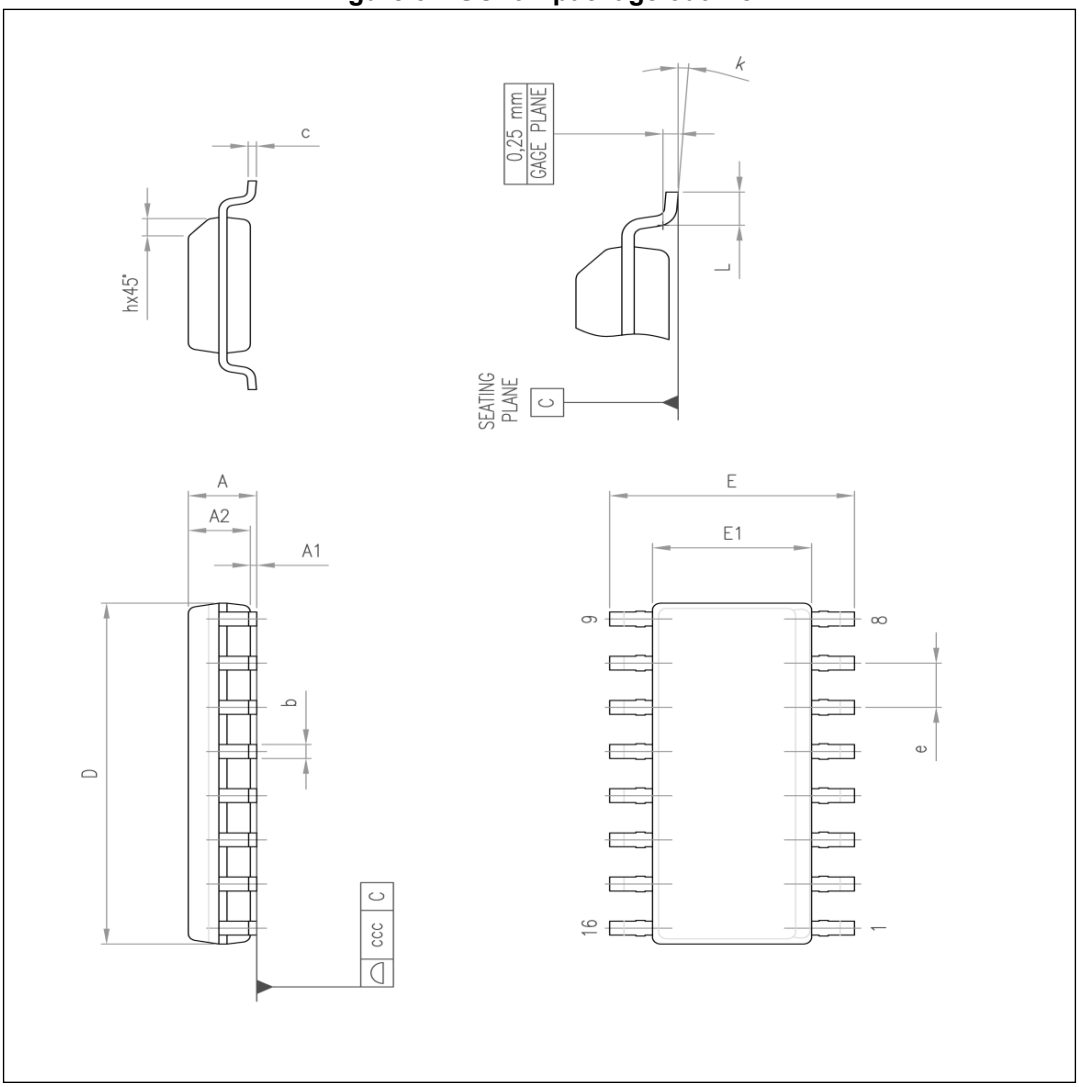

Table 9. SO16N mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			1.1

7 Order code

Table 10. Order codes

Order Code	Package	IDLIM	Packaging
VIPER265KDTR	SO16N	500 mA	Tape & Reel
VIPER267KDTR		700 mA	

8 Revision history

Table 11. Document history

Date	Revision	Changes
23-Apr-2019	1	Initial release.

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