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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2015

FDC3535

P-Channel Power Trench® MOSFET

-80 V, -2.1 A, 183 mΩ

Features

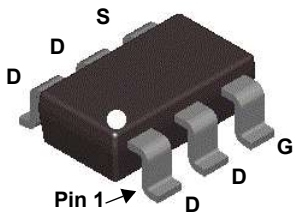
- Max $r_{DS(on)}$ = 183 mΩ at V_{GS} = -10 V, I_D = -2.1 A
- Max $r_{DS(on)}$ = 233 mΩ at V_{GS} = -4.5 V, I_D = -1.9 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

General Description

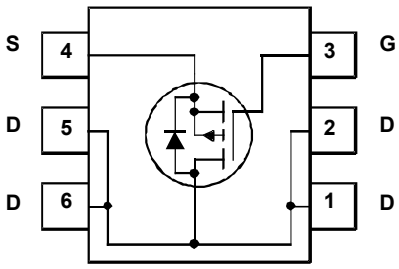
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- Load Switch
- Synchronous Rectifier



SuperSOT™ -6



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		-80	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous	(Note 1a)	-2.1	A
	-Pulsed		-10	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	37	mJ
P_D	Power Dissipation	(Note 1a)	1.6	W
	Power Dissipation	(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		30	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78	

Package Marking and Ordering Information

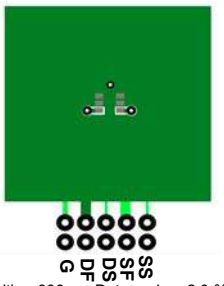
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.535	FDC3535	SSOT-6	7 ”	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

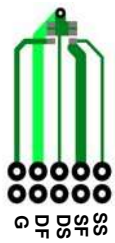
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-64		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -64 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -2.1 A		147	183	mΩ
		V_{GS} = -4.5 V, I_D = -1.9 A		176	233	
		V_{GS} = -10 V, I_D = -2.1 A, T_J = 125 °C		246	307	
g_{FS}	Forward Transconductance	V_{DD} = -10 V, I_D = -2.1 A		6.3		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -40 V, V_{GS} = 0 V, f = 1 MHz		659	880	pF
C_{oss}	Output Capacitance			49	65	pF
C_{rss}	Reverse Transfer Capacitance			24	40	pF
R_g	Gate Resistance			5.7		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -40 V, I_D = -2.1 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		6.5	13	ns
t_r	Rise Time			3.1	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	38	ns
t_f	Fall Time			2.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to -10 V; V_{DD} = -40 V, I_D = -2.1 A		14	20	nC
	Total Gate Charge	V_{GS} = 0 V to -4.5 V; V_{DD} = -40 V, I_D = -2.1 A		6.8	10	nC
Q_{gs}	Total Gate Charge	V_{DD} = -40 V, I_D = -2.1 A		1.6		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = -40 V, I_D = -2.1 A		2.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		-0.81	-1.3	V
t_{rr}	Reverse Recovery Time	I_F = -2.1 A, di/dt = 100 A/μs		25	40	ns
Q_{rr}	Reverse Recovery Charge			23	38	nC

NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b.175 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

3. Starting T_J = 25 °C, L = 3 mH, I_{AS} = -5 A, V_{DD} = -80 V, V_{GS} = -10 V.

Typical Characteristics T_J = 25 °C unless otherwise noted

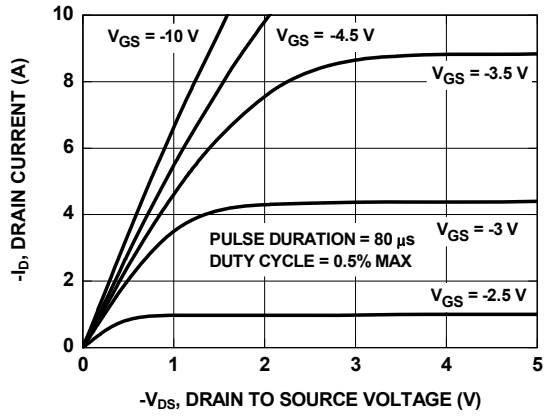


Figure 1. On-Region Characteristics

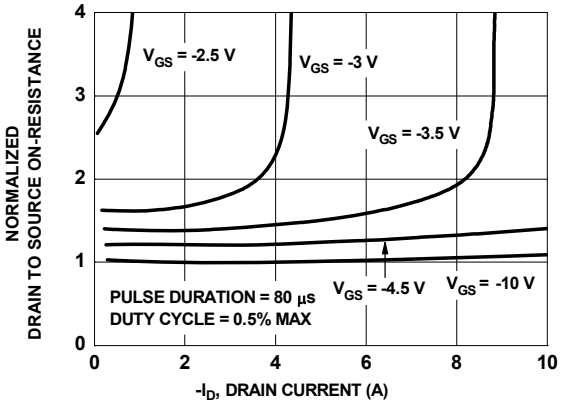


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

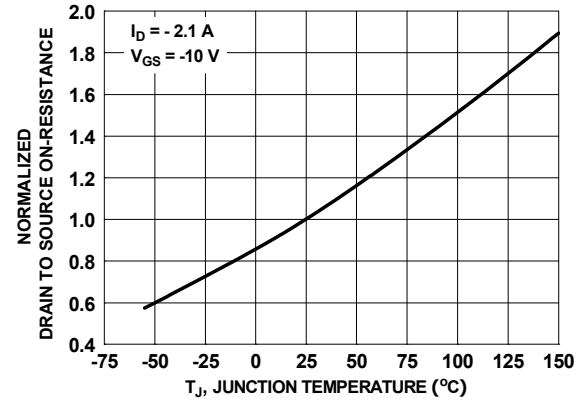


Figure 3. Normalized On-Resistance vs Junction Temperature

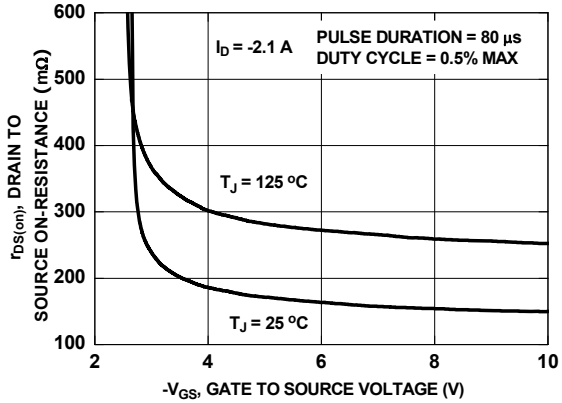


Figure 4. On-Resistance vs Gate to Source Voltage

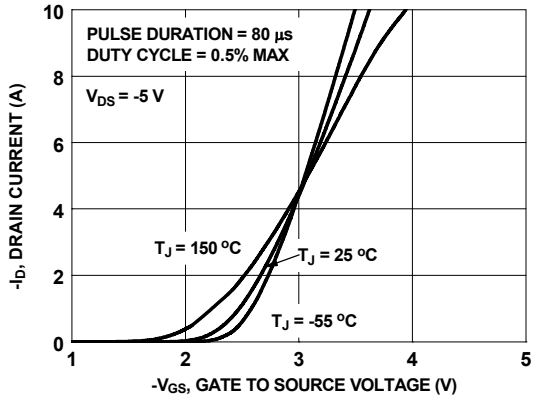


Figure 5. Transfer Characteristics

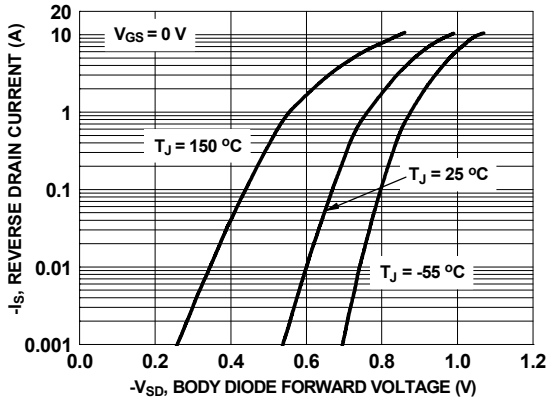


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

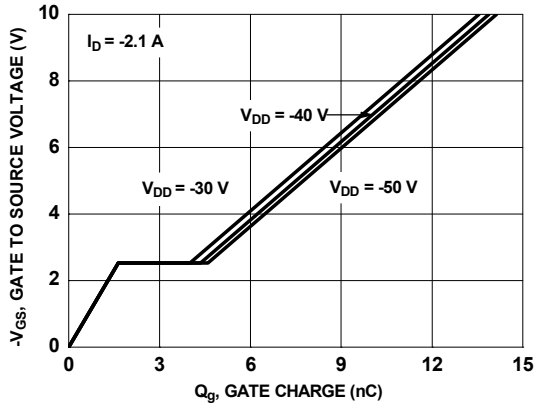


Figure 7. Gate Charge Characteristics

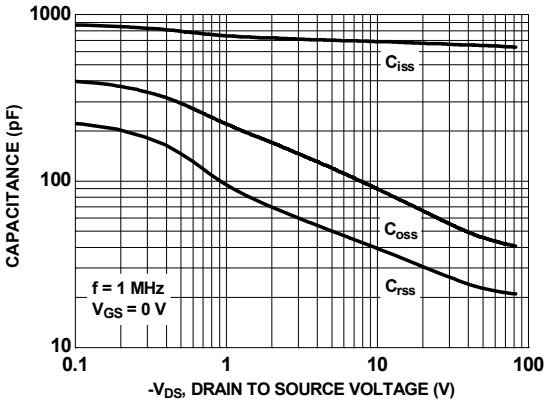


Figure 8. Capacitance vs Drain to Source Voltage

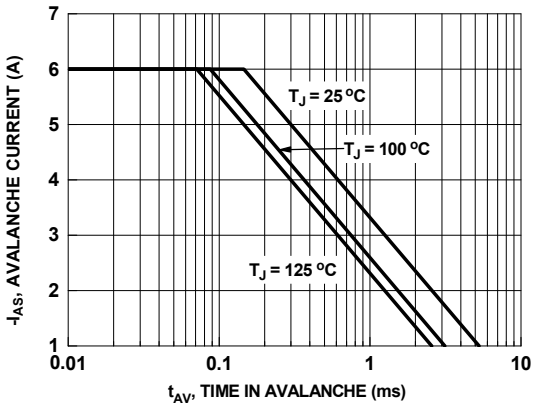


Figure 9. Unclamped Inductive Switching Capability

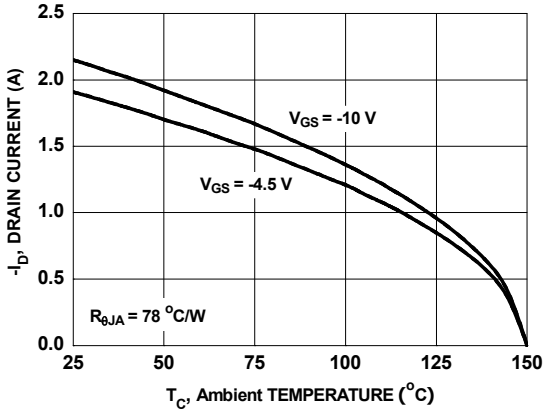


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

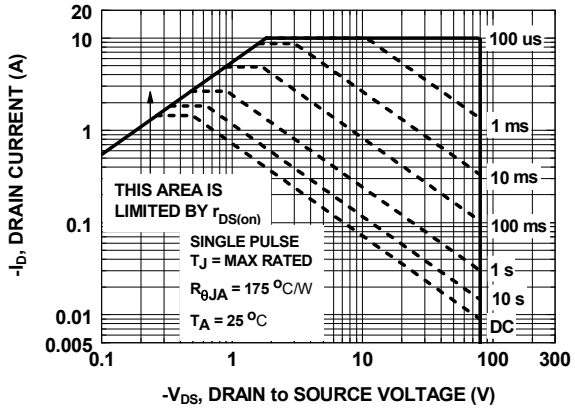


Figure 11. Forward Bias Safe Operating Area

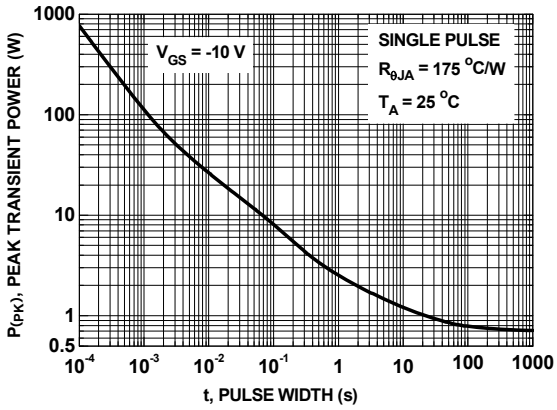


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

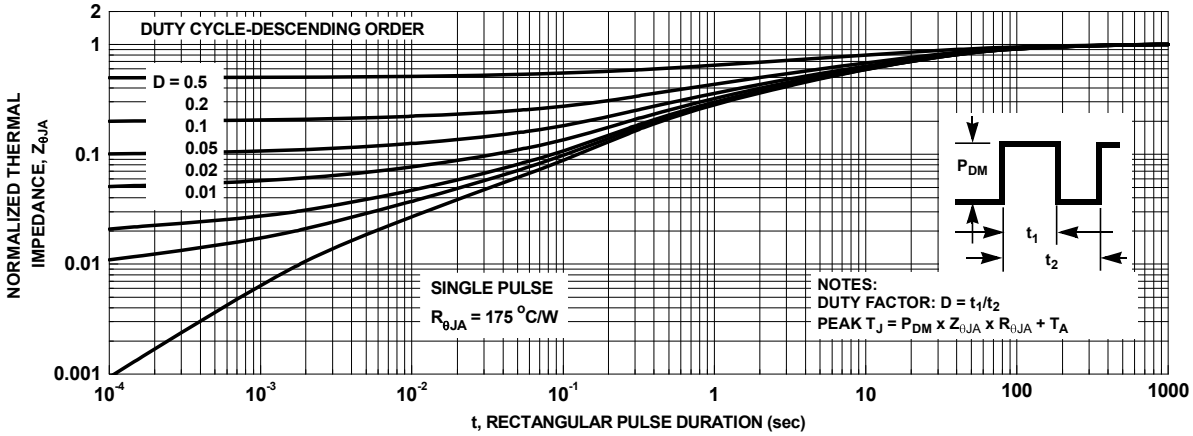
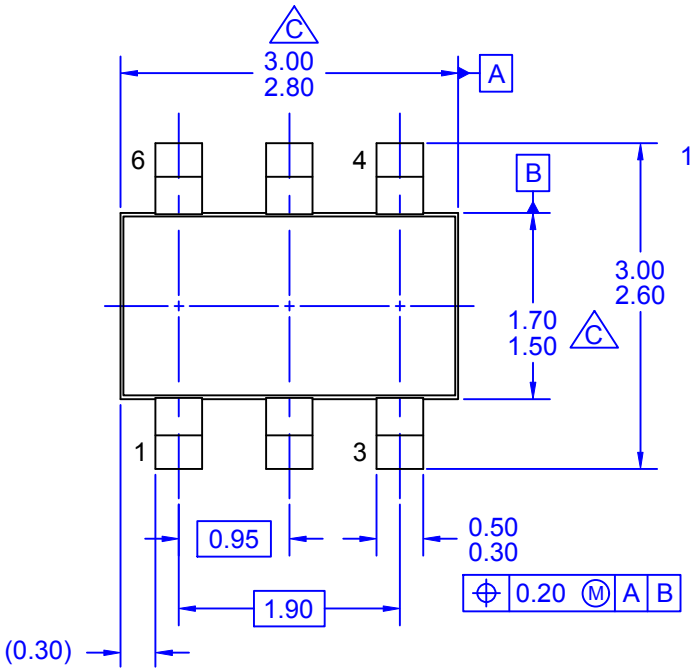
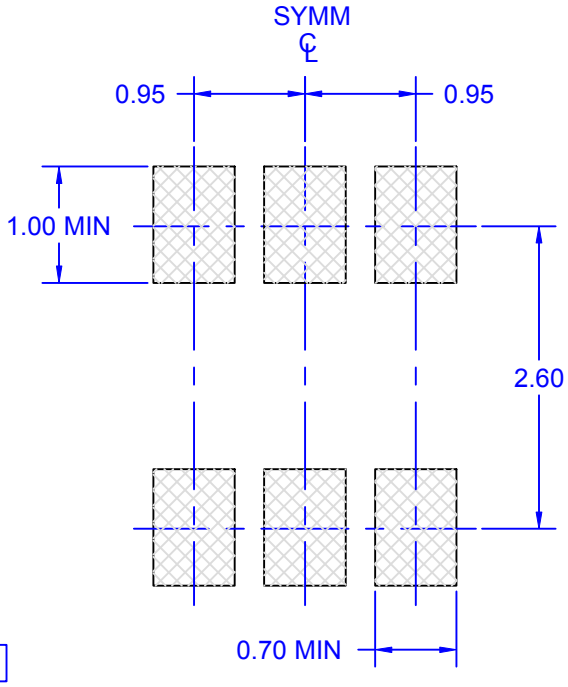
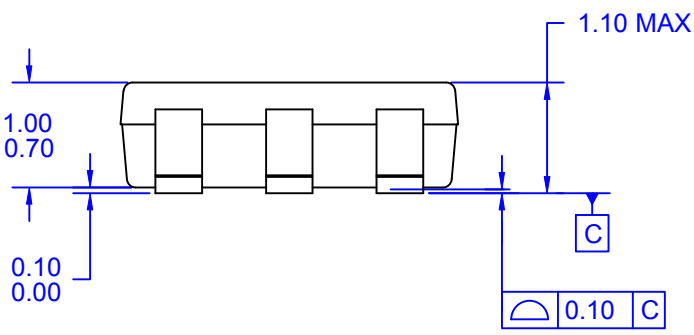


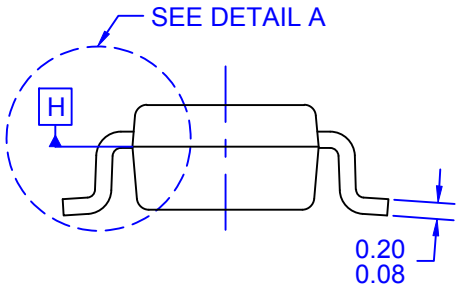
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

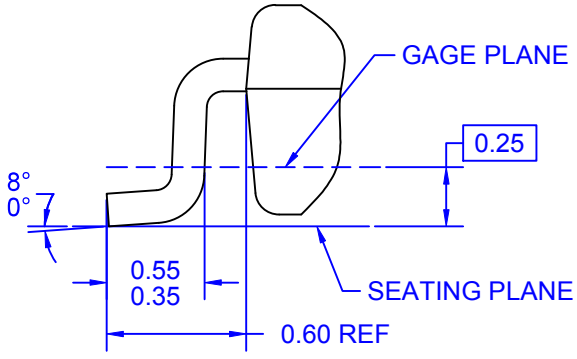




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 50X

NOTES: UNLESS OTHERWISE SPECIFIED

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C) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25mm PER END. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. PACKAGE LENGTH AND WIDTH DIMENSIONS ARE DETERMINED AT DATUM H.

D) DRAWING FILE NAME: MKT-MA06AREVF

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