82430FX PCIset DATASHEET 82437FX SYSTEM CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP)

- **Supports all 3V Pentium® Processors**
- **Integrated Second Level Cache Controller**
  - **— Direct Mapped Organization**
  - **— Write-Back Cache Policy**
  - **— Cacheless, 256-Kbyte, and 512-Kbyte**
  - **— Standard Burst and Pipelined Burst SRAMs**
  - **— Cache Hit Read/Write Cycle Timings at 3-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **— Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **— Integrated Tag/Valid Status Bits for Cost Savings and Performance**
  - **— Supports 5V SRAMs for Tag Address**
- **Integrated DRAM Controller**
  - **— 64-Bit Data Path to Memory**
  - **— 4 Mbytes to 128 Mbytes Main Memory**
  - **— EDO/Hyper Page Mode DRAM (x-2-2-2 Reads) or Standard Page Mode DRAMs**
  - **— 5 RAS Lines**
  - **— 4 Qword Deep Buffer for 3-1-1-1 Posted Write Cycles**
  - **— Symmetrical and Asymmetrical DRAMs**
  - **— 3V or 5V DRAMs**
- **EDO DRAM Support**
  - **— Highest Performance with Burst or Pipelined Burst SRAMs**
  - **— Superior Cacheless Designs**
- **Fully Synchronous 25/30/33 MHz PCI Bus Interface**
  - **— 100 MB/s Instant Access Enables Native Signal Processing (NSP) on Pentium Processors**
  - **— Synchronized CPU-to-PCI Interface for High Performance Graphics**
  - **— PCI Bus Arbiter: PIIX and Four PCI Bus Masters Supported**
  - **— CPU-to-PCI Memory Write Posting with 4 Dword Deep Buffers**
  - **— Converts Back-to-Back Sequential CPU to PCI Memory Writes to PCI Burst Writes**
  - **— PCI-to-DRAM Posting of 12 Dwords**
  - **— PCI-to-DRAM up to 120 Mbytes/Sec Bandwidth Utilizing Snoop Ahead Feature**
- **NAND Tree for Board-Level ATE Testing**
- **208 Pin QFP for the 82437FX System Controller (TSC); 100 Pin QFP for Each 82438FX Data Path (TDP)**
- **Supported Kits**
  - **— 82437FX ISA Kit (TSC, TDPs, PIIX)**

The 82430FX PCIset consists of the 82437FX System Controller (TSC), two 82438FX Data Paths (TDP), and the 82371FB PCI ISA IDE Xcelerator (PIIX). The PCIset forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The TSC integrates the cache and main memory DRAM control functions and provides bus control for transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with either standard, burst, or pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the TSC's DRAM controller, five rows are supported for up to 128 Mbytes of main memory. The TSC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, the TSC allows PCI masters to achieve full PCI bandwidth. The TDPs provide the data paths between the CPU/cache, main memory, and PCI. For increased system performance, the TDPs contain read prefetch and posted write buffers.

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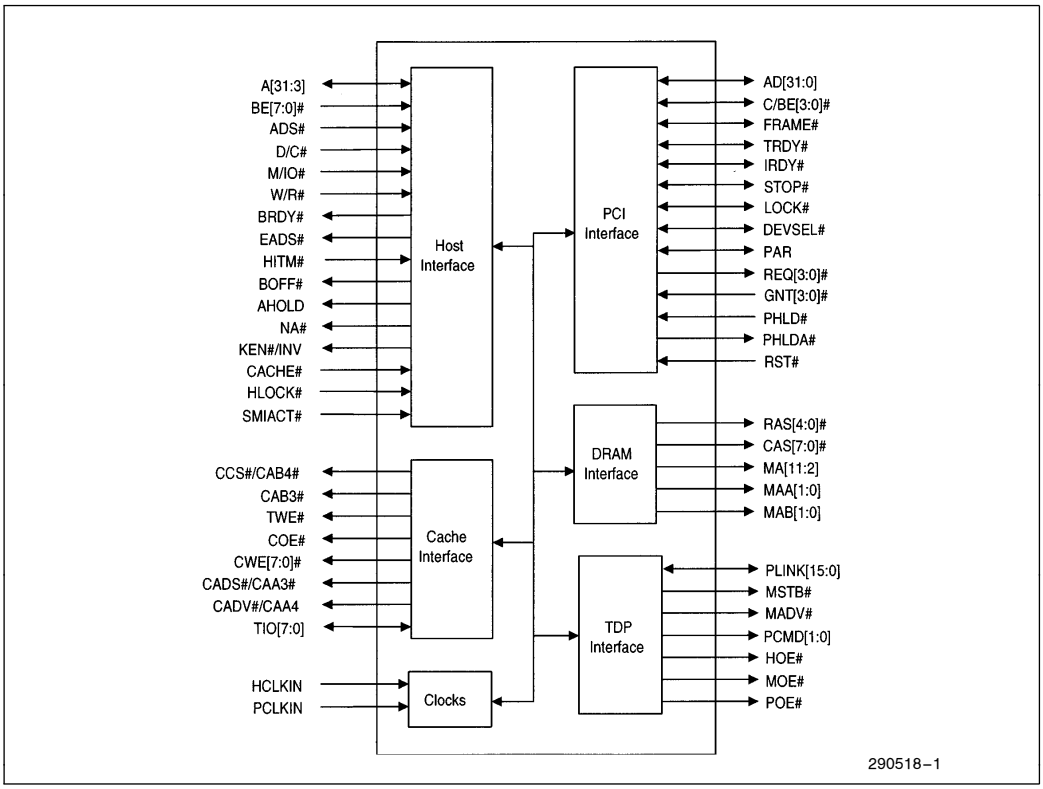
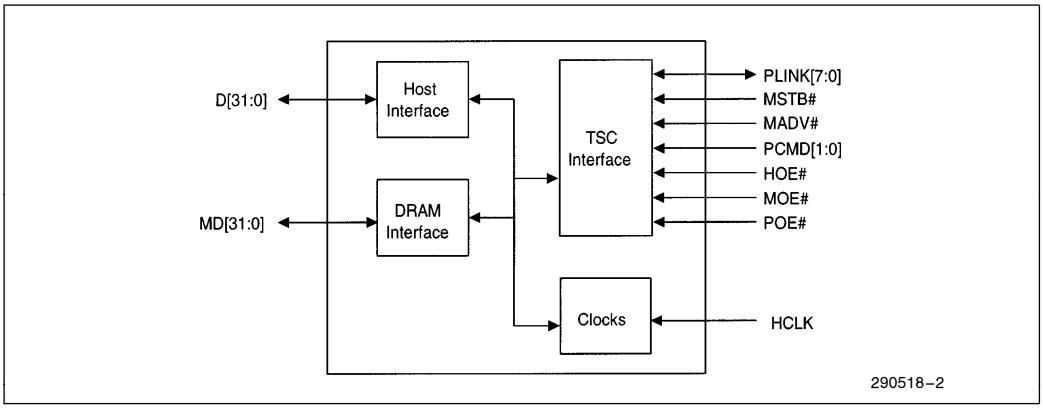


82437FX TSC Simplified Block Diagram



82438FX TDP Simplified Block Diagram

82430FX PCIset DATASHEET 82437FX SYSTEM CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP)

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1.0 ARCHITECTURE OVERVIEW OF TSC/TDP

The 82430FX PCIset (Figure 1) consists of the 82437FX System Controller (TSC), two 82438FX Data Path (TDP) units, and the 82371FB PCI IDE ISA Xcelerator (PIIX). The TSC and two TDPs form a Host-to-PCI bridge. The PIIX is a multi-function PCI device providing a PCI-to-ISA bridge and a fast IDE interface. The PIIX also provides power management and has a plug and play port.

The two TDPs provide a 64-bit data path to the host and to main memory and provide a 16-bit data path (PLINK) between the TSC and TDP. PLINK provides the data path for CPU to PCI accesses and for PCI to main memory accesses. The TSC and TDP bus interfaces are designed for 3V and 5V busses. The TSC/TDP connect directly to the Pentium® processor 3V host bus; The TSC/TDP connect directly to 5V or 3V main memory DRAMs; and the TSC connects directly to the 5V PCI Bus.

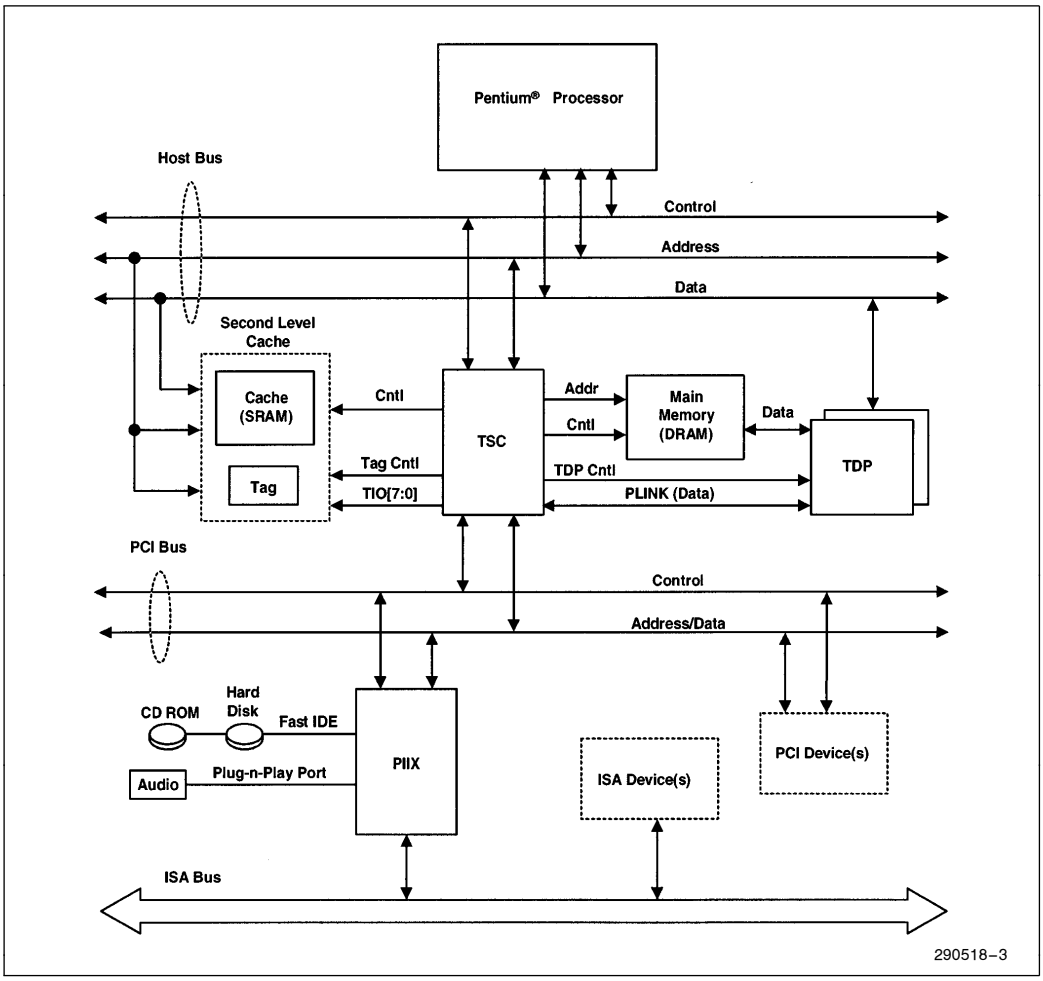


Figure 1. 82430FX PCIset System

DRAM Interface

The DRAM interface is a 64-bit data path that supports both standard page mode and Extended Data Out (EDO) (also known as Hyper Page Mode) memory. The DRAM interface supports 4 Mbytes to 128 Mbytes with five RAS lines available and also supports symmetrical and asymmetrical addressing for 512K, 1M, 2M, and 4M deep DRAMs.

Second Level Cache

The TSC supports a write-back cache policy providing all necessary snoop functions and inquire cycles. The second level cache is direct mapped and supports both a 256-Kbyte or 512-Kbyte SRAM configuration using either burst, pipelined burst, or standard SRAMs. The burst 256-Kbyte configuration performance is 3-1-1-1 for read/write cycles; pipelined back-to-back reads can maintain a 3-1-1-1-1-1-1-1 transfer rate.

TDP

Two TDPs create a 64-bit CPU and main memory data path. The TDP's also interface to the TSC's 16-bit PLINK inter-chip bus for PCI transactions. The combination of the 64-bit memory path and the 16-bit PLINK bus make the TDP's a cost effective solution, providing optimal CPU-to-main memory performance while maintaining a small package footprint (100 pins each).

PCI Interface

The PCI interface is 2.0 compliant and supports up to 4 PCI bus masters in addition to the PIIX bus master requests. While the TSC and TDP's together provide the interface between PCI and main memory, only the TSC connects to the PCI Bus.

Buffers

The TSC and TDP's together contain buffers for optimizing data flow. A four Qword deep buffer is provided for CPU-to-main memory writes, second level cache write back cycles, and PCI-to-main memory transfers. This buffer is used to achieve 3-1-1-1 posted writes to main memory. A four Dword buffer is used for CPU-to-PCI writes. In addition, a four Dword PCI Write Buffer is provided which is combined with the DRAM Write Buffer to supply a 12 Dword deep buffering for PCI to main memory writes.

System Clocking

The processor, second level cache, main memory subsystem, and PLINK bus all run synchronous to the host clock. The PCI clock runs synchronously at half the host clock frequency. The TSC and TDP's have a host clock input and the TSC has a PCI clock input. These clocks are derived from an external source and have a maximum clock skew requirement with respect to each other.

2.0 SIGNAL DESCRIPTION

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The ''#'' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When ''#'' is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of ''active-low'' and ''active-high'' signals. The term **assert**, or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation** indicates that a signal is inactive.

The following notations are used to describe the signal type.

I Input is a standard input-only signal.

O Totem pole output is a standard active driver.

o/d Open drain.

t/s Tri-State is a bi-directional, tri-state input/output pin.

s/t/s Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives a s/t/s pin low must drive it high for at least one clock before letting it float. A new agent can not start driving a s/t/s signal any sooner than one clock after the previous owner tri-states it. An external pull-up is required to sustain the inactive state until another agent drives it and must be provided by the central resource.

2.1 TSC Signals

2.1.1 HOST INTERFACE (TSC)

Signal Name	Type	Description
A[31:3]	I/O 3V	**ADDRESS BUS:** A[31:3] connect to the address bus of the CPU. During CPU cycles A[31:3] are inputs. These signals are driven by the TSC during cache snoop operations. Note that A[31:28] provide poweron/reset strapping options for the second level cache.
BE[7:0]#	I 3V	**BYTE ENABLES:** The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes are provided to the CPU if the cycle is a cacheable read regardless of the state of BE[7:0]#.
ADS#	I 3V	**ADDRESS STATUS:** The CPU asserts ADS# to indicate that a new bus cycle is being driven.
BRDY#	O 3V	**BUS READY:** The TSC asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
NA#	O 3V	**NEXT ADDRESS:** When burst SRAMs are used in the second level cache or the second level cache is disabled, the TSC asserts NA# in T2 during CPU write cycles and with the first assertion of BRDY# during CPU linefills. NA# is never asserted if the second level cache is enabled with asynchronous SRAMs. NA# on the TSC must be connected to the CPU NA# pin for all configurations.
AHOLD	O 3V	**ADDRESS HOLD:** The TSC asserts AHOLD when a PCI master is accessing main memory. AHOLD is held for the duration of the PCI burst transfer. The TSC negates AHOLD when the PCI to main memory read/write cycles complete and during PCI peer transfers.
EADS#	O 3V	**EXTERNAL ADDRESS STROBE:** Asserted by the TSC to inquire the first level cache when servicing PCI master accesses to main memory.
BOFF#	O 3V	**BACK OFF:** Asserted by the TSC when required to terminate a CPU cycle that was in progress.
HITM#	I 3V	**HIT MODIFIED:** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.
M/IO#, D/C#, W/R#	I 3V	**MEMORY/IO; DATA/CONTROL; WRITE/READ:** Asserted by the CPU with ADS# to indicate the type of cycle on the host bus.
HLOCK#	I 3V	**HOST LOCK:** All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e., no PCI activity to main memory is allowed).
CACHE#	I 3V	**CACHEABLE:** Asserted by the CPU during a read cycle to indicate the CPU can perform a burst line fill. Asserted by the CPU during a write cycle to indicate that the CPU will perform a burst write-back cycle. If CACHE# is asserted to indicate cacheability, the TSC asserts KEN# either with the first BRDY#, or with NA#, if NA# is asserted before the first BRDY#.

Signal Name	Type	Description
KEN# /INV	O 3V	**CACHE ENABLE/INVALIDATE:** KEN# /INV functions as both the KEN# signal during CPU read cycles and the INV signal during first level cache snoop cycles. During CPU cycles, KEN# /INV is normally low. The TSC drives KEN# high during the first BRDY# or NA# assertion of a non-cacheable (in first level cache) CPU read cycle. The TSC drives INV high during the EADS# assertion of a PCI master DRAM write snoop cycle and low during the EADS# assertion of a PCI master DRAM read snoop cycle.
SMIACT#	I 3V	**SYSTEM MANAGEMENT INTERRUPT ACTIVE:** The CPU asserts SMIACT# when it is in system management mode as a result of an SMI. After SMM space (located at A0000h) is loaded and locked by BIOS, this signal must be sampled active with ADS# for the processor to access the SMM space of DRAM.

2.1.2 DRAM INTERFACE (TSC)

Signal Name	Type	Description
RAS[4:0]#	O 3V	**ROW ADDRESS STROBE:** These pins select the DRAM row.
CAS[7:0]#	O 3V	**COLUMN ADDRESS STROBE:** These pins always select which bytes are affected by a DRAM cycle.
MA[11:2]	O 3V	**MEMORY ADDRESS:** This is the row and column address for DRAM.
MAA[1:0]	O 3V	**MEMORY ADDRESS COPY A**: One copy of the MAs that change during a burst read or write of DRAM.
MAB[1:0]	O 3V	**MEMORY ADDRESS COPY B:** A second copy of the MAs that change during a burst read or write of DRAM.

2.1.3 SECONDARY CACHE INTERFACE (TSC)

Signal Name	Type	Description
CADV# / CAA4	O 3V	**CACHE ADVANCE/CACHE ADDRESS 4 (COPY A):** This pin has two modes of operation depending on the type of SRAMs selected via hardware strapping options or programming the CC Register. The CAA4 mode is used when the L2 cache consists of asynchronous SRAMs. CAA4 is used to sequence through the Qwords in a cache line during a burst operation. CADV# mode is used when the L2 cache consists of burst SRAMs. In this mode, assertion causes the burst SRAM in the L2 cache to advance to the next Qword in the cache line.
CADS# /CAA3	O 3V	**CACHE ADDRESS STROBE/CACHE ADDRESS 3 (COPY A):** This pin has two modes of operation depending on the type of SRAMs selected via hardware strapping options or programming the CC Register. The CAA3 mode is used when the L2 cache consists of asynchronous SRAMs. CAA3 is used to sequence through the Qwords in a cache line during a burst operation. CADS# mode is used when the L2 cache consists of burst SRAMs. In this mode assertion causes the burst SRAM in the L2 cache to load the BSRAM address register from the BSRAM address pins.
CAB3	O 3V	**CACHE ADDRESS 3 (COPY B):** CAB3 is used when the L2 cache consists of asynchronous SRAMs. CAB3 is used to sequence through the Qwords in a cache line during a burst operation
CCS# /CAB4	O 3V	**CACHE CHIP SELECT/CACHE ADDRESS (COPY B):** This pin has two modes of operation depending on the type of SRAMs selected via hardware strapping options or programming the CC Register. The CAB4 mode is used when the L2 cache consists of asynchronous SRAMs. CAB4 is used to sequence through the Qwords in a cache line during a burst operation. A L2 cache consisting of burst SRAMs will power up, if necessary, and perform an access if CCS# is asserted when CADS# is asserted. A L2 cache consisting of burst SRAMs will power down if CCS# is negated when CADS# is asserted. When CCS# is negated, a L2 cache consisting of burst SRAMs ignores ADS#. If CCS# is asserted when ADS# is asserted, a L2 cache consisting of burst SRAMs will power up, if necessary, and perform an access.
COE#	O 3V	**CACHE OUTPUT ENABLE**: The secondary cache data RAMs drive the CPU's data bus when COE# is asserted.
CWE[7:0]#	O 3V	**CACHE WRITE ENABLE:** Each CWE# corresponds to one byte lane. Assertion causes the byte lane to be written into the secondary cache data RAMs if they are powered up.
TIO[7:0]	I/O 5V	**TAG ADDRESS:** These are inputs during CPU accesses and outputs during L2 cache line fills and L2 cache line invalidates due to inquire cycles. TIO[7:0] contain the L2 tag address for 256-Kbyte L2 caches. TIO[6:0] contains the L2 tag address and TIO7 contains the L2 cache valid bit for 512-Kbyte caches.
TWE#	O 5V	**TAG WRITE ENABLE:** When asserted, new state and tag addresses are written into the external tag.

2.1.4 PCI INTERFACE (TSC)

Signal Name	Type	Description
AD[31:0]	I/O 5V	**ADDRESS DATA BUS:** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following clocks.
C/BE[3:0]#	I/O 5V	**COMMAND, BYTE ENABLE:** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	I/O 5V	**FRAME:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 5V	**DEVICE SELECT:** The TSC drvies DEVSEL# when a PCI initiator attempts to access main memory. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 5V	**INITIATOR READY:** Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 5V	**TARGET READY:** Asserted when the target is ready for a data transfer.
STOP#	I/O 5V	**STOP:** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 5V	**LOCK:** Used to establish, maintain, and release resource locks on PCI.
REQ[3:0]#	I 5V	**REQUEST:** PCI master requests for PCI.
GNT[3:0]#	O 5V	**GRANT:** Permission is given to the master to use PCI.
PHLD#	I 5V	**PCI HOLD**: This signal comes from the PIIX. PHLD# is the PIIX request for the PCI Bus. The TSC flushes the DRAM Write Buffers and acquires the host bus before granting PIIX via PHLDA#. This ensures that the guaranteed access time is met for ISA masters.
PHLDA#	O 5V	**PCI HOLD ACKNOWLEDGE:** This signal is driven by the TSC to grant PCI to the PIIX.
PAR	I/O 5V	**PARITY:** A single parity bit is provided over AD[31:0] and C/BE[3:0].
RST#	I 5V	**RESET:** When asserted, RST# resets the TSC and sets all register bits to the default value.

2.1.5 TDP INTERFACE (TSC)

Signal Name	Type	Description
PLINK[15:0]	I/O 3V	**PCI LINK:** These signals are connected to the PLINK data bus on the TDP. This is the data path between the TSC and TDP. Each TDP connects to one byte of the 16-bit bus.
MSTB#	O 3V	**MEMORY STROBE:** Assertion causes data to be posted in the DRAM Write Buffer.
MADV#	O 3V	**MEMORY ADVANCE:** For memory write cycles, assertion causes a Qword to be drained from the DRAM Write Buffer and the next data to be made available to the MD pins of the TDPs. For memory read cycles, assertion causes a Qword to be latched in the DRAM Input Register.
PCMD[1:0]	O 3V	**PLINK COMMAND:** This field controls how data is loaded into the PLINK input and output registers.
HOE#	O 3V	**HOST OUTPUT ENABLE:** This signal is used as the output enable for the Host Data Bus.
MOE#	O 3V	**MEMORY OUTPUT ENABLE:** This signal is used as the output enable for the memory data bus. A buffered copy of MOE# also serves as a WE# select for the DRAM array.
POE#	O 3V	**PLINK OUTPUT ENABLE:** This signal is used as the output enable for the PLINK Data Bus.

2.1.6 CLOCKS (TSC)

Signal Name	Type	Description
HCLKIN	I 5V	**HOST CLOCK IN:** This pin receives a buffered host clock. This clock is used by all of the TSC logic that is in the Host clock domain. This should be the same clock net that is delivered to the CPU. The net should tee and have equal lengths from the tee to the CPU and the TSC.
PCLKIN	I 5V	**PCI CLOCK IN:** This pin receives a buffered divide-by-2 host clock. This clock is used by all of the TSC logic that is in the PCI clock domain.

2.2 TDP Signals

2.2.1 DATA INTERFACE SIGNALS (TDP)

Signal Name	Type	Description
HD[31:0]	I/O 3V	**HOST DATA**: These signals are connected to the CPU data bus. The CPU data bus is interleaved between the two TDPs for every byte, effectively creating an even and an odd TDP.
MD[31:0]	I/O 3V/5V	**MEMORY DATA:** These signals are connected to the DRAM data bus. The DRAM data bus is interleaved between the two TDPs for every byte, effectively creating an even and an odd TDP.
PLINK[7:0]	I/O 3V	**PCI LINK:** These signals are connected to the PLINK data bus on the TSC. This is the data path between the TSC and TDP. Each TDP connects to one byte of the 16-bit bus.

2.2.2 TSC INTERFACE SIGNALS (TDP)

Signal Name	Type	Description
MSTB#	I 3V	**MEMORY STROBE:** Assertion causes data to be posted in the DRAM Write Buffer.
MADV#	I 3V	**MEMORY ADVANCE:** For memory write cycles, assertion causes a Qword to be flushed from the DRAM Write Buffer and the next data to be made available to the MD pins of the TDPs. For memory read cycles, assertion causes a Qword to be latched in the DRAM Input register.
PCMD[1:0]	I 3V	**PLINK COMMAND:** This field controls how data is loaded into the PLINK input and output registers.
HOE#	I 3V	**HOST OUTPUT ENABLE:** This signal is used as the output enable for the Host Data Bus.
MOE#	I 3V	**MEMORY OUTPUT ENABLE:** This signal is used as the output enable for the Memory Data Bus.
POE#	I 3V	**PLINK OUTPUT ENABLE:** This signal is used as the output enable for the PLINK Data Bus.

2.2.3 CLOCK SIGNAL (TDP)

Signal Name	Type	Description
HCLK	I 5V	**HOST CLOCK**: Primary clock input used to drive the part.

2.3 Signal State During Reset

Table 1 shows the state of all TSC and TDP output and bi-directional signals during a hard reset (RST# asserted). The TSC samples the strapping options on the A[31:28] signal lines on the rising edge of RST#. When RST# is asserted, the TSC enables the TDP outputs via the HOE#, MOE#, and POE# TSC/TDP interface signals. When RST# is negated, the TSC resets the TDP logic by driving HOE#, MOE#, and POE# inactive for two HCLKs.

Table 1. Output and I/O Signal States During Hard Reset

Signal	State
TSC	
A[31:28]	Input
A[27:3]	Low
BRDY#	High
NA#	High
AHOLD	High
EADS#	High
BOFF#	High
KEN#/INV	Low
RAS[4:0]#	Low
CAS[7:0]#	Low
MA[11:2]	Low
MAA[1:0]	Low
MAB[1:0]	Low
CADV#/CAA4	High
CADS#/CAA3	High

Signal	State
CCS#/CAB4	High
CAB3	High
COE#	High
CWE[7:0]#	High
TIO[7:0]#	Tri-state
TWE#	High
AD[31:0]	Low
C/BE[3:0]#	Low
FRAME#	Tri-state
DEVSEL#	Tri-state
IRDY#	Tri-state
TRDY#	Tri-state
STOP#	Tri-state
LOCK#	Tri-state
GNT[3:0]#	Tri-state
PHLDA#	Tri-state

Signal	State
PAR	Low
PLINK[15:0]	Low
MSTB#	High
MADV#	High
PCMD[1:0]	High
HOE#	High
MOE#	Low
POE#	Low
TDP	
HD[31:0]	Low
MD[31:1]	Low
MD0	NAND Tree Output
PLINK[7:0]	Low

3.0 REGISTER DESCRIPTION

The TSC contains two sets of software accessible registers (Control and Configuration registers), accessed via the Host CPU I/O address space. Control Registers control access to PCI configuration space. Configuration Registers reside in PCI configuration space and specify PCI configuration, DRAM configuration, cache configuration, operating parameters, and optional system features.

The TSC internal registers (both I/O Mapped and Configuration registers) are only accessible by the Host CPU and cannot be accessed by PCI masters. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFADD which can only be accessed as a Dword. All multi-byte numeric fields use ''little-endian'' ordering (i.e., lower addresses contain the least significant parts of the field). The following nomenclature is used for access attributes.

RO **Read Only**. If a register is read only, writes to this register have no effect.

R/W **Read/Write**. A register with this attribute can be read and written.

R/WC **Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Some of the TSC registers described in this section contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

In addition to reserved bits within a register, the TSC contains address locations in the PCI configuration space that are marked ''Reserved'' (Table 2). The TSC responds to accesses to these address locations by completing the Host cycle. Software should not write to reserved TSC configuration locations in the device-specific region (above address offset 3Fh).

During a hard reset (RST# asserted), the TSC sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, cache configuration, operating parameters and optional system features that are applicable, and to program the TSC registers accordingly.

3.1 Control Registers

The TSC contains two registers that reside in the CPU I/O address space—the Configuration Address (CONFADD) Register and the Configuration Data (CONFDATA) Register. These registers can not reside in PCI configuration space because of the special functions they perform. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.1.1 CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address: 0CF8h (Dword access only)
Default Value: 00000000h
Access: Read/Write

CONFADD is a 32-bit register accessed only when referenced as a Dword. A Byte or Word reference will ''pass through'' the Configuration Address Register to the PCI Bus. The CONFADD Register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CONE):** 1 = Enable; 0 = Disable.
30:24	**Reserved.**
23:16	**Bus Number (BUSNUM):** When BUSNUM is programmed to 00h, the target of the configuration cycle is either the TSC or the PCI Bus that is directly connected to the TSC, depending on the Device Number field. If the Bus Number is programmed to 00h and the TSC is not the target, a type 0 configuration cycle is generated on PCI. If the Bus Number is non-zero, a type 1 configuration cycle is generated on PCI with the Bus Number mapped to AD[23:16] during the address phase.
15:11	**Device Number (DEVNUM):** This field selects one agent on the PCI Bus selected by the Bus Number. During a Type 1 Configuration cycle, this field is mapped to AD[15:11]. During a Type 0 configuration cycle, this field is decoded and one of AD[31:11] is driven to 1. The TSC is always Device Number 0.
10:8	**Function Number (FUNCNUM):** This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The TSC responds to configuration cycles with a function number of 000b; all other function number values attempting access to the TSC (Device Number = 0, Bus Number = 0) generate a type 0 configuration cycle on the PCI Bus with no IDSEL asserted, which results in a master abort.
7:2	**Register Number (REGNUM):** This field selects one register within a particular bus, device, and function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	**Reserved.**

3.1.2 CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: CFCh
Default Value: 00000000h
Access: Read/Write

CONFDATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	**Configuration Data Window (CDW):** If bit 31 of CONFADD is 1, any I/O reference in the CONFDATA I/O space is mapped to configuration space using the contents of CONFADD.

3.2 PCI Configuration Registers

The PCI Bus defines a slot based ''configuration space'' that allows each device to contain up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported by the Pentium microprocessor, configuration space is not supported. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The TSC only supports Mechanism #1. Table 2 shows the TSC configuration space.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register, a Dword I/O write cycle is used to place a value into CONFADD that specifies the PCI Bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. Then, CONFDATA becomes a window onto four bytes of configuration space specified by the contents of CONFADD. Read/write accesses to CONFDATA generates a PCI configuration cycle to the address specified by CONFADD.

Type 0 Access

If the Bus Number field of CONFADD is 0, a type 0 configuration cycle is generated on PCI. CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The TSC is Device #0 and does not pass its configuration cycles to PCI. Thus, AD11 is never asserted. (For accesses to device #1, AD12 is asserted, etc., to Device #20 which asserts AD31.) Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which results in a master abort.

Type 1 Access

If the Bus Number field of CONFADD is non-zero, a type 1 configuration cycle is generated on PCI. CONFADD[23:2] are mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

Table 2. TSC Configuration Space

Address Offset	Symbol	Register Name	Access
00–01h	VID	Vendor Identification	RO
02–03h	DID	Device Identification	RO
04–05h	PCICMD	Command Register	R/W
06–07h	PCISTS	Status Register	RO, R/WC
08h	RID	Revision Identification	RO
09h		Reserved	
0Ah	SUBC	Sub-Class Code	RO
0Bh	BCC	Base Class Code	RO
0Ch		Reserved	
0Dh	MLT	Master Latency Timer	R/W
0Eh		Reserved	
0Fh	BIST	BIST Register	R/W
10–49h		Reserved	
50h	PCON	PCI Control Register	R/W
51h		Reserved	
52h	CC	Cache Control	R/W
53–56h		Reserved	
57h	DRAMC	DRAM Control	R/W
58h	DRAMT	DRAM Timing	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	R/W
60–64h	DRB[4:0]	DRAM Row Boundary (5 registers)	R/W
65–67h		Reserved	
68h	DRT	DRAM Row Type	R/W
69–71h		Reserved	
72h	SMRAM	System Management RAM Control	R/W
73–FFh		Reserved	

3.2.1 VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number**: This is a 16-bit value assigned to Intel.

3.2.2 DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h
Default Value: 122Dh
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number**. This is a 16-bit value assigned to the TSC.

3.2.3 PCICMD—PCI COMMAND REGISTER

Address Offset: 04–05h
Default: 06h
Access: Read/Write

This register controls the TSC's ability to respond to PCI cycles.

Bit	Descriptions
15:10	**Reserved.**
9	**Fast Back-to-Back: (Not Implemented)** This bit is hardwired to 0.
8	**SERR# Enable (SERRE): (Not Implemented)** This bit is hardwired to 0.
7	**Address/Data Stepping: (Not Implemented)** This bit is hardwired to 0.
6	**Parity Error Enable (PERRE): (Not Implemented)** This bit is hardwired to 0.
5:3	**Reserved:** These bits are hardwired to 0.
2	**Bus Master Enable (BME): (Not Implemented)** The TSC does not support disabling of its bus master capability on the PCI Bus. This bit is hardwired to 1.
1	**Memory Access Enable (MAE):** 1 = Enable PCI master access to main memory, if the PCI address selects enabled DRAM space; 0 = Disable (TSC does not respond to main memory accesses).
0	**I/O Access Enable (IOAE): (Not Implemented)** This bit is hardwired to 0. The TSC does not respond to PCI I/O cycles.

3.2.4 PCISTS—PCI STATUS REGISTER

Address Offset: 06–07h
Default Value: 0200h
Access: Read Only, Read/Write Clear

PCISTS reports the occurrence of a PCI master abort and PCI target abort. PCISTS also indicates the DEVSEL# timing that has been set by the TSC hardware.

Bit	Descriptions
15	**Detected Parity Error (DPE): (Not Implemented)** This bit is hardwired to 0.
14	**Signaled System Error (SSE)R/WC:** This bit is hardwired to 0.
13	**Received Master Abort Status (RMAS)—R/WC:** When the TSC terminates a Host-to-PCI transaction (TSC is a PCI master) with an unexpected master abort, this bit is set to 1. **NOTE:** Master abort is the normal and expected termination of PCI special cycles. Software sets this bit to 0 by writing 1 to it.
12	**Received Target Abort Status (RTAS)—R/WC:** When a TSC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. Software sets RTAS to 0 by writing 1 to it.
11	**Signaled Target Abort Status (STAS):** This bit is hardwired to 0. The TSC never terminates a PCI cycle with a target abort.
10:9	**DEVSEL# Timing (DEVT)—RO:** This 2-bit field indicates the timing of the DEVSEL# signal when the TSC responds as a target, and is hard-wired to the value 01b (medium) to indicate the slowest time that DEVSEL# is generated.
8	**Data Parity Detected (DPD)—R/WC:** This bit is hardwired to 0
7	**Fast Back-to-Back (FB2B): (Not Implemented)** This bit is hardwired to 0.
6:0	**Reserved.**

3.2.5 RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: See stepping information document
Access: Read Only

This register contains the revision number of the TSC.

Bit	Description
7:0	**Revision Identification Number:** This is an 8-bit value that indicates the revision identification number for the TSC.

3.2.6 SUBC—SUB-CLASS CODE REGISTER

Address Offset: 0Ah
Default Value: 00h
Access: Read Only

This register indicates the function sub-class in relation to the Base Class Code.

Bit	Description
7:0	**Sub-Class Code (SUBC)**: 00h = Host bridge.

3.2.7 BCC—BASE CLASS CODE REGISTER

Address Offset: 0Bh
Default Value: 06h
Access: Read Only

This register contains the Base Class Code of the TSC.

Bit	Description
7:0	**Base Class Code (BASEC):** 06h = Bridge device.

3.2.8 MLT—MASTER LATENCY TIMER REGISTER

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write

MLT is an 8-bit register that controls the amount of time the TSC, as a bus master, can burst data on the PCI Bus. The Count Value is an 8-bit quantity. However, MLT[2:0] are hardwired to 0. MLT is also used to guarantee the host CPU a minimum amount of the system resources as described in the PCI Bus Arbitration section.

Bit	Description
7:3	**Master Latency Timer Count Value:** The number of clocks programmed in the MLT represents the minimum guaranteed time slice (measured in PCI clocks) allotted to the TSC, after which it must surrender the bus as soon as other PCI masters are granted the bus. The default value of MLT is 00h or 0 PCI clocks. The MLT should always be programmed to a non-zero value.
2:0	**Reserved:** Hardwired to 0.

3.2.9 BIST—BIST REGISTER

Address Offset: 0Fh
Default: 00h
Access: Read/Write

The Built In Self Test (BIST) function is not supported by the TSC. Writes to this register have no affect.

Bit	Descriptions
7	**BIST Supported—RO:** 00h = Disable BIST function.
6	**Start BIST:** This function is not supported and writes have no affect.
5:4	**Reserved.**
3:0	**Completion Code—RO:** This field always returns 0 when read and writes have no affect.

3.2.10 PCON—PCI CONTROL REGISTER

Address Offset: 50h
Default: 00h
Access: Read/Write

The PCON Register enables and disables features related to the PCI unit operation not already covered in the PCI required configuration space.

Bit	Descriptions
7:5	**CPU Inactivity Timer Bits:** This field selects the value used in the CPU Inactivity Timer. This timer counts CPU inactivity in PCI clocks. The inactivity window is defined as the last BRDY# to the next ADS#. When active, the CPU is default owner of the PCI Bus. If the CPU is inactive, PHOLD and the REQx# lines are given priority. **Bits[7:5] PCI Clocks** 000 1 001 2 010 3* 011 4 100 5* 101 6 110 7 111 8 * Recommended settings
4	**Reserved.**
3	**Peer Concurrency Enable Bit (PCE):** 1 = Peer Concurrency enabled. 0 = Peer Concurrency disabled. This bit is normally programmed to 1.
2	**CPU-to-PCI Write Bursting Disable Bit:** 0 = CPU-to-PCI Write bursting enabled. 1 = CPU-to-PCI Write bursting disabled.
1	**PCI Streaming Bit:** 0 = PCI streaming enabled. 1 = PCI streaming disabled.
0	**Bus Concurrency Disable Bit:** 0 = Bus concurrency enabled. 1 = Bus concurrency disabled.

3.2.11 CC—CACHE CONTROL REGISTER

Address Offset: 52h
Default: SSSS0010 (S = Strapping option)
Access: Read/Write

The CC Register selects the secondary cache operations. This register enables/disables the L2 cache, adjusts cache size, defines the cache SRAM type, and controls tag initialization. After a hard reset, CC[7:4] reflect the inverted signal levels on the host address lines A[31:28].

Bit	Description
7:6	**Secondary Cache Size (SCS):** This field reflects the inverted signal level on the A[31:30] pins at the rising edge of the RESET signal (default). The default values can be overwritten with subsequent writes to the CC Register. The options for this field are: **Bits[7:6] — Secondary Cache Size** 0 0 — Cache not populated 0 1 — 256 Kbytes 1 0 — 512 Kbytes 1 1 — Reserved **NOTE:** 1. When SCS = 00, the L2 cache is disabled and the cache tag state is frozen. 2. To enable the L2 cache, SCS must be non-zero and the FLCE bit must be 1.
5:4	**SRAM Type (SRAMT):** This field reflects the inverted signal level on the A[29:28] pins at the rising edge of the RESET signal (default). The default values can be overwritten with subsequent writes to the CC Register. The options for this field are: **Bits[5:4] — SRAM Type** 0 0 — Pipelined Burst 0 1 — Burst 1 0 — Asynchronous 1 1 — Pipelined Burst for 512K/Dual-bank inplementations. Selects 3-1-1-1-2-1-1-1 instead of 3-1-1-1-1-1-1-1 back-to-back burst timings with NA# enabled. An extra clock is inserted for bank turnaround. SCS must be set to 10.
3	**NA# Disable Bit:** 0 = NA# will be asserted as appropriate by the TSC (default). 1 = TCS's NA# signal is never asserted. This bit should be configured as desired before either the L1 or L2 caches are enabled. The NA# signal can be connected or disconnected from the processor as long as the NA# Disable bit is set to 1. Default is not set.
2	**Reserved.**
1	**Secondary Cache Force Miss or Invalidate (SCFMI):** When SCFMI = 1, the L2 hit/miss detection is disabled, and all tag lookups result in a miss. If the L2 is enabled, the cycle is processed as a miss. If the L2 is populated but disabled (FLCE = 0) and SCFMI = 1, any CPU read cycle invalidates the selected tag entry. When SCFMI = 0, normal L2 cache hit/miss detection and cycle processing occurs. Software can flush the cache (cause all modified lines to be written back to main memory) by setting SCFMI to 1 with the L2 cache enabled (SCS ≠ 00 and FLCE = 1), and reading all L2 cache tag address locations.

Bit	Description
0	**First Level Cache Enable (FLCE):** FLCE enables/disables the first level cache. When FLCE = 1, the TSC responds to CPU cycles with KEN# asserted for cacheable memory cycles. When FLCE = 0, KEN# is always negated and line fills to either the first level or L2 cache are prevented. Note that, when FLCE = 1 and SCFMI = 1, writes to the cache are also forced as misses. Thus, it is possible to create incoherent data between main memory and the L2 cache. A summary of FLCE/SCFMI bit interactions is as follows: **FLCE SCFMI L2 Cache Result** 0 0 Disabled 0 1 Disabled; tag invalidate on reads 1 0 Normal L2 cache operation (dependent on SCS) 1 1 Enabled; miss forced on reads/writes

3.2.12 DRAMC—DRAM CONTROL REGISTER

Address Offset: 57h
Default Value: 01h
Access: Read/Write

This 8-bit register controls main memory DRAM operating modes and features.

Bit	Description
7:6	**Hole Enable (HEN):** This field enables a memory hole in main memory space. CPU cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole are ignored by the TSC (no DEVSEL#). Note that a selected hole is not remapped. Note that this field should not be changed while the L2 cache is enabled. **Bits[7:6] Hole Enabled** 00 None 01 512 Kbytes –640 Kbytes 10 15 Mbytes –16 Mbytes 11 Reserved
5:4	**Reserved.**
3	**EDO Detect Mode Enable (EDME):** This bit, if set to 1, enables a special timing mode for BIOS to detect EDO DRAM type on a bank-by-bank basis. Once all DRAM row banks have been tested for EDO, the EDME bit should be set to 0. Otherwise, performance will be seriously impacted. An algorithm for using the EDME bit 3 follows the table.
2:0	**DRAM Refresh Rate (DRR):** The DRAM refresh rate is adjusted according to the frequency selected by this field. Note that refresh is also disabled via this field, and that disabling refresh results in the eventual loss of DRAM data. **Bits[2:0] Host Bus Frequency** 000 Refresh Disabled 001 50 MHz 010 60 MHz 011 66 MHz 1XX Reserved

DRAM Type Detection

The EDO Detect Mode Enable field (bit 3) provides a special timing mode that allows BIOS to determine the DRAM type in each of the banks of main memory DRAM. To exploit the performance improvements from EDO DRAMs, the BIOS should provide for dynamic detection of any EDO DRAMs in the DRAM rows.

3.2.13 DRAMT—DRAM TIMING REGISTER

Address Offset: 58h
Default Value: 00h
Access: Read/Write

This 8-bit register controls main memory DRAM timings. While most system designs will be able to use one of the faster burst mode timings, slower rates may be required in certain system designs to support layouts with longer trace lengths or slower DRAMs.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7</td><td>Reserved.</td></tr>
<tr><td>6:5</td><td>DRAM Read Burst Timing (DRBT): The DRAM read burst timings are controlled by the DRBT field. The timing used depends on the type of DRAM on a per-bank basis, as indicated by the DRT register.

<table>
<tr><th>DRBT</th><th>EDO Burst Rate</th><th>Standard Page Mode Rate</th></tr>
<tr><td>00</td><td>x444</td><td>x444</td></tr>
<tr><td>01</td><td>x333</td><td>x444</td></tr>
<tr><td>10</td><td>x222</td><td>x333</td></tr>
<tr><td>11</td><td>Reserved</td><td>Reserved</td></tr>
</table>
This field is typically set to ‘‘01’’ or ‘‘10’’ depending on the system configuration.</td></tr>
<tr><td>4:3</td><td>DRAM Write Burst Timing (DWBT): The DRAM write burst timings are controlled by the DWBT field. Slower rates may be required in certain system designs to support layouts with longer trace lengths or slower DRAMs. Most system designs will be able to use one of the faster burst mode timings.

<table>
<tr><th>DWBT</th><th>Standard Page Mode Rate</th></tr>
<tr><td>00</td><td>x444</td></tr>
<tr><td>01</td><td>x333</td></tr>
<tr><td>10</td><td>x222 (see notes 1 and 2)</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
NOTES:
1. Minimum 3-Clock CAS# Cycle Time for Single Writes. The DWBT field controls the minimum CAS# cycle time for single and burst write cycles, except for the x222 programming case in which the minimum cycle time for single writes is limited to 3-clocks.
2. Two clock writes should not be programmed at 66 MHz.</td></tr>
<tr><td>2</td><td>RAS to CAS Delay (RCD): RCD controls the DRAM page miss and row miss leadoff timings. When RCD = 1, the RAS active to CAS active delay is 2 clocks. When RCD = 0, the timing is 3 clocks. Note that RCD timing adjustments are independent to DLT timing adjustments.

<table>
<tr><th>RCD</th><th>RAS to CAS Delay</th></tr>
<tr><td>0</td><td>3</td></tr>
<tr><td>1</td><td>2</td></tr>
</table></td></tr>
</table>

Bit	Description
1:0	**DRAM Leadoff Timing (DLT):** The DRAM leadoff timings for page/row miss cycles are controlled by the DLT bits. DLT controls the MA setup to the first CAS# assertion. The DLT bits do not effect page hit cycles.

DLT	Read Leadoff	Write Leadoff	RAS# Precharge
00	8	6	3
01	7	5	3
10	8	6	4
11	7	5	4

Note that the DLT field and RCD bit have cumulative affects (i.e., setting DLT0 = 0 and RCD = 0 results in two additional clocks betwwen RAS# assertion and CAS# assertion).

3.2.14 PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0])

Address Offset: PAM0 (59h)—PAM6 (5Fh)

Default Value: 00h

Attribute: Read/Write

The TSC allows programmable memory and cacheability attributes on 14 memory segments of various sizes in the 640-Kbyte to 1-Mbyte address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Three bits are used to specify L1 cacheability and memory attributes for each memory segment. These attributes are:

RE **Read Enable**. When RE = 1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE = 0, the CPU read accesses are directed to PCI.

WE **Write Enable**. When WE = 1, the CPU write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE = 0, the CPU write accesses are directed to PCI.

CE **Cache Enable**. When CE = 1, the corresponding memory segment is L1 cacheable. CE must not be set to 1 when RE = 0 for any particular memory segment. When CE = 1 and WE = 0, the corresponding memory segment is cached in the first level cache only on CPU code read cycles.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled (Table 3.). For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Table 3. Attribute Definition

Read/Write Attribute	Definition
Read Only	**Read cycles:** CPU cycles are serviced by the main memory or second level cache in a normal manner. **Write cycles:** CPU initiated write cycles are ignored by the DRAM interface as well as the second level cache. Instead, the cycles are passed to PCI for termination. Areas marked as read only are L1 cacheable for code accesses only. These regions are not cached in the second level cache.
Write Only	**Read cycles:** All read cycles are ignored by main memory as well as the second level cache. CPU-initiated read cycles are passed onto PCI for termination. The write only state can be used while copying the contents of a ROM, accessible on PCI, to main memory for shadowing, as in the case of BIOS shadowing. **Write cycles**: CPU write cycles are serviced by main memory and L2 cache in a normal manner.
Read/Write	This is the normal operating mode of main memory. Both read and write cycles from the CPU and PCI are serviced by main memory and L2 cache interface.
Disabled	All read and write cycles to this area are ignored by the main memory and cache interface. These cycles are forwarded to PCI for termination.

Each PAM Register controls two regions, typically 16-Kbyte in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 4.

PCI master access to main memory space is also controlled by the PAM Registers. If the PAM programming indicates a region is writeable, then PCI master writes are accepted (DEVSEL# generated). If the PAM programming indicates a region is readable, PCI master reads are accepted. If a PCI write to a non-writeable main memory region or a PCI read of a non-readable main memory region occurs, the TSC does not accept the cycle (DEVSEL# is not asserted). PCI master accesses to enabled memory hole regions are not accepted by the TSC.

Table 4. Attribute Bit Assignment

Bits [7,3] Reserved	Bits [6,2] Cache Enable	Bits [5,1] Write Enable	Bits [4,0] Read Enable	Description
x	x	0	0	Main memory disabled; accesses directed to PCI
x	0	0	1	Read only; main memory write protected; non-cacheable. Read-modify-write cycles to this space is not supported.
x	1	0	1	Read only; main memory write protected; L1 cacheable for code accesses only
x	0	1	0	Write only
x	0	1	1	Read/write; non-cacheable
x	1	1	1	Read/write; cacheable

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process, BIOS can be shadowed in main memory to increase the system performance. To shadow BIOS, the attributes for that address range should be set to write only. BIOS is shadowed by first performing a read of that address. This read is forwarded to the expansion bus. The CPU then performs a write of the same address, which is directed to main memory. After BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

Table 5. PAM Registers and Associated Memory Segments

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	**Reserved**						59h
PAM0[7:4]	R	CE	WE	RE	0F0000–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	CE	WE	RE	0C0000–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	CE	WE	RE	0C4000–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	CE	WE	RE	0C8000–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	CE	WE	RE	0CC000–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	CE	WE	RE	0D0000–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	CE	WE	RE	0D4000–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	CE	WE	RE	0D8000–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	CE	WE	RE	0DC000–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	CE	WE	RE	0E0000–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	CE	WE	RE	0E4000–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	CE	WE	RE	0E8000–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	CE	WE	RE	0EC000–0EFFFFh	BIOS Extension	5Fh

NOTE:
The CE bit should not be changed while the L2 cache is enabled.

DOS Application Area (00000–9FFFh)

Read, write, and cacheability attributes are always enabled and are not programmable for the 0–640-Kbyte DOS application region.

Video Buffer Area (A0000–BFFFFh)

This 128-Kbyte area is not controlled by attribute bits. CPU-initiated cycles in this region are always forwarded to PCI for termination. This area is not cacheable. See section 3.2.16 for details on the use of this range as SMRAM.

Expansion Area (C0000–DFFFFh)

This 128-Kbyte area is divided into eight 16-Kbyte segments. Each segment can be assigned one of four read/write states: read-only, write-only, read/write, or disabled memory that is disabled is not remapped. Cacheability status can also be specified for each segment.

Extended System BIOS Area (E0000–EFFFFh)

This 64-Kbyte area is divided into four 16-Kbyte segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000–FFFFFh)

This area is a single 64-Kbyte segment. This segment can be assigned cacheability, read, and write attributes. When disabled, this segment is not remapped.

Extended Memory Area (100000–FFFFFFFFh)

The extended memory area can be split into several parts;

- Flash BIOS area from 4 Gbyte to 4 Gbyte - 512 Kbyte (aliased on ISA at 16 Mbyte - 15.5 Mbyte)
- Main Memory from 1 Mbyte to a maximum of 128 Mbytes
- PCI Memory space from the top of main memory to 4 Gbyte - 512 Kbyte

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 Gbyte to 4 Gbyte - 512 Kbyte. This area is physically mapped on the expansion bus. Since these addresses are in the upper 4 Gbyte range, the request is directed to PCI.

The main memory space can occupy extended memory from a minimum of 1 Mbyte up to 128 Mbytes. This memory is cacheable.

PCI memory space from the top of main memory to 4Gbytes is always non-cacheable.

3.2.15 DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset: 60h(DRB0)—64h(DRB4)

Default Value: 02h

Access: Read/Write

The TSC supports 5 rows of DRAM. Each row is 64 bits wide. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 4-Mbyte granularity. Note that bit 0 of each DRB must always be programmed to 0 for proper operation.

DRB0 = Total amount of memory in row 0 (in 4 Mbytes)
DRB1 = Total amount of memory in row 0 + row 1 (in 4 Mbytes)
DRB2 = Total amount of memory in row 0 + row 1 + row 2 (in 4 Mbytes)
DRB3 = Total amount of memory in row 0 + row 1 + row 2 + row 3 (in 4 Mbytes)
DRB4 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row4 (in 4 Mbytes)

The DRAM array can be configured with 512Kx32, 1Mx32, 2Mx32, and 4Mx32 SIMMs. Each register defines an address range that causes a particular RAS# line to be asserted (e.g., if the first DRAM row is 8 Mbytes in size then accesses within the 0 to 8-Mbyte range causes RAS0# to be asserted).

Bit	Description
7:6	**Reserved.**
5:0	**Row Boundary Address:** This 6-bit field is compared against address lines A[27:22] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB = row size).

Row Boundary Address

These 6-bit values represent the upper address limits of the 5 rows (i.e., this row minus previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). DRB4 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB4. If DRB4 is greater than 128 Mbytes, then 128 Mbytes of DRAM are available.

As an example of a general purpose configuration where 4 physical rows are configured for either single-sided or double-sided SIMMs, the memory array would be configured like the one shown Figure 2. In this configuration, the TSC drives two RAS# signals directly to the SIMM rows. If single-sided SIMMs are populated, the even RAS# signal is used and the odd RAS# is not connected. If double-sided SIMMs are used, both RAS# signals are used.

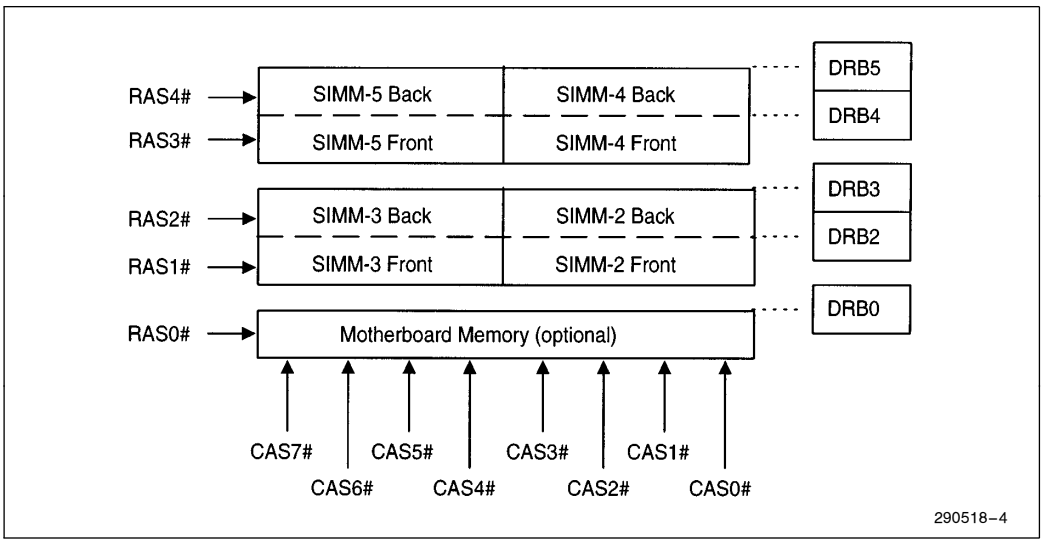


Figure 2. SIMMs and Corresponding DRB Registers

The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of four 8-byte or eight 4-byte SIMM sockets.

Example #1

The memory array is populated with four single-sided 1MB x 32 SIMMs, a total of 16 Mbytes of DRAM. Two SIMMs are required for each populated row making each populated row 8 Mbytes in size.

DRB0 = 02h populated (2 SIMMs, 8 Mbyte this row)

DRB1 = 04h populated (2 SIMMs, 8 Mbyte this row)

DRB2 = 04h empty row

DRB3 = 04h empty row

DRB4 = 04h empty row

Example #2

The memory array is populated with two 2-Mbyte x 32 double-sided SIMMs (one row), and four 4-Mbyte x 32 single-sided SIMMs (two rows), yielding a total of 96 Mbytes of DRAM. The DRB Registers are programmed as follows:

DRB0 = 04h populated with 16 Mbytes, ½ of double-sided SIMMs

DRB1 = 08h the other 16 Mbytes of the double-sided SIMMs

DRB2 = 10h populated with 32 Mbytes, one of the sided SIMMs

DRB3 = 18h the other 32 Mbytes of single-sided SIMMs

DRB4 = 18h empty row

3.2.16 DRT—DRAM ROW TYPE REGISTER

Address Offset: 68h

Default Value: 00h

Access: Read/Write

This 8-bit register identifies the type of DRAM (EDO or page mode) used in each row, and should be programmed by BIOS for optimum performance if EDO DRAMs are used. The TSC uses these bits to determine the correct cycle timing on DRAM cycles.

Bit	Description
7:5	**Reserved.**
4:0	**DRAM Row Type (DRT[4:0]):** Each bit in this field corresponds to the DRAM row identified by the corresponding DRB Register. Thus, DRT0 corresponds to row 0, DRT1 to row 1, etc. When DRTx = 0, page mode DRAM timings are used for that bank. When DRTx = 1, EDO DRAM timings are used for that bank.

3.2.17 SMRAM—SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 72h
Default Value: 02h
Access: Read/Write

The System Management RAM Control Register controls how accesses to this space are treated. The Open, Close, and Lock SMRAM Space bits function only when the SMRAM enable bit is set to 1. Also, the OPEN bit (DOPEN) should be set to 0 before the LOCK bit (DLCK) is set to 1.

Bit	Description
7	**Reserved.**
6	**SMM Space Open (DOPEN):** When DOPEN = 1 and DLCK = 0, SMM space DRAM is made visible, even when SMIACT# is negated. This is intended to help BIOS initialize SMM space. Software should ensure that DOPEN = 1 is mutually exclusive with DCLS = 1. When DLCK is set to 1, DOPEN is set to 0 and becomes read only.
5	**SMM Space Closed (DCLS):** When DCLS = 1, SMM space DRAM is not accessible to data references, even if SMIACT# is asserted. Code references may still access SMM space DRAM. This allows SMM software to reference ''through'' SMM space to update the display, even when SMM space is mapped over the VGA range. Software should ensure that DOPEN = 1 is mutually exclusive with DCLS = 1.
4	**SMM Space Locked (DLCK):** When DLCK is set to 1, the TSC sets DOPEN to 0 and both DLCK and DOPEN become read only. DLCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of DLCK and DOPEN provide convenience with security. The BIOS can use the DOPEN function to initialize SMM space and then use DLCK to ''lock down'' SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the DOPEN function.
3	**SMRAM Enable (SMRAME):** When SMRAME = 1, the SMRAM function is enabled, providing 128 Kbytes of DRAM accessible at the A0000h address while in SMM (ADS# with SMIACT#).
2:0	**SMM Space Base Segment (DBASESEG):** This field selects the location of SMM space. ''SMM DRAM'' is not remapped. It is simply ''made visible'' if the conditions are right to access SMM space. Otherwise, the access is forwarded to PCI. DBASESEG = 010 is the only allowable setting and selects the SMM space as A0000–BFFFFh. All other values are reserved. PCI masters are not allowed access to SMM space.

Table 6 summarizes the operation of SMRAM space cycles targeting SMI space addresses (A and B segments):

Table 6. SMRAM Space Cycles

SMRAME	DLCK	DCLS	DOPEN	SMIACT#	Code Fetch	Data Reference
0	X	X	X	X	PCI	PCI
1	0	0	0	0	DRAM	DRAM
1	0	X	0	1	PCI	PCI
1	0	0	1	X	DRAM	DRAM
1	0	1	0	0	DRAM	PCI
1	0	1	1	X	INVALID	INVALID
1	1	0	X	0	DRAM	DRAM
1	1	X	X	1	PCI	PCI
1	1	1	X	0	DRAM	PCI

4.0 FUNCTIONAL DESCRIPTION

This section provides a functional description of the TSC and TDP.

4.1 Host Interface

The Host Interface of the TSC is designed to support the Pentium processor. The host interface of the TSC supports 50 MHz, 60 MHz, and 66 MHz bus speeds. The 82430FX PCIset supports the Pentium processor with a full 64-bit data bus, 32-bit address bus, and associated internal write-back cache logic. Host bus addresses are decoded by the TSC for accesses to main memory, PCI memory, and PCI I/O. The TSC also supports the pipelined addressing capability of the Pentium processor.

4.2 PCI Interface

The 82437FX integrates a high performance interface to the PCI local bus taking full advantage of the high bandwidth and low latency of PCI. Five PCI masters are supported by the integrated arbiter including a PCI-to-ISA bridge and four general PCI masters. The TSC acts as a PCI master for CPU accesses to PCI. The PCI Bus is clocked at one half the frequency of the CPU clock. This divided synchronous interface minimizes latency for CPU-to-PCI cycles and PCI-to-main memory cycles.

The TSC/TDPs integrate posted write buffers for CPU memory writes to PCI. Back-to-back sequential memory writes to PCI are converted to burst writes on PCI. This feature allows the CPU to continue posting dword writes at the maximum bandwidth for the Pentium processor for the highest possible transfer rates to the graphics frame buffer.

Read prefetch and write posting buffers in the TSC/TDPs enable PCI masters to access main memory at up to 120 MB/second. The TSC incorporates a snoop-ahead feature which allows PCI masters to continue bursting on both reads and writes even as the bursts cross cache line boundaries.

4.3 Secondary Cache Interface

The TSC integrates a high performance second level cache controller using internal/external tags and provides a full first level and second level cache coherency mechanism. The second level cache is direct mapped, non-sectored, and supports a write-back cache policy. Cache lines are allocated on read misses (no write allocate).

The second level cache can be configured for either 256-Kbyte or 512-Kbyte cache sizes using either synchronous burst or pipelined burst SRAMs, or standard asynchronous SRAMs. For the 256-Kbyte configurations, an 8kx8 standard SRAM is used to store the tags. For the 512-Kbyte configurations, a 16kx8 standard SRAM is used to store the tags and the valid bits. A 5V SRAM is used for the Tag.

A second level cache line is 32 bytes wide. In the 256-Kbyte configurations, the second level cache contains 8K lines, while the 512-Kbyte configurations contain 16K lines. Valid and modified status bits are kept on a per-line basis. Cacheability of the entire memory space in the first level cache is supported. For the second level cache, only the lower 64 Mbytes of main memory are cacheable (only main memory controlled by the TSC DRAM interface is cached). PCI memory is not cached. Table 7 shows the different standard SRAM access time requirements for different host clock frequencies.

Table 7. SRAM Access Time Requirements

Host Clock Frequency (MHz)	Standard SRAM Access Time (ns)	Burst SRAM Clock-to-Output Access Time (ns)	Standard	Burst
			Tag RAM Access Time (ns)	Tag RAM Access Time (ns)
50	20 (17 ns Buffer)	13.5	30	20
60	17 (10 ns Buffer)	10	20	15
66	15 (7 ns Buffer)	8.5	15	15

4.3.1 CLOCK LATENCIES

Table 8 and Table 9 list the latencies for various processor transfers to and from the second level cache for standard and burst SRAM. The clock counts are identical for pipelined and non-pipelined burst SRAM.

Table 8. Second Level Cache Latencies with Standard SRAM

Cycle Type	HCLK Count
Burst Read	3-2-2-2
Burst Write (Write Back)	4-3-3-3
Single Read	3
Single Write	4

Table 9. Second Level Cache Latencies with Burst SRAM

Cycle Type	HCLK Count
Burst Read	3-1-1-1
Burst Write (Write Back)	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads	3-1-1-1, 1-1-1-1

4.3.2 SNOOP CYCLES

Snoop cycles are used to maintain coherency between the caches (first and second level) and main memory. The TSC generates a snoop (or inquire) cycle to probe the first level and second level caches when a PCI master attempts to access main memory. Snoop cycles are performed by driving the PCI master address onto the host address bus and asserting EADS#.

To maintain optimum PCI bandwidth to main memory, the TSC utilizes a ''snoop ahead'' algorithm. Once the snoop for the first cache line of a transfer has completed, the TSC automatically snoops the next sequential cache line. This algorithm enables the TSC to continue burst transfers across cache line boundaries.

Reads

If the snoop cycle generates a first level cache hit to a modified line, the line in the first level cache is written back to main memory (via the DRAM Posted Write Buffers). The line in the second level cache (if it exists) is invalidated. Note that the line in the first level cache is not invalidated if the INV pin on the CPU is tied to the KEN# signal from the TSC. The TSC drives KEN#/INV low with EADS# assertion during PCI master read cycles.

At the same time as the first level snoop cycle, the TSC performs a tag look-up to determine whether the addressed memory is in the second level cache. If the snoop cycle generates a second level cache hit to a modified line and there was not a hit in the first level cache (HITM# not asserted), the second level cache line is written back to main memory (via the DRAM Posted Write Buffers) and changed to the ''clean'' state. The PCI master read completes after the data has been written back to main memory.

Writes

PCI Master write cycles never result in a write directly into the second level cache. A snoop hit to a modified line in either the first or second caches results in a write-back of that line to main memory. If both the first and second level caches have modified lines, the line is written back from the first level cache. In all cases, lines in the first and second level caches are invalidated and the PCI write to main memory occurs after the writeback completes. A PCI master write snoop hit to an unmodified line in either the first or second level caches results in the line being invalidated. The TSC drives KEN#/INV with EADS# assertion during PCI master write cycles.

4.3.3 CACHE ORGANIZATION

Figure 3, Figure 4, Figure 5, Figure 6, and Figure 7 show the connections between the TSC and the external tag RAM and data SRAM. A 512K standard SRAM cache is implemented with 64Kx8 data SRAMs and a 16Kx8 tag RAM. The second ADS# pin from the CPU should be used to drive the ADSP# pin on Burst or Pipelined Burst SRAMs.

4.3.4 Clarification On How to Flush the L2 Cache

The SCFMI (Force Miss/Invalidate) mode is intended to allow flushing of dirty L2 lines back to memory. Since the flushed dirty line is posted to the DRAM write buffer in parallel with the linefill, the new line (which is filled to both L1 and L2) is guaranteed to be stale data.

The implication of the actual operation is that any program that is attempting to flush the L2 must not be run from the L2 itself, unless the L2 code image is coherent with DRAM. For example, if a DOS program to flush the L2 is loaded, it is loaded from disk using a string move. The MOVS may result in loading the program partially into L2, since the memory writes will (likely) hit previously valid lines in the L2. When the flush program sets the SCFMI bit to force misses, subsequent code fetches may be serviced from L2 which contain the stale code image.

An important aspect to consider when flushing L2 is to ensure that the code being used to flush the cache is not in the current 256K page (256K L2 being used here) residing in L2. The BIOS algorithm will also work if it is executed from non-cacheable or write-protected DRAM space (e.g., BIOS region). If this can't be guaranteed, then an alternate software flush algorthm is to read 2X the size of the L2. Note that this implies a protected-mode code for the 512K L2 case.

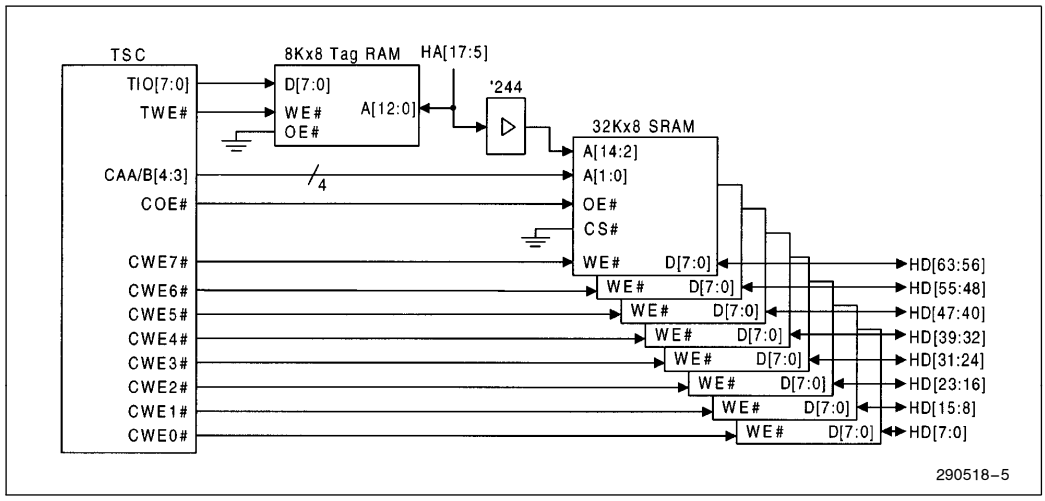


Figure 3. 256-Kbyte Second Level Cache (Standard SRAM)

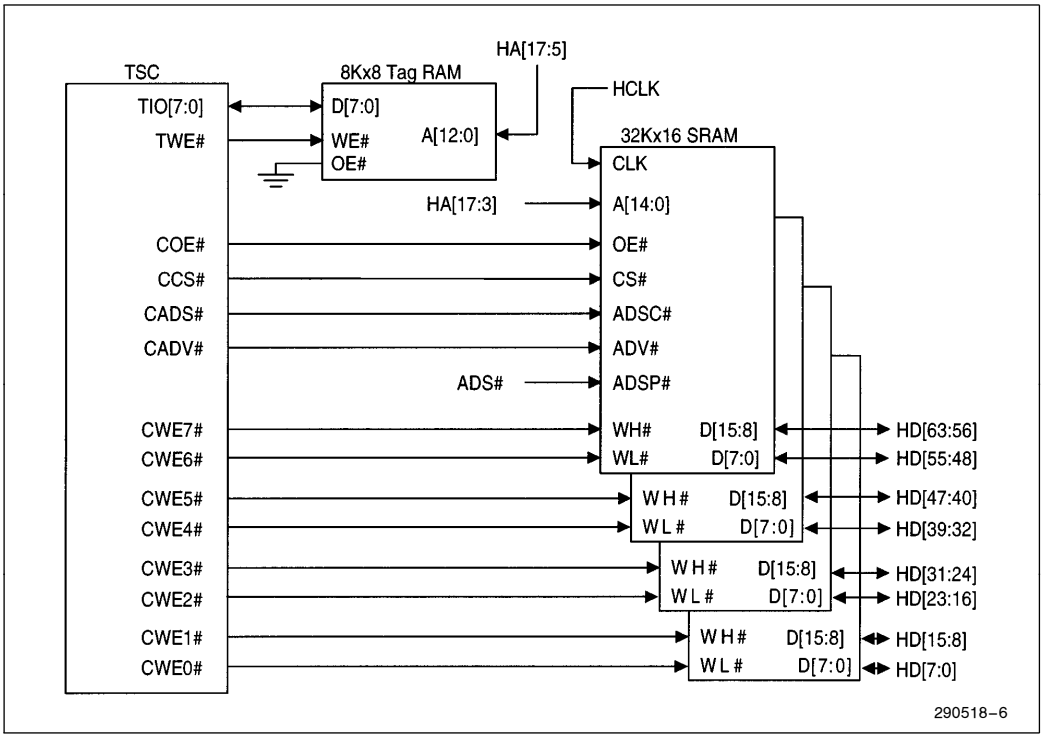


Figure 4. 256-Kbyte Second Level Cache (Burst SRAM)

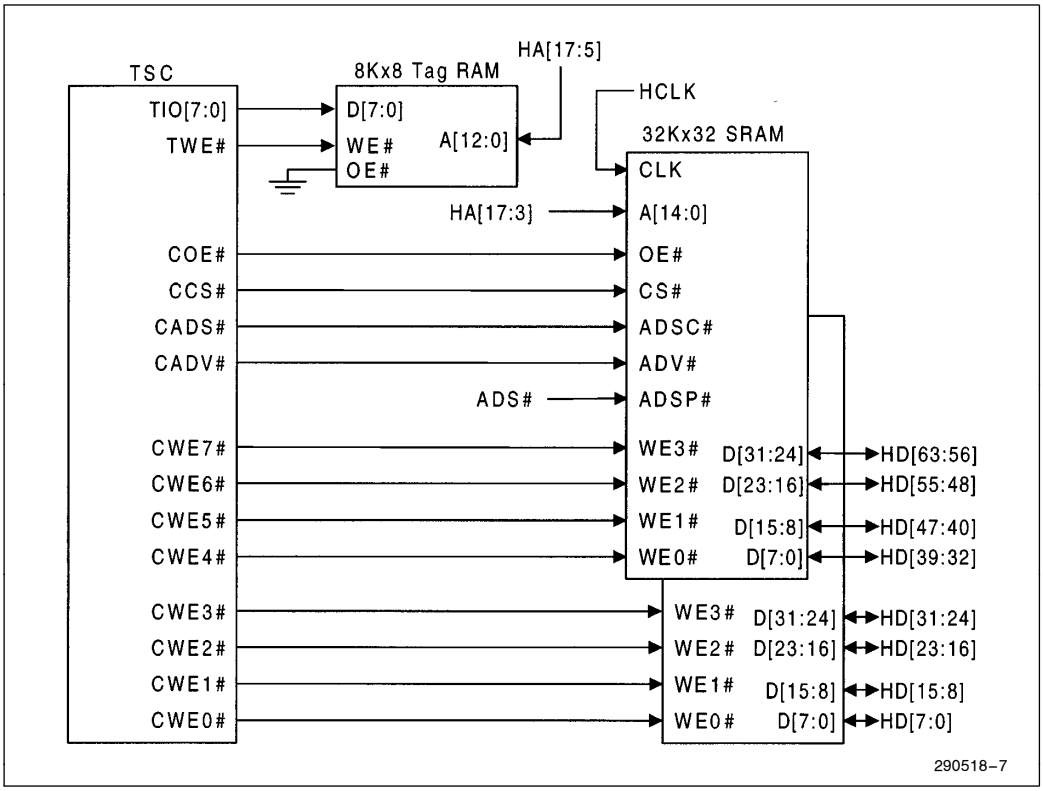


Figure 5. 256-Kbyte Second Level Cache (Burst SRAM)

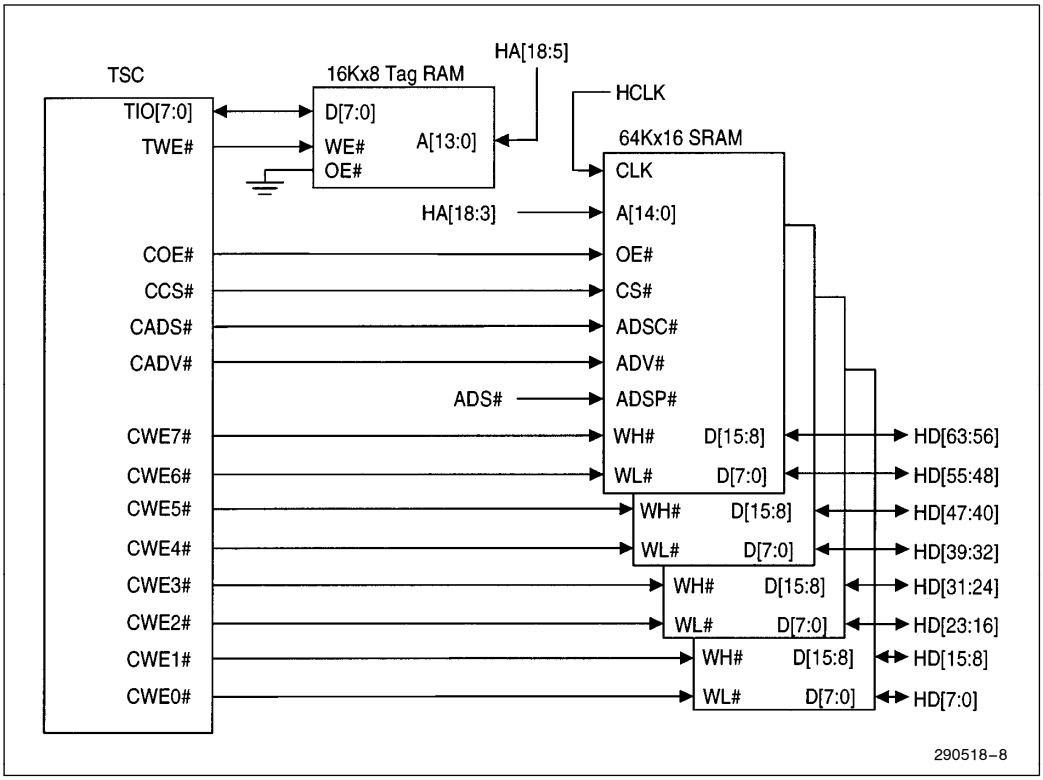


Figure 6. 512-Kbyte Second Level Cache (Burst SRAM)

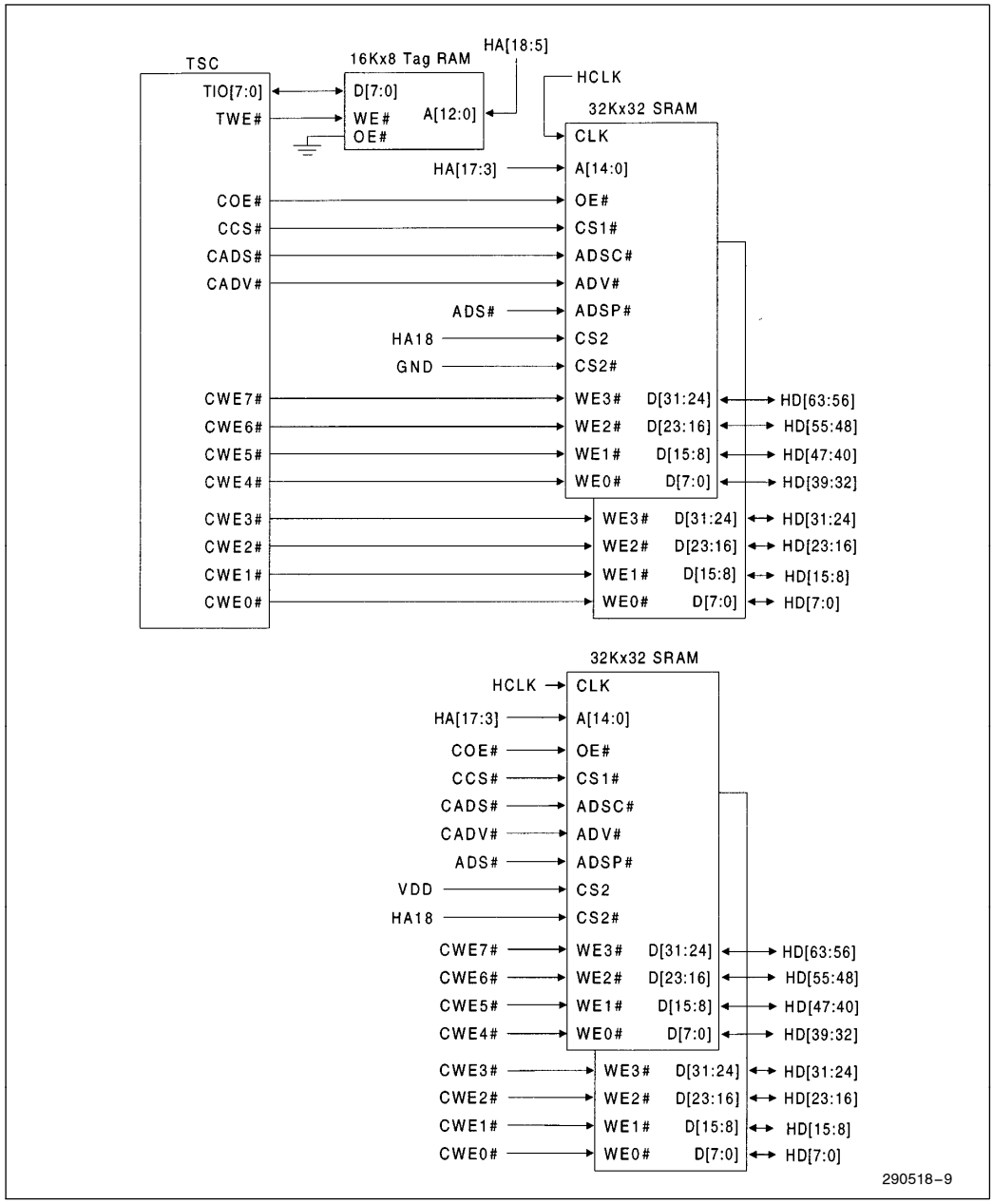


Figure 7. Two Bank 512-Kbyte Second Level Cache (Pipelined Burst SRAM)

4.4 DRAM Interface

The 82430FX PCIset's main memory DRAM interface supports a 64-bit wide memory array and main memory sizes from 4 to 128 Mbytes. The TSC generates the RAS#, CAS#, WE# (using MOE#) and multiplexed addresses for the DRAM array and controls the data flow through the 82438FX TDP's. For CPU-to-DRAM cycles the address flows through the TSC and data flows through the TDP's. For PCI or ISA cycles to memory the address flows through the TSC and data flows to the TDP's through the TSC and PLINK bus. The TSC and TDP DRAM interfaces are synchronous to the CPU clock.

The 82430FX PCIset supports industry standard 32-bit wide memory modules with fast page-mode DRAMs and EDO (Extended Data Out) DRAMs (also known as Hyper Page mode). With twelve multiplexed address lines (MA[11:0]), the TSC supports 512Kx32, 1M32, 2Mx32, and 4Mx32 SIMM's (both symmetrical and asymmetrical addressing). Five RAS# lines permit up to five rows of DRAM and eight CAS# lines provide byte write control over the array. The TSC supports 60 ns and 70 ns DRAMs (both single and double-sided SIMM's). The TSC also provides an automatic RAS# only refresh, at a rate of 1 refresh per 15.6 ms at 66 MHz, 60 MHz, and 50 MHz. A refresh priority queue and ''smart refresh'' algorithm are used to minimize the performance impact due to refresh.

The DRAM controller interface is fully configurable through a set of control registers (see Register Description section for programming details). The DRAM interface is configured by the DRAM Control Mode Register, the five DRAM Row Boundary (DRB) Registers, and the DRAM Row Type (DRT) Register. The DRAM Control Mode Registers configure the DRAM interface to select fast page-mode or EDO DRAMs, RAS timings, and CAS rates. The five DRB Registers define the size of each row in the memory array, enabling the TSC to assert the proper RAS# line for accesses to the array.

Seven Programmable Attribute Map (PAM) Registers are used to specify the cacheability, PCI enable, and read/write status of the memory space between 640 Kbytes and 1 Mbyte. Each PAM Register defines a specific address area enabling the system to selectively mark specific memory ranges as cacheable, read-only, write-only, read/write, or disabled. When a memory range is disabled, all CPU accesses to that range are forwarded to PCI.

The TSC also supports one of two memory holes; either from 512 Kbytes − 640 Kbytes or from 15 Mbytes − 16 Mbytes in main memory. Accesses to the memory holes are forwarded to PCI. The memory hole can be enabled/disabled through the DRAM Control Register. All other memory from 1 Mbyte to the top of main memory is read/write and cacheable.

The SMRAM memory space is controlled by the SMRAM Control Register. This register selects if the SMRAM space is enabled, opened, closed, or locked. SMRAM space is between 640 Kbytes and 768 Kbytes. See section 3.2.17 for more details on SMRAM.

4.4.1 DRAM ORGANIZATION

Figure 8 illustrates a 4-SIMM configuration that supports 4 double-sided SIMM's and motherboard DRAM. RAS0# is used for motherboard memory. This memory should not be implemented with SIMMs.

Except for motherboard memory, a row in the DRAM array is made up of two SIMM's that share a common RAS# line. Within any given row, the two SIMMs must be the same size. For different rows, SIMM densities can be mixed in any order. Each row is controlled by 8 CAS lines. EDO and Standard page mode DRAM's can be mixed between rows or within a row. When DRAM types are mixed (EDO and standard page mode), each row will run optimized for that particular type of DRAM. If DRAM types are mixed within a row, page mode timings must be selected.

SIMMs can be used for the sockets connected to RAS[2:1]# and RAS[4:3]#. The two RAS lines permit double-sided SIMMs to be used in these socket pairs. The following rules apply to the SIMM configuration.

1. SIMM sockets can be populated in any order.
2. SIMM socket pairs need to be populated with the same densities. For example, SIMM sockets RAS[2:1]# should be populated with identical densities. However, SIMM sockets using RAS[4:3]# can be populated with different densities than the SIMM socket pair using RAS[2:1]#.

3. The TSC only recognizes a maximum of 128 Mbytes of main memory, even if populated with more memory.
4. EDO's and standard page mode can both be used.

4.4.2 MAIN MEMORY ADDRESS MAP

The main memory organization (Figure 9) represents the maximum 128 Mbytes of address space. Accesses to memory space above the top of main memory, video buffer range, or the memory gaps (if enabled) are not cacheable and are forwarded to PCI. Below 1 Mbyte, there are several memory segments with selectable cacheability.

4.4.3 DRAM ADDRESS TRANSLATION

The multiplexed row/column address to the DRAM memory array is provided by MA[11:0] which are derived from the host address bus or PCI address as defined by Table 10. The TSC has a 4-Kbyte page size. The page offset address is driven on the MA[8:0] lines when driving the column address. The MA[11:0] lines are translated from the address lines A[24:3] for all memory accesses.

Table 10. DRAM Address Translation

Memory Address, MA[11:0]	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Row Address	A24	A23	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column Address	X	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

The types of DRAMs depth configuration supported are:

Depth	Row Width	Column Width
512K	10	9
1M	10	10
2M	11	10
4M	11	11
4M	12	10

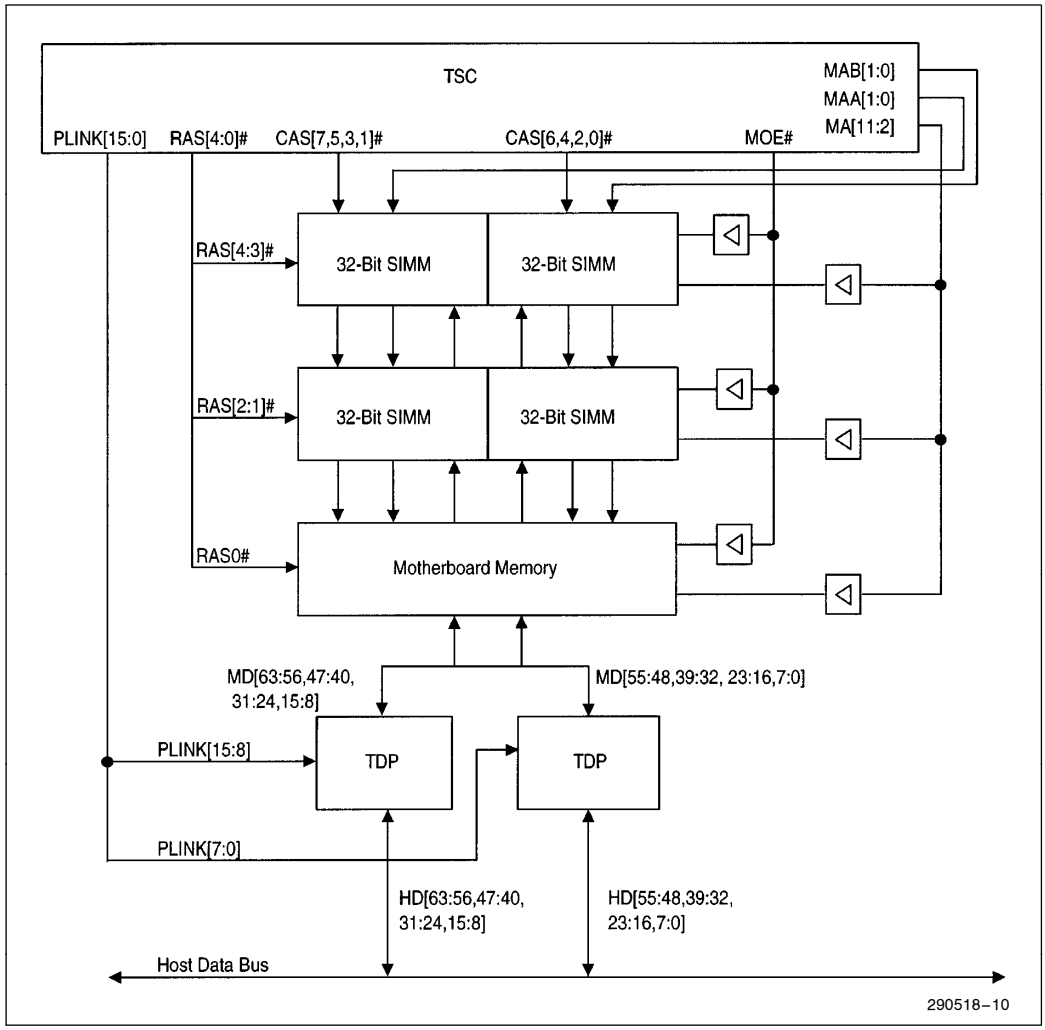


Figure 8. DRAM Array Connections

4.4.4 DRAM PAGE MODE

For any row containing standard page mode DRAM on read cycles, the TSC keeps CAS[7:0]# asserted until data is sampled by the TDPs.

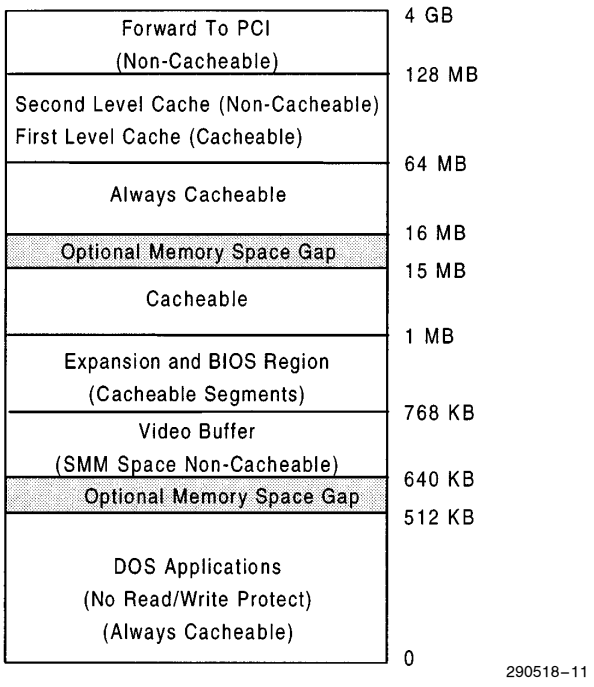


Figure 9. Memory Space Organization

4.4.5 EDO MODE

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge. Note that standard page mode DRAM tri-states the memory data when CAS# negates to precharge. With EDO, the CAS# precharge overlaps the memory data valid time. This allows CAS# to negate earlier while still satisfying the memory data valid window time.

The EDO Detect Mode Enable bit in the DRAM Control Register enables a special timing mode for BIOS to detect the DRAM type on a row by row basis.

4.4.5.1 BIOS Configuration of DRAM Array When Using EDO DRAMs

The following algorithm should be followed in order to dynamically detect if EDO DRAMs are installed in the system. When this algorithm has completed, the DRAM type installed in each row is programmed into the DRAM Row Type register (TSC PCI Config. Offset 68h):

1. Initialize all of the DRAM Row Type values to 'EDO' in the DRT register (TSC PCI Config. Offset 68h). Since there are five rows, the DRT register value becomes '1Fh'.
2. For each bank row (Row1, Row2, Row3, Row4, Row5)
   - Write all 1's to a QWORD address within the row.
   - Enable EDO detection mode by setting the EDO Detect Mode Enable bit in the DRAMC register (TSC PCI Config. Offset 57h) to 1.
   - Immediately read back the value of the QWORD ADDRESS.
   - If the value is not all 1's, then standard page mode DRAMs are installed in that row. Otherwise the EDO mode DRAMs are installed in that row.
   - Disable EDO detection mode by clearing the EDO Detect Mode Enable bit in the DRAMC register.
3. Depending on the findings of Step #2, program the DRAM row type into the corresponding bit in the DRT register (TSC PCI Config. Offset 68h): set for EDO type (1) or reset for standard page mode (0). Do not program this register until all of the bank rows have been tested.

Once all DRAM row banks have been tested for EDO, the EDME bit should be cleared in DRAMC (TSC PCI Config. Offset 57h, bit 2 is 0). It is very important that the EDME bit be cleared afterwards or performance will be seriously impacted.

Table 11. CPU to DRAM Performance Summary

Processor Cycle Type (Pipelined)	Clock Count (ADS# to BRDY#)	Comments
Burst read page hit	7-2-2-2	EDO
Read row miss	9-2-2-2 (note 1)	EDO
Read page miss	12-2-2-2	EDO
Back-to-back burst reads page hit	7-2-2-2-3-2-2-2	EDO
Burst read page hit	7-3-3-3	Standard page mode
Burst read row miss	9-3-3-3 (note 1)	Standard page mode
Burst read page miss	12-3-3-3	Standard page mode
Back-to-back burst read page hit	7-3-3-3-3-3-3-3	Standard page mode
Posted write	3-1-1-1	EDO/Standard page mode
Retire data for posted write	Every 3 clocks	EDO/Standard page mode

NOTES:
1. Due to the MA[11:2] to RAS# setup requirements, if a page is open, two clocks are added to the leadoff.
2. Read and write rates to DRAM are programmable via the DRAMT Register.

4.4.6 DRAM PERFORMANCE

The DRAM performance is controlled by the DRAM Timing Register, processor pipelining, and by the type of DRAM used (EDO or standard page mode). Table 11 lists both EDO and standard page mode optimum timings.

4.4.7 DRAM REFRESH

The TSC supports RAS# only refresh and generates refresh requests. The rate that requests are generated is determined by the DRAM Control Register. When a refresh request is generated, the request is placed in a four entry queue. The DRAM controller services a refresh request when the refresh queue is not empty and the controller has no other requests pending. When the refresh queue is full, refresh becomes the highest priority request and is serviced next by the DRAM controller, regardless of other pending requests. When the DRAM controller begins to service a refresh request, the request is removed from the refresh queue.

There is also a ''smart refresh'' algorithm implemented in the refresh controller. Except for Bank 0, refresh is only performed on banks that are populated. For bank 0, refresh is always performed. If only one bank is populated, using bank 0 will result in better performance.

4.4.8 SYSTEM MANAGEMENT RAM

The 82430FX PCIset support the use of main memory as System Management RAM (SMRAM), enabling the use of System Management Mode. When this function is disabled, the TSC memory map is defined by the DRB and PAM Registers. When SMRAM is enabled, the TSC reserves the A and B segments of main memory for use as SMRAM.

SMRAM is placed at A0000-BFFFFh via the SMRAM Space Register. Enhanced SMRAM features can also be enabled via this register. PCI masters can not access SMRAM when it is programmed to the A and B segments.

When the TSC detects a CPU stop grant special cycle, it generates a PCI Stop Grant Special cycle with 0002h in the message field (AD[15:0]) and 0012h in the message dependent data field (AD[31:16]) during the first data phase (IRDY# asserted).

A system using 5mm interrupts with addresses directed to SMM memory space in segments A0000 and B0000h must not have the 512K–640K memory hole enabled.

4.5 82438FX Data Path (TDP)

The TDP's provide the data path for host-to-main memory, PCI-to-main memory, and host-to-PCI cycles. Two TDP's are required for the 82430FX PCIset system configuration. The TSC controls the data flow through the TDP's with the PCMD[1:0], HOE#, POE#, MOE#, MSTB#, and MADV# signals.

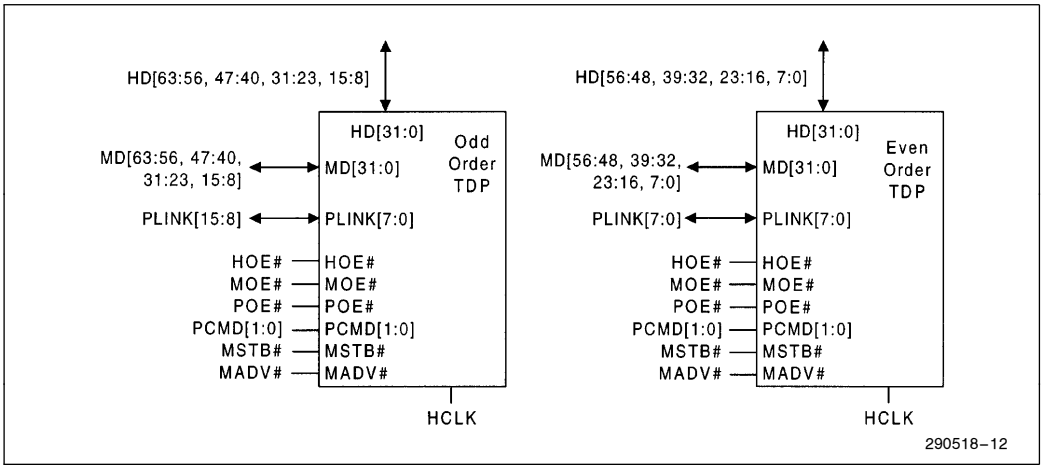


Figure 10. TDP 64-Bit Data Path Partitioning

The TDP's have three data path interfaces; the host bus (HD[63:0]). the memory bus (MD[63:0]), and the PLINK[15:0] bus between the TDP and TSC. The data paths for the TDP's are interleaved on byte boundaries (Figure 10). Byte lanes 0, 2, 4, and 6 from the host CPU data bus connects to the even order TDP and byte lanes 1, 3, 5, and 7 connect to the odd order TDP. PLINK[7:0] connects to the even order TDP and PLINK[15:8] connect to the odd order TDP.

4.6 PCI Bus Arbitration

The TSC's PCI Bus arbiter allows PCI peer-to-peer traffic concurrent with CPU main memory/second level cache cycles. The arbiter supports five PCI masters (Figure 11). REQ[3:0]#/GNT[3:0]# are used by PCI masters other than the PCI-to-ISA expansion bridge (PIIX). PHLD#/PHLDA# are the arbitration request/grant signals for the PIIX and provide guaranteed access time capability for ISA masters. PHLD#/PHLDA# also optimize system performance based on PIIX known policies.

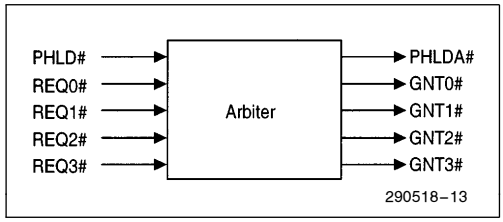


Figure 11. Arbiter

4.6.1 PRIORITY SCHEME AND BUS GRANT

The arbitration mechanism employs two interacting priority queues; one for the CPU and one for the PCI agents. The CPU queue guaranatees that the CPU is explicity granted the bus on every fourth arbitration event. The PCI priority queue determines which PCI agent is granted when PCI wins the arbitration event.

A rotating priority scheme is used to determine the highest priority requester in the case of simultaneous requests. If the highest priority input at arbitration time does not have an active request, the next priority active requester is granted the bus. Granting the bus to a lower priority requester does not change the rotation order, but it does advance the priority rotation. The rotation priority chain is fixed (Figure 12). If the highest priority agent does not request the bus, the next agent in the chain is the highest priority, and so forth down the chain.

When no PCI agents are requesting the bus, the CPU is the default owner of the bus. CPU cycles incur no additional delays in this state.

The grant signals (GNTx#) are normally negated after FRAME# assertion or 16 PCLKs from grant assertion, if no cycle has started. Once asserted, PHLDA# is only negated after PHLD# has been negated.

A possible PCI contention condition is possible if a PCI master had been requesting the PCI bus for some time and the TSC has just flushed its CPU-to-PCI write posting buffers. In this case, the TSC could grant the master the bus one clock early. The TSC will be in the process of floating its output buffers while a newly granted master is starting to drive the bus. Some contention is possible on AD[31:0], C/BE[3:0]# and PAR signals.

4.6.1.1 Arbitration Signaling Protocol: REQ# Functionality

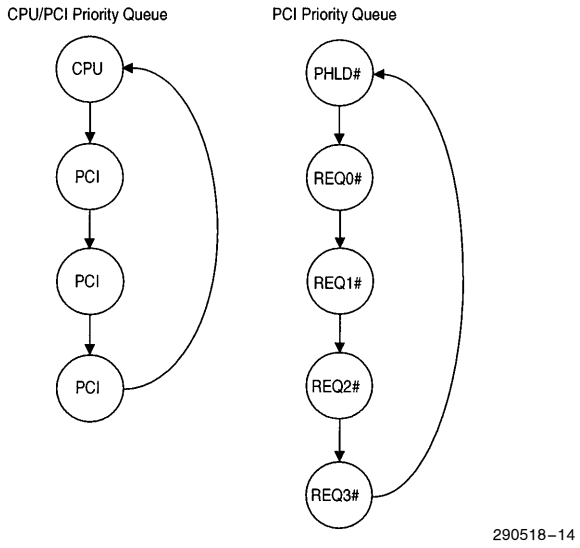
PCI Masters should follow the intent of the PCI Specification as quoted from the PCI Specification below:

1. ''Agents must only use REQ# to signal a true need to use the bus.''
2. ''An Agent must never use REQ# to ''park'' itself on the bus.''

A ''well behaved'' card should use REQ# when the bus is really needed. Typically REQ# should be removed, once the PCI master has been granted the bus, after FRAM# is asserted.

REQ# line behavior, of future PCI Cards, that *may not* operate as required could include:

1. Glitching REQ# lines for one or more clocks without any apparent reason.
2. Glitching REQ# lines and then not waiting for GNT# assertion.
3. Continually asserting REQ# lines in an attempt to park itself on the PCI bus.
4. Failing to assert FRAME# with several clocks of GNT# assertion when bus is idle.



NOTES:
1. For the CPU/PCI priority queue, the CPU is granted the PCI Bus after three consecutive PCI grants.
2. For the PCI priority queue, the last agent granted is always dropped to the bottom of the queue for the next arbitration cycle. However, the order of the chain is always preserved.

Figure 12. Arbitration Priority Rotation

PCI Cards that do not operate properly may not function properly with the TSC.

4.6.2 CPU POLICIES

The CPU never explicitly requests the bus. Instead, the arbiter grants the bus to the CPU when:

- the CPU is the highest priority
- PCI agents do not require main memory (peer-to-peer transfers or bus idle) and the PCI Bus is not currently locked by a PCI master

When the CPU is granted as highest priority, the MLT timer is used to guarantee a minimum amount of system resources to the CPU before another requesting PCI agent is granted.

An AHOLD mechanism controls granting the bus to the CPU.

4.7 Clock Generation and Distribution

The TSC and CPU should be clocked from one clock driver output to minimize skew between the CPU and TSC. The TDPs should share another clock driver output.

4.7.1 RESET SEQUENCING

The TSC is asynchronously reset by the PCI reset (RST#). After RST# is negated, the TSC resets the TDP by driving HOE#, MOE#, and POE# to 1 for two HCLKs. The TSC changes HOE#, MOE#, and POE# to their default value after the TDP is reset.

Arbiter (Central Resource) Functions on Reset

The TSC arbiter includes support for PCI central resource functions. These functions include driving the AD[31:0], C/BE[3:0]#, and PAR signals when no agent is granted the PCI Bus and the bus is idle. The TSC drives 0's on these signals during reset and drives valid levels when no other agent is granted and the bus is idle.

5.0 PINOUT AND PACKAGE INFORMATION

5.1 82437FX Pinout

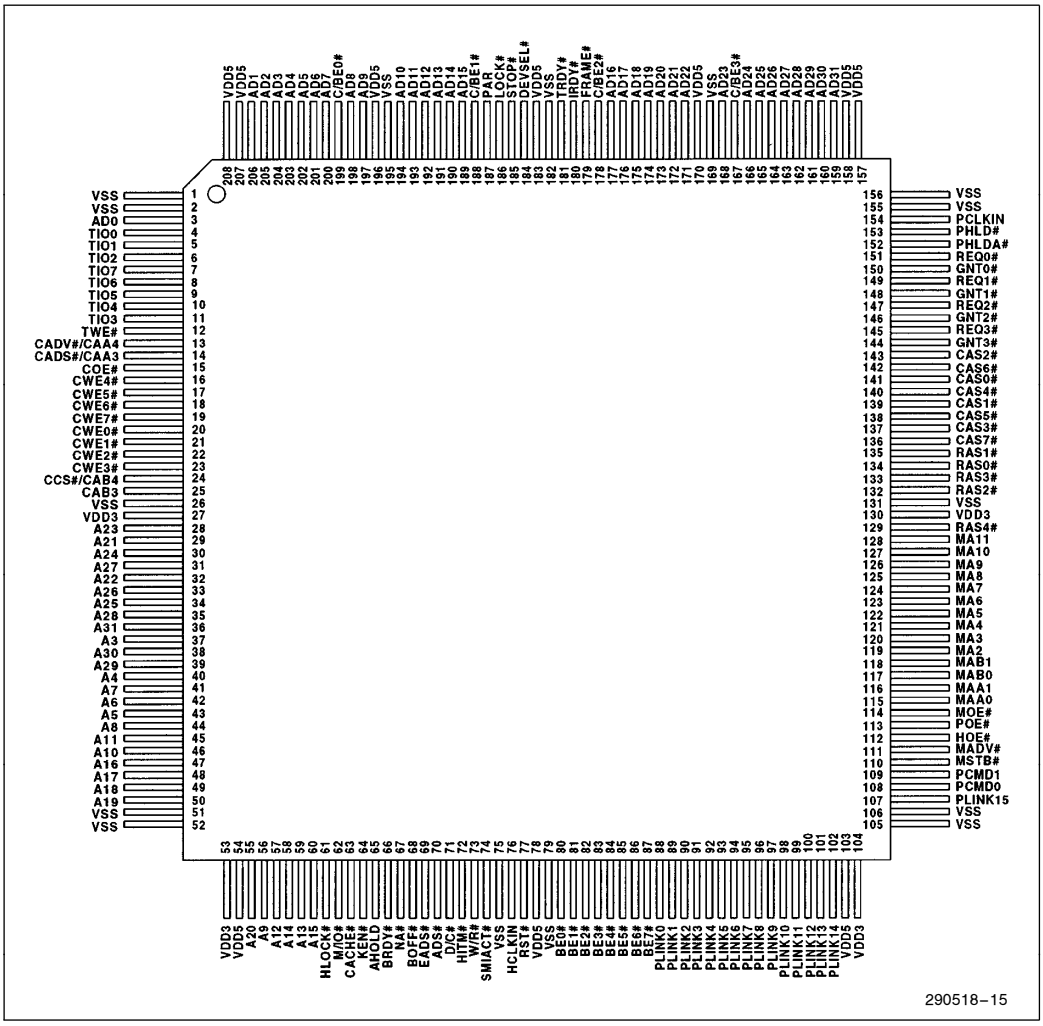


Figure 13. 82437FX Pin Assignment

Table 12. 82437FX Alphabetical Pin Assignment

Name	Pin #	Type
A3	37	I/O
A4	40	I/O
A5	43	I/O
A6	42	I/O
A7	41	I/O
A8	44	I/O
A9	56	I/O
A10	46	I/O
A11	45	I/O
A12	57	I/O
A13	59	I/O
A14	58	I/O
A15	60	I/O
A16	47	I/O
A17	48	I/O
A18	49	I/O
A19	50	I/O
A20	55	I/O
A21	29	I/O
A22	32	I/O
A23	28	I/O
A24	30	I/O
A25	34	I/O
A26	33	I/O
A27	31	I/O
A28	35	I/O
A29	39	I/O
A30	38	I/O
A31	36	I/O

Name	Pin #	Type
AD0	3	I/O
AD1	206	I/O
AD2	205	I/O
AD3	204	I/O
AD4	203	I/O
AD5	202	I/O
AD6	201	I/O
AD7	200	I/O
AD8	198	I/O
AD9	197	I/O
AD10	194	I/O
AD11	193	I/O
AD12	192	I/O
AD13	191	I/O
AD14	190	I/O
AD15	189	I/O
AD16	177	I/O
AD17	176	I/O
AD18	175	I/O
AD19	174	I/O
AD20	173	I/O
AD21	172	I/O
AD22	171	I/O
AD23	168	I/O
AD24	166	I/O
AD25	165	I/O
AD26	164	I/O
AD27	163	I/O
AD28	162	I/O

Name	Pin #	Type
AD29	161	I/O
AD30	160	I/O
AD31	159	I/O
ADS #	70	I
AHOLD	65	O
BE0 #	80	I
BE1 #	81	I
BE2 #	82	I
BE3 #	83	I
BE4 #	84	I
BE5 #	85	I
BE6 #	86	I
BE7 #	87	I
BOFF #	68	O
BRDY #	66	O
C/BE0 #	199	I/O
C/BE1 #	188	I/O
C/BE2 #	178	I/O
C/BE3 #	167	I/O
CAB3	25	O
CACHE #	63	I
CADS # / CAA3	14	O
CADV # / CAA4	13	O
CAS0 #	141	O
CAS1 #	139	O
CAS2 #	143	O
CAS3 #	137	O
CAS4 #	140	O

Table 12. 82437FX Alphabetical Pin Assignment (Continued)

Name	Pin #	Type
CAS5#	138	O
CAS6#	142	O
CAS7#	136	O
CCS# / CAB4	24	O
COE#	15	O
CWE0#	20	O
CWE1#	21	O
CWE2#	22	O
CWE3#	23	O
CWE4#	16	O
CWE5#	17	O
CWE6#	18	O
CWE7#	19	O
D/C#	71	I
DEVSEL#	184	I/O
EADS#	69	O
FRAME#	179	I/O
GNT0#	150	O
GNT1#	148	O
GNT2#	146	O
GNT3#	144	O
HCLKIN	76	I
HITM#	72	I
HLOCK#	61	I
HOE#	112	O
IRDY#	180	I/O
KEN#	64	O
LOCK#	186	I/O
M/IO#	62	I
MA2	119	O

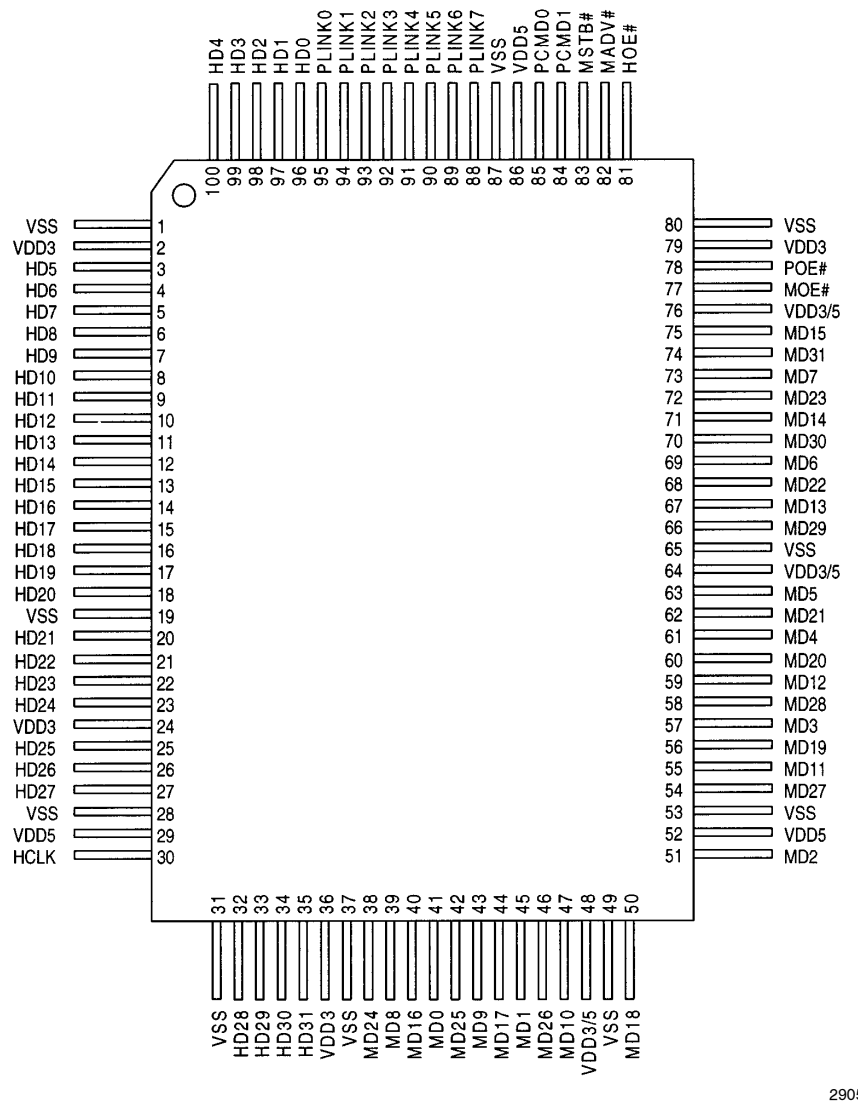
Name	Pin #	Type
MA3	120	O
MA4	121	O
MA5	122	O
MA6	123	O
MA7	124	O
MA8	125	O
MA9	126	O
MA10	127	O
MA11	128	O
MAA0	115	O
MAA1	116	O
MAB0	117	O
MAB1	118	O
MADV#	111	O
MOE#	114	O
MSTB#	110	O
NA#	67	O
PAR	187	I/O
PCLKIN	154	I
PCMD0	108	O
PCMD1	109	O
PHLD#	153	I
PHLDA#	152	O
PLINK0	88	I/O
PLINK1	89	I/O
PLINK2	90	I/O
PLINK3	91	I/O
PLINK4	92	I/O
PLINK5	93	I/O
PLINK6	94	I/O
PLINK7	95	I/O

Name	Pin #	Type
PLINK8	96	I/O
PLINK9	97	I/O
PLINK10	98	I/O
PLINK11	99	I/O
PLINK12	100	I/O
PLINK13	101	I/O
PLINK14	102	I/O
PLINK15	107	I/O
POE#	113	O
RAS0#	134	O
RAS1#	135	O
RAS2#	132	O
RAS3#	133	O
RAS4#	129	O
REQ0#	151	I
REQ1#	149	I
REQ2#	147	I
REQ3#	145	I
RST#	77	I
SMIACT#	74	I
STOP#	185	I/O
TIO0	4	I/O
TIO1	5	I/O
TIO2	6	I/O
TIO3	11	I/O
TIO4	10	I/O
TIO5	9	I/O
TIO6	8	I/O
TIO7	7	I/O
TRDY#	181	I/O
TWE#	12	O

Table 12. 82437FX Alphabetical Pin Assignment (Continued)

Name	Pin #	Type
VDD3	27	V
VDD3	53	V
VDD3	104	V
VDD3	130	V
VDD5	54	V
VDD5	78	V
VDD5	103	V
VDD5	157	V
VDD5	158	V
VDD5	170	V
VDD5	183	V
VDD5	196	V
VDD5	207	V
VDD5	208	V
VSS	1	V
VSS	2	V
VSS	26	V
VSS	51	V
VSS	52	V
VSS	75	V
VSS	79	V
VSS	105	V
VSS	106	V
VSS	131	V
VSS	155	V
VSS	156	V
VSS	169	V
VSS	182	V
VSS	195	V
W/R#	73	I

5.2 82438FX Pinout



290518–16

NOTES:
VDD3 is connected to the 3.3V rail; VDD5 is connected to the 5V, VDD3/5 is connected to the 3.3V rail for 3.3V DRAMs and to the 5V rail for 5V DRAMs.

Figure 14. 82438FX Pin Assignment

Table 13. 82438FX Alphabetical Pin Assignment

Name	Pin #	Type
HCLK	30	I
HD0	96	I/O
HD1	97	I/O
HD2	98	I/O
HD3	99	I/O
HD4	100	I/O
HD5	3	I/O
HD6	4	I/O
HD7	5	I/O
HD8	6	I/O
HD9	7	I/O
HD10	8	I/O
HD11	9	I/O
HD12	10	I/O
HD13	11	I/O
HD14	12	I/O
HD15	13	I/O
HD16	14	I/O
HD17	15	I/O
HD18	16	I/O
HD19	17	I/O
HD20	18	I/O
HD21	20	I/O
HD22	21	I/O
HD23	22	I/O
HD24	23	I/O
HD25	25	I/O
HD26	26	I/O
HD27	27	I/O
HD28	32	I/O

Name	Pin #	Type
HD29	33	I/O
HD30	34	I/O
HD31	35	I/O
HOE #	81	I
MADV #	82	I
MD0	41	I/O
MD1	45	I/O
MD2	51	I/O
MD3	57	I/O
MD4	61	I/O
MD5	63	I/O
MD6	69	I/O
MD7	73	I/O
MD8	39	I/O
MD9	43	I/O
MD10	47	I/O
MD11	55	I/O
MD12	59	I/O
MD13	67	I/O
MD14	71	I/O
MD15	75	I/O
MD16	40	I/O
MD17	44	I/O
MD18	50	I/O
MD19	56	I/O
MD20	60	I/O
MD21	62	I/O
MD22	68	I/O
MD23	72	I/O
MD24	38	I/O

Name	Pin #	Type
MD25	42	I/O
MD26	46	I/O
MD27	54	I/O
MD28	58	I/O
MD29	66	I/O
MD30	70	I/O
MD31	74	I/O
MOE #	77	I
MSTB #	83	I
PCMD0	85	I
PCMD1	84	I
PLINK0	95	I/O
PLINK1	94	I/O
PLINK2	93	I/O
PLINK3	92	I/O
PLINK4	91	I/O
PLINK5	90	I/O
PLINK6	89	I/O
PLINK7	88	I/O
POE #	78	I
VDD3	2	V
VDD3	24	V
VDD5	29	V
VDD3	36	V
VDD3/5	48	V
VDD5	52	V
VDD3/5	64	V
VDD3/5	76	V
VDD3	79	V
VDD5	86	V

Table 13. 82438FX Alphabetical Pin Assignment (Continued)

Name	Pin #	Type
VSS	1	V
VSS	19	V
VSS	28	V
VSS	31	V

Name	Pin #	Type
VSS	37	V
VSS	49	V
VSS	53	V
VSS	65	V

Name	Pin #	Type
VSS	80	V
VSS	87	V

5.3 82437FX Package Dimensions

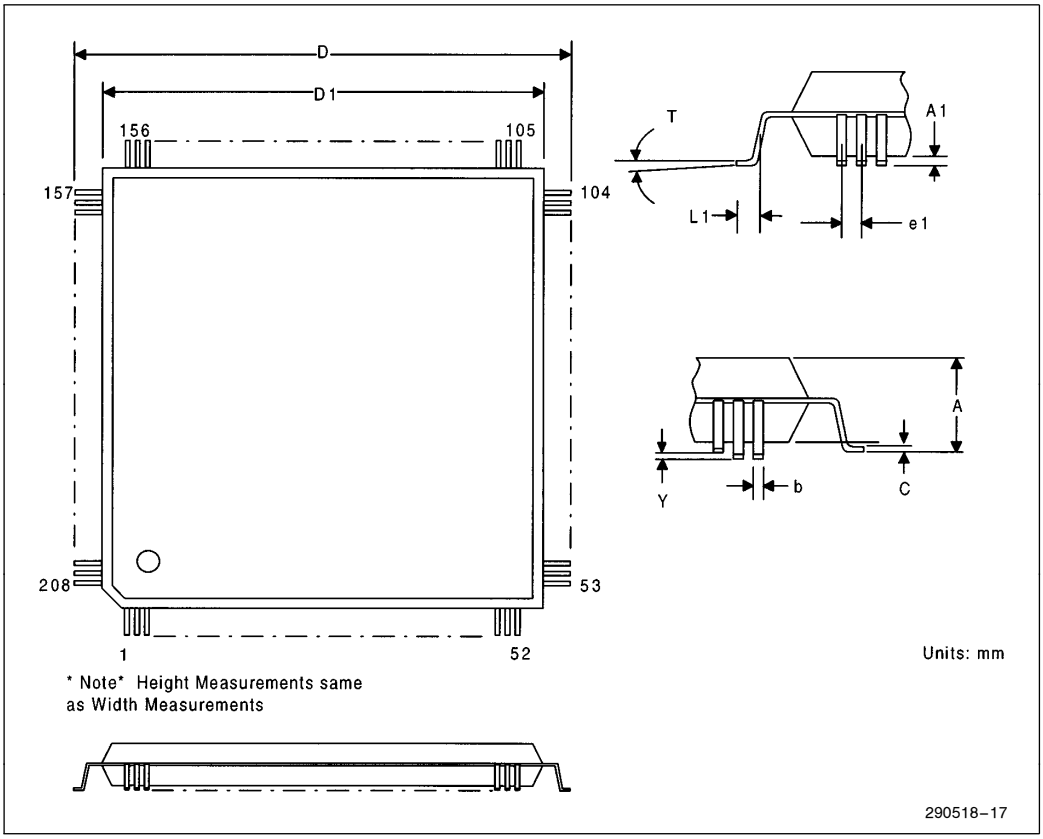


Figure 15. 208 Pin Quad Flat Pack (QFP) Dimensions

Table 14. 208 Pin Quad Flat Pack (QFP) Dimensions

Symbol	Description	Value (mm)
A	Seating Height	4.25 (max)
A1	Stand-off	0.05 (min); 0.40 (max)
b	Lead Width	0.2 ± 0.10
C	Lead Thickness	0.15 +0.1/-0.05
D	Package Length and Width, including pins	30.6 ± 0.4
D1	Package Length and Width, excluding pins	28 ± 0.2
e1	Linear Lead Pitch	0.5 ± 0.1
Y	Lead Coplanarity	0.08 (max)
L1	Foot Length	0.5 ± 0.2
T	Lead Angle	0° - 10°

5.4 82438FX Package Dimensions

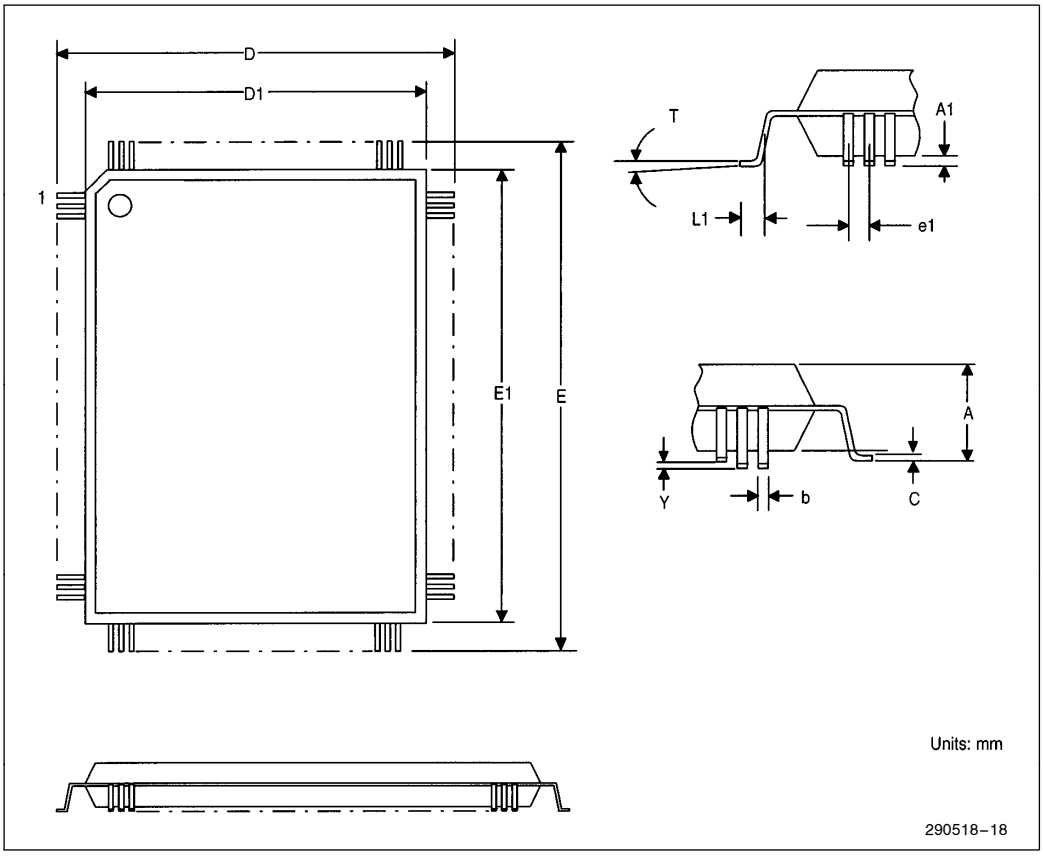


Figure 16. 100 Pin Plastic Quad Flat Pack (PQFP) Dimensions

Table 15. 100 Pin Quad Flat Pack (QFP) Dimensions

Symbol	Description	Value (mm)
A	Seating Height	3.3 (max)
A1	Stand-off	0.0 (min); 0.50 (max)
b	Lead Width	0.3 ± 0.10
C	Lead Thickness	0.15 +0.1/-0.05
D	Package Width, including pins	17.9 ± 0.4
D1	Package Width, excluding pins	14 0.2
E	Package Length, including pins	23.9 ± 0.4
E1	Package Length, excluding pins	20 ± 0.2
e1	Linear Lead Pitch	0.65 ± 0.12
Y	Lead Coplanarity	0.1 (max)
L1	Foot Length	0.8 0.2
T	Lead Angle	0° - 10°

6.0 82437FX TSC TESTABILITY

6.1 Test Mode Description

The test modes are decoded from the REQ#[3:0] and qualified with the RESET# pin. Test mode selection is asynchronous, these signals need to remain in their respective state for the duration of the test modes. The test modes are defined as follows.

Test Mode	RST#	REQ0#	REQ1#	REQ2#	REQ3#
NAND Tree	0	0	0	0	0

6.2 NAND Tree Mode

Tri-states all outputs and bi-directional buffers except for RST#, REQ#[3:0], GNT#[3:1]. The NAND tree follows the pins sequentially around the chip skipping only RESET#, REQ#[3:0], and GNT#[3:1]. The first input of the NAND chain GNT0#, and the NAND chain is routed counter-clockwise around the chip (e.g., GNT0#, PHLDA#, . . .). The only valid outputs during NAND tree mode are GNT1#, GNT2#, and GNT3#. GNT1# and GNT#3 are both final outputs of the NAND tree, and GNT2# is the halfway point of the NAND tree.

To perform a NAND tree test, all pins included in the NAND tree should be driven to 1 with the exception of PCLKIN which should be driven to 0.

Beginning with GNT0# and working counter-clockwise around the chip, each pin can be toggled with a resulting toggle observed on GNT3#, GNT2#, and GNT1#. The GNT2# output is provided so that the NAND tree test can be divided into two sections.

Table 16. NAND Tree Cell Order for the 82437FX

Pin #	Pin Name	Notes
77	RST#	Must be 0 to enter NAND tree mode. This signal must remain 0 during the entire NAND tree test.
145	REQ3#	Must be 0 to enter NAND tree mode. This signal must remain 0 during the entire NAND tree test.
147	REQ2#	Must be 0 to enter NAND tree mode. This signal must remain 0 during the entire NAND tree test.
149	REQ1#	Must be 0 to enter NAND tree mode. This signal must remain 0 during the entire NAND tree test.
151	REQ0#	Must be 0 to enter NAND tree mode. This signal must remain 0 during the entire NAND tree test.
150	GNT0#	Start of the NAND tree chain.
152	PHLDA#	
153	PHOLD#	
154	PCLKIN	PCLKIN needs to be 0 to pass the NAND-tree chain, a logic 1 will block the NAND-tree chain.
159	AD31	
160	AD30	
161	AD29	
162	AD28	
163	AD27	
164	AD26	
165	AD25	
166	AD24	
167	C/BE3#	
168	AD23	

Pin #	Pin Name	Notes
171	AD22	
172	AD21	
173	AD20	
174	AD19	
175	AD18	
176	AD17	
177	AD16	
178	C/BE2#	
179	FRAME#	
180	IRDY#	
181	TRDY#	
184	DEVSEL#	
185	STOP#	
186	LOCK#	
187	PAR	
188	C/BE1#	
189	AD15	
190	AD14	
191	AD13	
192	AD12	
193	AD11	
194	AD10	
197	AD9	
198	AD8	
199	C/BE0#	
200	AD7	
201	AD6	
202	AD5	
203	AD4	
204	AD3	
205	AD2	

Table 16. NAND Tree Cell Order for the 82437FX (Continued)

Pin #	Pin Name	Notes
206	AD1	
3	AD0	
4	TIO0	
5	TIO1	
6	TIO2	
7	TIO7	
8	TIO6	
9	TIO5	
10	TIO4	
11	TIO3	
12	TWE#	
13	CADV# / CAA4	
14	CADS# / CAA3	
15	COE#	
16	CWE4#	
17	CWE5#	
18	CWE6#	
19	CWE7#	
20	CWE0#	
21	CWE1#	
22	CWE2#	
23	CWE3#	
24	CCS# / CAB4	
25	CAB3	
28	A23	
29	A21	
30	A24	
31	A27	
32	A22	

Pin #	Pin Name	Notes
33	A26	
34	A25	
35	A28	
36	A31	
37	A3	
38	A30	
39	A29	
40	A4	
41	A7	
42	A6	
43	A5	
44	A8	
45	A11	
46	A10	
47	A16	
48	A17	
49	A18	
50	A19	
55	A20	
56	A9	
57	A12	
58	A14	
59	A13	
60	A15	
61	HLOCK#	
62	M/IO#	
63	CACHE#	
64	KEN#	
65	AHOLD	
66	BRDY#	

Table 16. NAND Tree Cell Order for the 82437FX (Continued)

Pin #	Pin Name	Notes
67	NA#	
68	BOFF#	
69	EADS#	
70	ADS#	
71	D/C#	
72	HITM#	
73	W/R#	
74	SMIACT#	
76	HCLKIN	
80	BE0#	
81	BE1#	
82	BE2#	
83	BE3#	
84	BE4#	
85	BE5#	
86	BE6#	
87	BE7#	
88	PLINK0	
89	PLINK1	
90	PLINK2	
91	PLINK3	
92	PLINK4	
93	PLINK5	
94	PLINK6	
95	PLINK7	
96	PLINK8	
97	PLINK9	
98	PLINK10	
99	PLINK11	
100	PLINK12	

Pin #	Pin Name	Notes
101	PLINK13	
102	PLINK14	
107	PLINK15	
108	PCMD0	
109	PCMD1	
110	MSTB#	
111	MADV#	
112	HOE#	
113	POE#	
114	MOE#	
115	MAA0	
116	MAA1	
117	MAB0	
118	MAB1	
119	MA2	
120	MA3	
121	MA4	
122	MA5	
123	MA6	
124	MA7	
125	MA8	
126	MA9	
127	MA10	
128	MA11	
129	RAS4#	
132	RAS2#	
133	RAS3#	
134	RAS0#	
135	RAS1#	
136	CAS7#	

Table 16. NAND Tree Cell Order for the 82437FX (Continued)

Pin #	Pin Name	Notes
137	CAS3#	
138	CAS5#	
139	CAS1#	
140	CAS4#	
141	CAS0#	
142	CAS6#	
143	CAS2#	
144	GNT3#	Final output of the NAND tree chain.
146	GNT2#	Half way point of the NAND tree chain.
148	GNT1#	Final output of the NAND-tree chain.

Figure 17 is a schematic of the NAND tree circuitry.

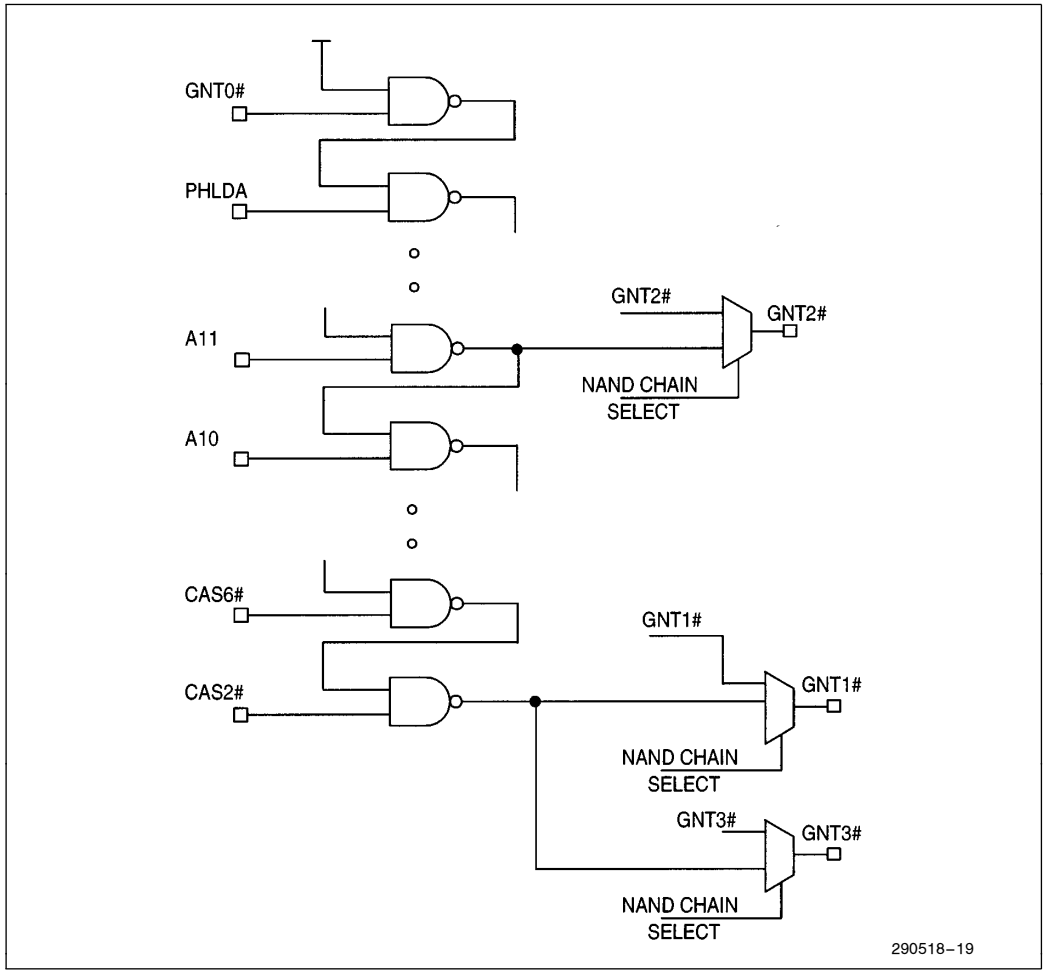


Figure 17. 82437FX NAND Tree Circuitry

NAND Tree Timing Requirements

Allow 800 ns for the input signals to propagate to the NAND tree outputs (input-to-output propagation delay specification).

7.0 82438FX TDP TESTABILITY

7.1 Test Mode Description

The test modes are decoded from HOE#, MOE#, POE#, and MSTB#. HCLK must be active for at least one clock to sample the above signals. Once these signals are sampled then HCLK must be asserted to 0 for the duration of the NAND tree test. The test modes are defined as follows.

Test Mode	HOE#	MOE#	POE#	MSTB#
NAND Tree	1	1	1	1

NAND tree mode is exited by starting HCLK with HOE#, MOE#, and POE# **not** equal to ‘‘111’’.

7.2 NAND Tree Mode

Tri-states all outputs and bidirectional buffers except for MD0 which is the output of the NAND tree. The NAND tree follows the pins sequentially around the chip skipping only HCLK and MD0. The first input of the NAND chain is HD5, and the NAND chain is routed counter-clockwise around the chip (e.g., HD5, HD6 . . .). The only valid output during NAND tree mode is MD0.

To perform a NAND tree test, all pins included in the NAND tree should be driven to 1, with the exception of HCLK and MDO. Beginning with HD5 and working counter-clockwise around the chip, each pin can be toggled with a resulting toggle observed on MD0. After changing an input pin to 0, keep it at 0 for the remainder of the NAND tree test.

Table 17. NAND Tree Cell Order for the 82438FX

Pin #	Pin Name	Notes
77	MOE#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
78	POE#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
81	HOE#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
83	MSTB#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
30	HCLK	HCLK must clock at least once to sample MOE#, POE#, HOE#, and MSTB# to select NAND tree mode. Then to enter NAND tree mode HCLK must remain 0. To exit NAND tree mode HCLK must be started.
41	MD0	Output of the NAND tree chain.
3	HD5	First signal in the NAND tree chain.
4	HD6	
5	HD7	
6	HD8	
7	HD9	
8	HD10	
9	HD11	
10	HD12	
11	HD13	
12	HD14	
13	HD15	
14	HD16	
15	HD17	
16	HD18	
17	HD19	
18	HD20	
20	HD21	
21	HD22	
22	HD23	
23	HD24	
25	HD25	
26	HD26	
27	HD27	
32	HD28	
33	HD29	
34	HD30	
35	HD31	
38	MD24	
39	MD8	
40	MD16	
42	MD25	
43	MD9	
44	MD17	
45	MD1	
46	MD26	
47	MD10	
50	MD18	
51	MD2	
54	MD27	
55	MD11	

Table 17. NAND Tree Cell Order for the 82438FX (Continued)

Pin #	Pin Name	Notes
56	MD19	
57	MD3	
58	MD28	
59	MD12	
60	MD20	
61	MD4	
62	MD21	
63	MD5	
66	MD29	
67	MD13	
68	MD22	
69	MD6	
70	MD30	
71	MD14	
72	MD23	
73	MD7	
74	MD31	
75	MD15	
77	MOE#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
78	POE#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
81	HOE#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
82	MADV#	
83	MSTB#	Must be 1 to enter NAND tree mode. This pin is included in the NAND tree mode input pin sequence.
84	PCMD1	
85	PCMD0	
88	PLINK7	
89	PLINK6	
90	PLINK5	
91	PLINK4	
92	PLINK3	
93	PLINK2	
94	PLINK1	
95	PLINK0	
96	HD0	
97	HD1	
98	HD2	
99	HD3	
100	HD4	Final signal in the NAND tree chain.

Figure 18 is a schematic of the NAND tree circuitry.

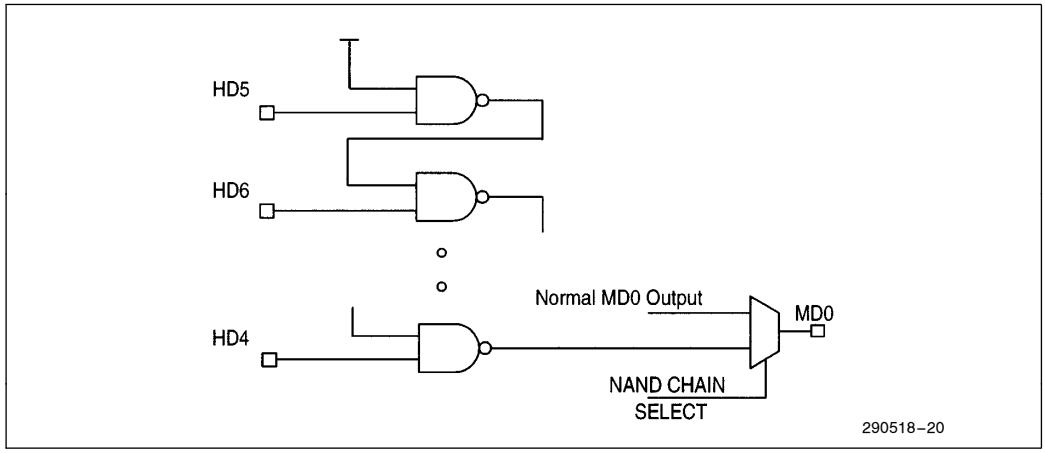


Figure 18. 82438FX NAND Tree Circuitry

NAND Tree Timing Requirements

Allow 500 ns for the input signals to propagate to the NAND tree outputs (input-to-output propagation delay specification).