## FEATURES

- Ultra Low Quiescent Power 8-phase single output PWM Controller
- Intel® VR12 and VR12.5, & Memory VR modes
- Overclocking & Gaming Modes
- PVI GPU VR mode
- Switching frequency from 194KHz to 2MHz per phase in 56 steps
- IR Efficiency Shaping Features including Variable Gate Drive, Dynamic Phase Control and Automatic Power State Switching
- Programmable 1-phase or 2-phase operation for Light Loads and Active Diode Emulation for Very Light Loads
- IR Adaptive Transient Algorithm (ATA) minimizes output bulk capacitors and system cost
- Auto-Phase Detection with PID Coefficient auto-scaling
- Fault Protection: OVP, UVP, OCP, OTP, CAT FLT
- I2C/SMBus/PMBus system interface for reporting of Temperature, Voltage, Current & Power telemetry for both loops
- Multiple Time Programming (MTP) with integrated charge pump for easy non-volatile programming
- Compatible with 3.3V tri-state drivers and IR ATL mode drivers
- +3.3V supply voltage; -40°C to 85°C ambient operation
- Pb-Free, RoHS, 6x6mm 48-pin, 0.4mm pitch QFN

## APPLICATIONS

- Intel® VR12 and VR12.5 based systems
- Overclocked & Gaming platforms

## DESCRIPTION

The IR3580 is a single-loop digital multi-phase buck controller that controls up to 8 phases. The IR3580 is fully compliant with Intel® VR12 and compliant with VR12.5 Rev 1.3 PWM specifications.

The IR3580 includes IR's Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. IR Variable Gate Drive optimizes the MOSFET gate drive voltage based on real-time load current. IR's Dynamic Phase Control adds/drops phases based upon load current. The IR3580 can be configured to enter 1 or 2-phase operation and active diode emulation mode automatically or by command.

IR's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors.

IR3580 has 127 possible address values for both the PMBus and I2C bus interfaces. The device configuration can be easily defined using the IR Digital Power Design Center (DPDC) GUI, and is stored in the on-chip Non-Volatile Memory (NVM). This reduces external components and minimizes the package size.

The IR3580 provides extensive OVP, UVP, OCP, OTP and CAT FLT fault protection and includes thermistor based temperature sensing or per phase temperature reporting when using the IR powIRstage. The controller is designed to work with either Rdson current sense PowIRstages or with DCR current sense.

The IR3580 also includes numerous VR design simplifying and differentiating features, like register diagnostics, which enable fast time-to-market.

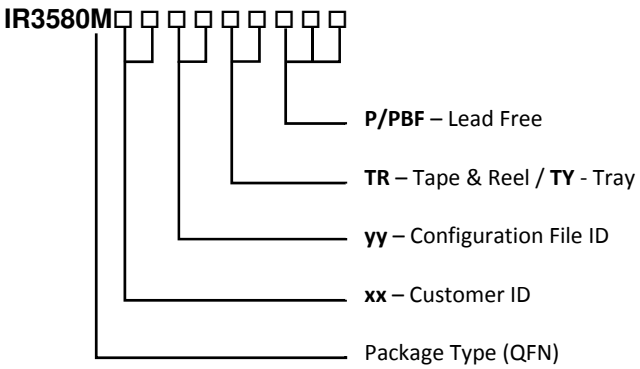
## ORDERING INFORMATION

| Base Part Number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IR3580 | 48-pin QFN 6 mm x 6 mm | Tape and Reel | 3000 | IR3580MxxyyTRP[1] |
| IR3580 | 48-pin QFN 6 mm x 6 mm | Tape and Reel | 3000 | IR3580MTRPBF |
| IR3580 | 48-pin QFN 6 mm x 6 mm | Tray | 4900 | IR3580MTYPBF |

**Notes:**

**1.** Customer Specific Configuration File, where xx = Customer ID and yy = Configuration File (Codes assigned by IR Marketing).

## ORDERING INFORMATION



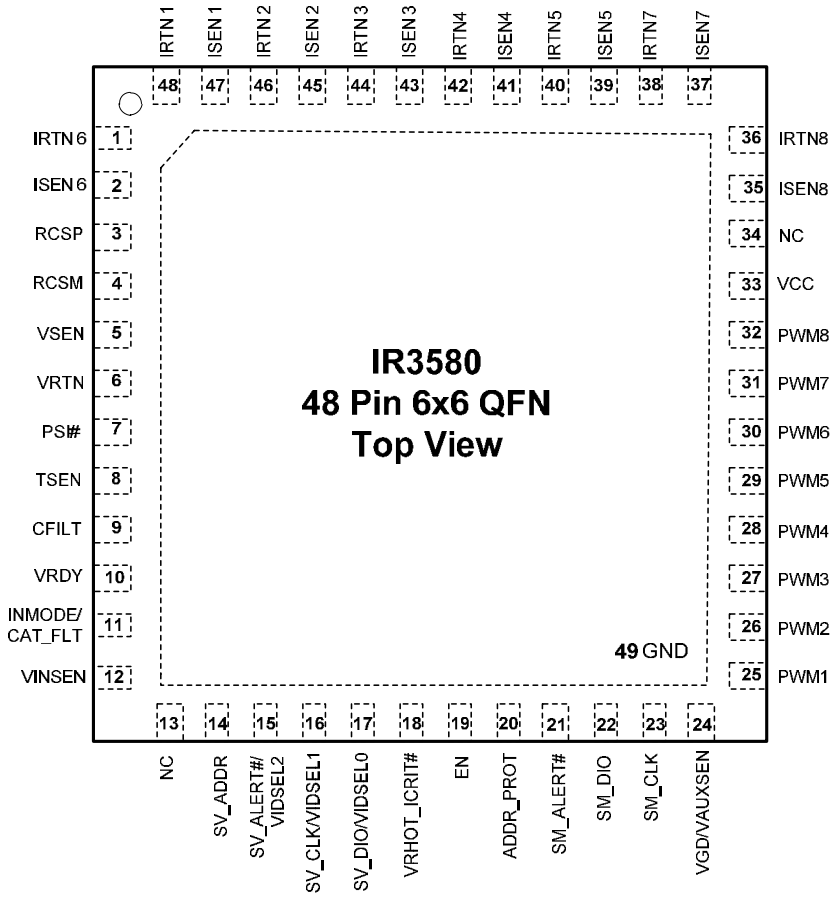




**Figure 1: IR3580 Pin Diagram**

# TYPICAL APPLICATION DIAGRAM

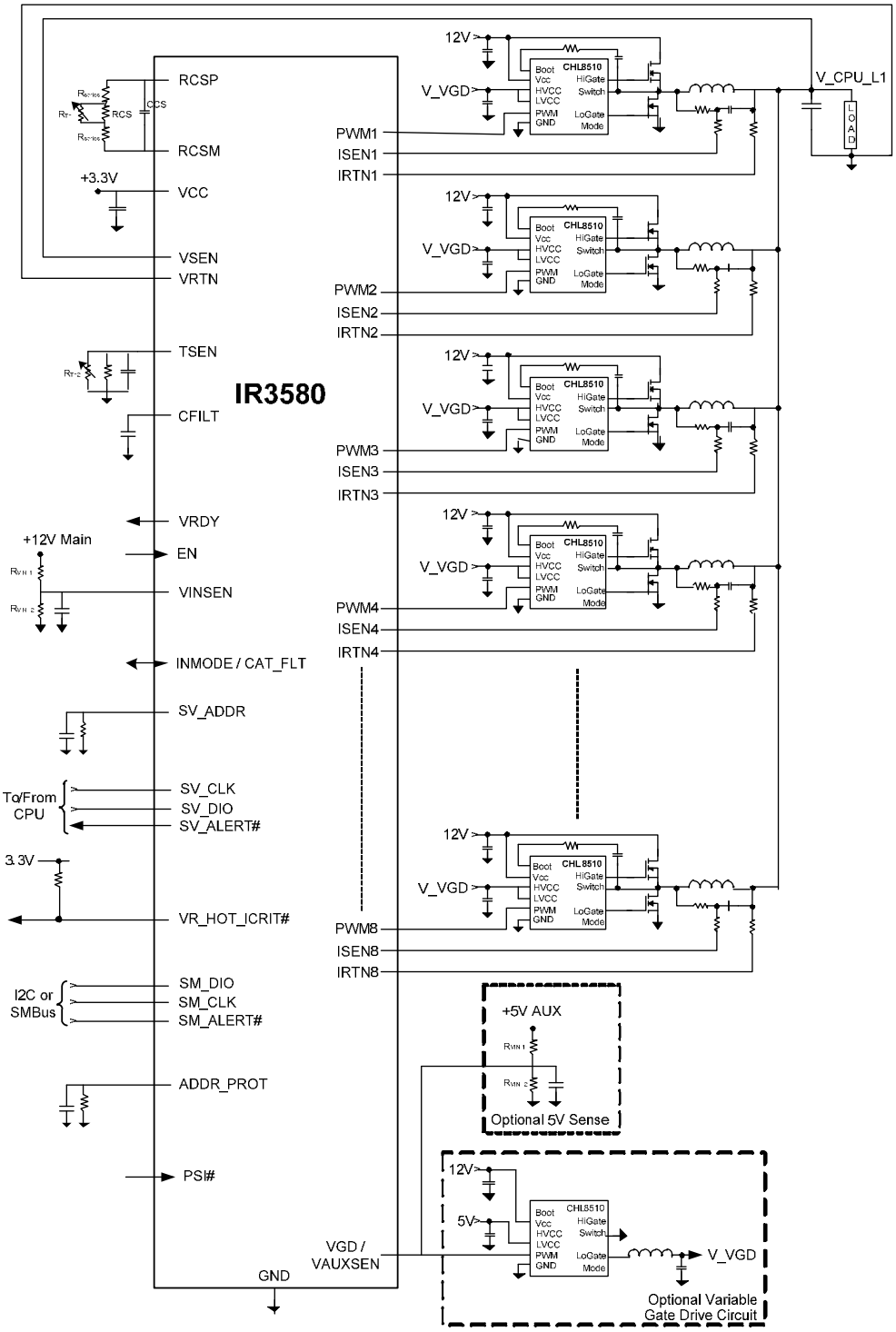



**Figure 2: VR using IR3580 Controller and CHL8510 MOSFET Drivers in 8-phase Configuration**

## PIN DESCRIPTIONS

| PIN# | PIN NAME | TYPE | PIN DESCRIPTION |
|---|---|---|---|
| 1 | IRTN6 | A [I] | **Phase 6 Current Sense Return Input.** Phase 6 sensed current input return (-).Short to GND if not used. |
| 2 | ISEN6 | A [I] | **Phase 6 Current Sense Input.** Phase 6 sensed current input (+). Short to GND if not used. |
| 3 | RCSP | A [O] | **Resistor Current Sense Positive.** This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation. |
| 4 | RCSM | A [O] | **Resistor Current Sense Minus.** This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation. |
| 5 | VSEN | A [I] | **Voltage Sense Input.** This pin is connected directly to the VR output voltage of Loop #1 at the load and should be routed differentially with VRTN. |
| 6 | VRTN | A [I] | **Voltage Sense Return Input.** This pin is connected directly to Loop#1 ground at the load and should be routed differentially with VSEN. |
| 7 | PSI# | A [I] | **Power Savings Indicator.** Output open drain pulldown (active low) for actively disabling external drivers when phases are unused to reduce system quiescent current. Define pin function using register setting. |
| 8 | TSEN | A [I] | **Temperature Sense Input.** An NTC network or a temperature reporting output from an IR PowIRstage can be connected to this pin to measure temperature for VRHOT and OTP shutdown. When connected to the IR PowIRstage's temperature output; the scaled input voltage to the controller needs to be at a gain of 4.88mV per degC and an offset of 0.365 Vdc so the controller can correctly report temperature. Typically a 10KOhm and 6.49KOhm resistive divider is used to accomplish the scaling between the power stage and the controller. Terminate to ground with a 10k resistor if not used. |
| 9 | CFILT | A [O] | **1.8V Decoupling.** A 1μF capacitor on this pin provides decoupling for the internal 1.8V supply. |
| 10 | VRDY | D [O] | **Voltage Regulator Ready Output.** Open-drain output that asserts high when the VR has completed soft-start to boot voltage. Pull-up to an external voltage through a resistor. |
| 11 | INMODE/ CAT FLT | D [B] | **Intel VR12 Mode Selection.** This pin may be configured to act as an Intel Mode Select pin to choose VR12 or VR12.5 operation.<br>**Catastrophic Fault Output Pin.** This pin may be used as a Catastrophic Fault CMOS Output Pin that is driven to VCC under output OVP, NVM CRC errors or a TSEN fault input. |
| 12 | VINSEN | A [I] | **Voltage Sense Input.** This is used to detect and measure a valid input supply voltage (typically 4.5V-13.2V) to the VR. Refer to **Error! Reference source not found.**Page **Error! Bookmark not defined.** for details. |
| 13 | NC | | **Do Not Connect.** |
| 14 | SV_ADDR | D [I] | **Serial VID Address.** If present, a resistor to ground sets the offset to the SVID address set in NVM. If not, the value stored in NVM is used. Requires a 0.01μF to ground for noise filtering. |
| 15 | SV_ALERT#/ VIDSEL2 | D [O] | **Serial VID ALERT# (INTEL).** SVID ALERT# is pulled low by the controller to alert the CPU of new VR12/12.5 Status. Pull-up to an external voltage through a resistor.<br>**Parallel VID selection.** When configured in GPU parallel VID mode, this pin is used to select the VID voltage registers. |
| 16 | SV_CLK/ VIDSEL1 | D [I] | **Serial VID Clock Input.** Clock input driven by the CPU Master.<br>**Parallel VID selection.** When configured in GPU parallel VID mode, this pin is used to select the VID voltage registers. |
| 17 | SV_DIO/ VIDSEL0 | D [B]/ D [I] | **Serial VID Data I/O.** Is a bi-directional serial line over which the CPU Master issues commands to slave/s.<br>**Parallel VID Selection.** When configured in GPU parallel VID mode, this pin is used to select the VID voltage registers. |
| 18 | VRHOT_ICRIT# | D [O] | **VRHOT_ICRIT# Output.** Active low alert pin that can be programmed to assert if temperature or average load current exceeds user-definable thresholds. Pull-up to an external voltage through a resistor. |

| PIN# | PIN NAME | TYPE | PIN DESCRIPTION |
|---|---|---|---|
| 19 | EN | D [I] | **VR Enable Input.** ENABLE is used to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up in the controller. The polarity of the chip enable function is bit-settable to either an active high or an active low configuration. When the controller is disabled, the controller de-asserts VR READY and shuts down the regulator. ENABLE pin cannot be left floating. ENABLE pin must be pulled high or low. |
| 20 | ADDR_PROT | D [B]/ | **Bus Address & I2C Bus Protection.** A resistor to ground on this pin sets the offset to the NVM value of the I2C address if configured to do so. Subsequently, this pin becomes a logic input to enable or disable communication on the I2C bus when protection is enabled. Requires a 0.01µF to ground for noise filtering. |
| 21 | SM_ALERT# | D [O] | **SMBus/PMBus Alert Line.** Active low alert pin to indicate that the regulator status has changed. Requires a pull-up. Ground if not used. |
| 22 | SM_DIO | D [B] | **Serial Data Line I/O.** I2C/SMBus/PMBus bi-directional serial data line. Ground if not used. |
| 23 | SM_CLK | D [I] | **Serial Clock Line Input.** I2C/SMBus/PMBus clock input. The interface is rated to 1 MHz. Ground if not used. |
| 24 | VGD/VAUXSEN | A [O]/ A [I] | **Variable Gate Drive PWM Output or Auxiliary Voltage Sense Input.** Multi-function pin that may be configured as Variable Gate Drive or Auxiliary Voltage Sense. As Variable Gate Drive, it is a PWM output that may be used to power MOSFET Driver and can be configured as inverted or non-inverted. As Auxiliary Voltage Sense, it monitors an additional power supply to ensure that both the IR3580 Vcc and other voltages (such as VCC to the driver) are operational. Float if not used. |
| 25 - 32 | PWM1 – PWM8 | A [O] | **Phase 1-8 Pulse Width Modulation Outputs.** PWM signal pin which is connected to the input of an external MOSFET gate driver. Refer to page **Error! Bookmark not defined.** for unused/disabled phases. The power-up state is high-impedance until ENABLE goes active. Float if not used. |
| 33 | VCC | A [P] | **Input Supply Voltage.** 3.3V supply to power the device. |
| 34 | NC | | **Do Not Connect.** |
| 35 | ISEN8 | A [I] | **Phase 8 Current Sense Input.** Phase 8 sensed current input (+). Short to GND if not used |
| 36 | IRTN8 | A [I] | **Phase 8 Current Sense Return Input.** Phase 8 sensed current input return (-). Short to GND if not used |
| 37 | ISEN7 | A [I] | **Phase 7 Current Sense Input.** Phase 7 sensed current input (+).Short to GND if not used |
| 38 | IRTN7 | A [I] | **Phase 7 Current Sense Return Input.** Phase 7 sensed current input return (-). Short to GND if not used |
| 39 | ISEN 5 | A [I] | **Phase 5 Current Sense Input.** Phase 5 sensed current input (+). Short to GND if not used |
| 40 | IRTN 5 | A [I] | **Phase 5 Current Sense Return Input.** Phase 5 sensed current input return (-). Short to GND if not used |
| 41 | ISEN 4 | A [I] | **Phase 4 Current Sense Input.** Phase 4 sensed current input (+). Short to GND if not used |
| 42 | IRTN 4 | A [I] | **Phase 4 Current Sense Return Input.** Phase 4 sensed current input return (-). Short to GND if not used |
| 43 | ISEN 3 | A [I] | **Phase 3 Current Sense Input.** Phase 3 sensed current input (+). Short to GND if not used |
| 44 | IRTN 3 | A [I] | **Phase 3 Current Sense Return Input.** Phase 3 sensed current input return (-). Short to GND if not used |
| 45 | ISEN 2 | A [I] | **Phase 2 Current Sense Input.** Phase 2 sensed current input (+). Short to GND if not used |
| 46 | IRTN 2 | A [I] | **Phase 2 Current Sense Return Input.** Phase 2 sensed current input return (-). Short to GND if not used |
| 47 | ISEN 1 | A [I] | **Phase 1 Current Sense Input.** Phase 1 sensed current input (+). Short to GND if not used |
| 48 | IRTN 1 | A [I] | **Phase 1 Current Sense Return Input.** Phase 1 sensed current input return (-). Short to GND if not used |
| 49 (PAD) | GND | | **Ground.** Ground reference for the IC. The large metal pad on the bottom must be connected to Ground. |

**Note 1:** A - Analog; D – Digital; [I] – Input; [O] – Output; [B] – Bi-directional; [P] - Power

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage (VCC) | GND-0.3V to 4.0V |
| RCSPx, RCSMx | 0 to 2.2V |
| VSEN, VRTN, ISENx, IRTNx | GND-0.2V to VCC + 0.3V |
| CFILT, VINSEN | GND-0.2V to 2.2V |
| TSEN | GND-0.3V to VCC |
| VIDSELx, SV_ADDR, SV_CLK, SV_DIO, SV_ALERT#, PSI# | GND-0.3V to VCC |
| PWMx | GND-0.3V to 4.1V |
| VRDY, EN, ADDR_PROT, VRHOT_ICRIT#, INMODE, CAT FLT | GND-0.3V to VCC |
| SM_DIO, SM_CLK, SM_ALERT# | GND-0.3V to 5.5V |
| **Thermal Information** | |
| Thermal Resistance ($\theta_{JA}$ & $\theta_{JC}$)[1] | 29°C/W & 3°C/W |
| Maximum Operating Junction Temperature | -40°C to +125°C |
| Maximum Storage Temperature Range | -65°C to +150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |

**Note:** 1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

## MARKING INFORMATION

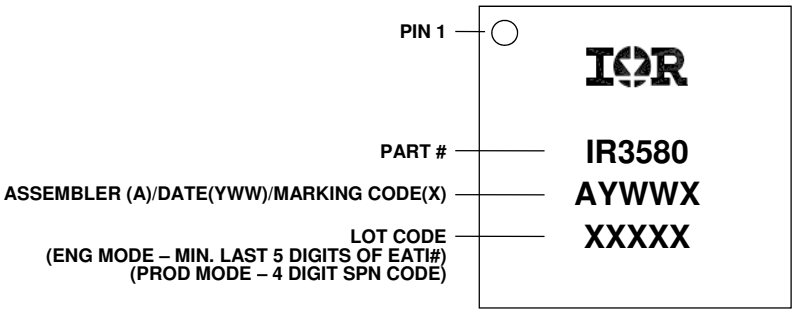



**Figure 3: Package Marking**

## PACKAGE INFORMATION

QFN 6x6mm, 48-pin

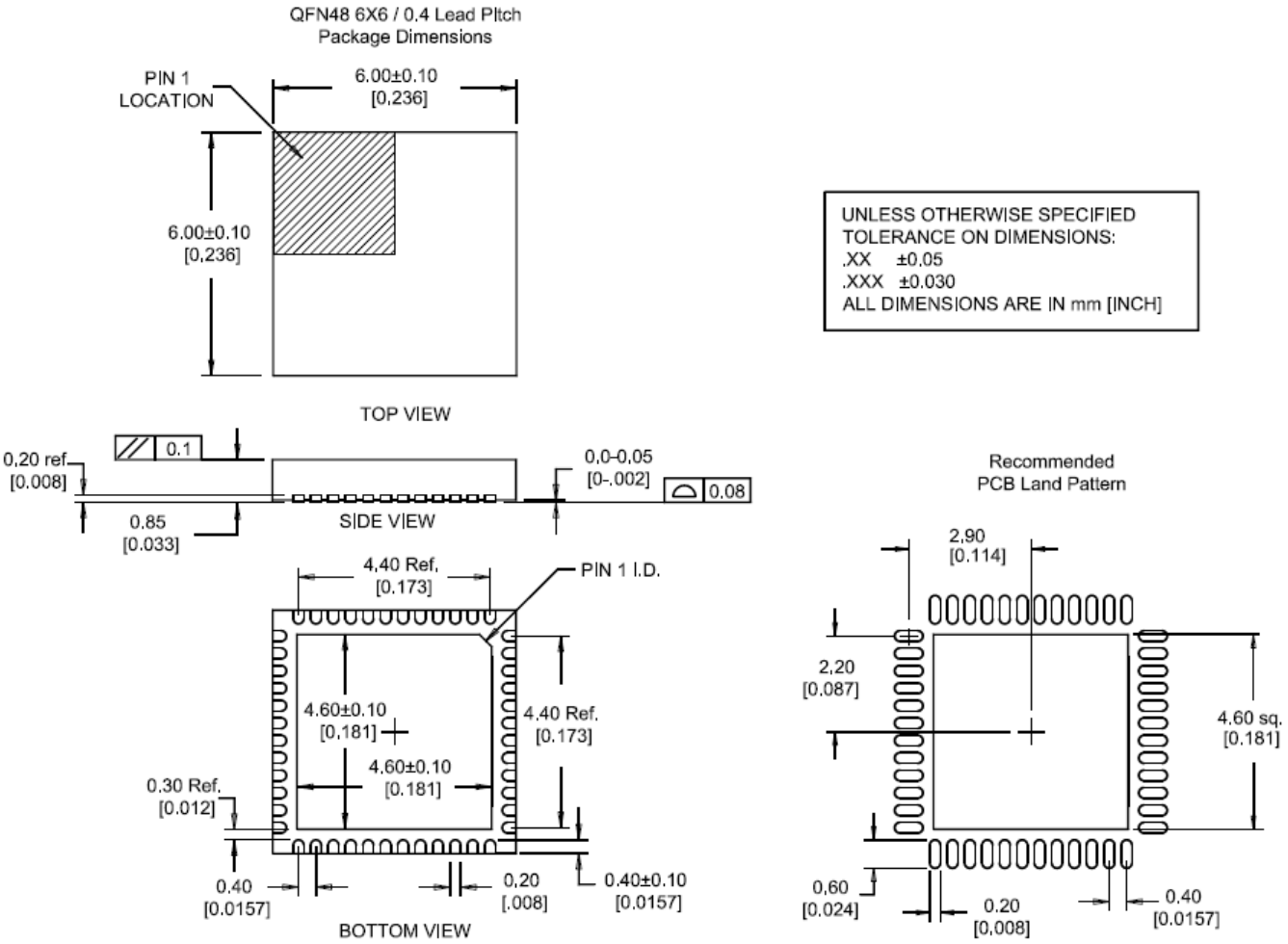



**Figure 4: Package Dimensions**