19-4813; Rev 0; 7/09

EVALUATION KIT AVAILABLE

1.62V to 3.6V, 8-Channel, High-Speed LLT

General Description

The MAX13055E–MAX13058E 8-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13055E–MAX13058E are ideal for level translation in systems with 8 channels. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic-high signals presented on the V_L side of the device appear as a logic-high signal on the V_{CC} side of the device and vice versa.

The MAX13055E–MAX13058E operate at full speed with external drivers that source as little as 4mA output current or larger. Each input/output (I/O) channel is pulled up to V_{CC} or V_L by an internal 40µA current source, allowing the MAX13055E–MAX13058E to be driven by either push-pull or open-drain drivers.

The MAX13055E–MAX13058E feature an enable (EN) input to place the device into a low-power shutdown mode when driven low. In addition, the MAX13055E–MAX13058E feature an automatic shutdown mode that disables the part when V_{CC} is less than V_L. Each device has a different I/O $V_{L\_}$ and I/O $V_{CC\_}$ state during shutdown mode (see the *Ordering Information/Selector Guide*).

The MAX13055E–MAX13058E operate with V_{CC} voltages from +2.2V to +3.6V and V_L voltages from +1.62V to +3.2V, making them ideal for data transfer between low-voltage ASIC/PLDs and higher voltage systems. The MAX13055E–MAX13058E are available in 0.4mm pitch, 24-bump WLP and 28-pin TQFN (3.5mm x 5.5mm) packages. The MAX13055E–MAX13058E operate over the extended -40°C to +85°C temperature range.

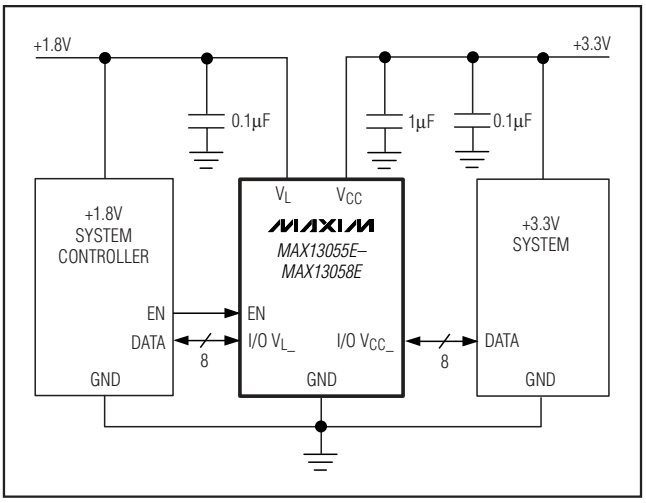
Applications

Low-Voltage ASIC Level Translation	Portable Communication Devices
Smart Card Readers	Cell Phones
Camera Modules	GPS
Portable POS Systems	Telecomm Equipment

Features

- **Compatible with 4mA Input Drivers or Larger**
- **100Mbps Guaranteed Data Rate**
- **8 Bidirectional Channels**
- **+1.62V ≤ V_L ≤ +3.2V and +2.2V ≤ V_{CC} ≤ +3.6V Supply Voltage Range**
- **24-Bump WLP (0.4mm Pitch) Lead-Free Package**
- **28-Pin TQFN (3.5mm x 5.5mm) Lead-Free Package**
- **Extended ESD Protection on I/O V_{CC} Lines**
  - **±15kV per Human Body Model**
  - **±15kV IEC 61000-4-2 Air Discharge**
  - **±8kV IEC 61000-4-2 Contact Discharge**

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

Ordering Information/Selector Guide

PART	I/O $V_{L\_}$ STATE DURING SHUTDOWN	I/O $V_{CC\_}$ STATE DURING SHUTDOWN	TEMP RANGE	PIN-PACKAGE
MAX13055EEWG+	Open Drain	Open Drain	-40°C to +85°C	24 WLP
MAX13055EETI+	Open Drain	Open Drain	-40°C to +85°C	28 TQFN-EP*

Ordering Information/Selector Guide continued at end of data sheet.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

1.62V to 3.6V, 8-Channel, High-Speed LLT

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC}, V_L .....-0.3V to +4.0V
EN .....-0.3V to +4.0V
I/O $V_{CC\_}$ .....-0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$ .....-0.3V to (V_L + 0.3V)
Short-Circuit Duration
I/O to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 28.6mW/°C above +70°C) 2286mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
28-Pin TQFN .....2.7°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
24-Bump WLP .....97°C/W
28-Pin TQFN .....35°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_L Supply Range	V_L		1.62		3.2	V
V_{CC} Supply Range	V_{CC}		2.2		3.6	V
Supply Current from V_{CC}	I_{QVCC}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L			40	µA
Supply Current from V_L	I_{QVL}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L			10	µA
V_{CC} Shutdown Supply Current	$I_{SHDN-VCC}$	T_A = +25°C, EN = GND		0.1	2	µA
V_L Shutdown Mode Supply Current	$I_{SHDN-VL}$	T_A = +25°C, EN = GND		0.1	1	µA
		T_A = +25°C, EN = V_L, V_{CC} = 0V		0.1	4	
I/O Three-State Leakage Current	I_{LEAK}	T_A = +25°C, EN = GND		0.1	2	µA
EN Input Leakage Current	I_{LEAK_EN}	T_A = +25°C			1	µA
V_L - V_{CC} Shutdown Threshold High	V_{TH_H}	V_{CC} rising	0	0.1 x V_L	0.8	V
V_L - V_{CC} Shutdown Threshold Low	V_{TH_L}	V_{CC} falling	0	0.12 x V_L	0.8	V
I/O $V_{CC\_}$ Pulldown Resistance During Shutdown	$R_{VCC\_PD\_SD}$	MAX13056E/MAX13058E	10	16.5	23	kΩ
I/O $V_{L\_}$ Pulldown Resistance During Shutdown	$R_{VL\_PD\_SD}$	MAX13057E/MAX13058E	10	16.5	23	kΩ
I/O $V_{L\_}$ Pullup Current (Normal Mode)	$I_{VL\_PU\_}$	I/O $V_{L\_}$ = GND, I/O $V_{CC\_}$ = GND	20		65	µA
I/O $V_{CC\_}$ Pullup Current (Normal Mode)	$I_{VCC\_PU\_}$	I/O $V_{CC\_}$ = GND, I/O $V_{L\_}$ = GND	20		65	µA
I/O $V_{L\_}$ to I/O $V_{CC\_}$ DC Resistance	R_{IOVL_IOVCC}			3		kΩ
ESD PROTECTION						
All Ports		Human Body Model		±2		kV
I/O $V_{CC\_}$ Only		Human Body Model		±15		kV
		IEC 61000-4-2 Air-Gap Discharge, C_{VCC} = 1µF		±15		
		IEC 61000-4-2 Contact Discharge, C_{VCC} = 1µF		±8		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS						
I/O $V_{L\_}$ Input-Voltage High	V_{IHL}	(Note 4)	V_L - 0.2			V
I/O $V_{L\_}$ Input-Voltage Low	V_{ILL}	(Note 4)			0.15	V
I/O $V_{CC\_}$ Input-Voltage High	V_{IHC}	(Note 4)	V_{CC} - 0.4			V
I/O $V_{CC\_}$ Input-Voltage Low	V_{ILC}	(Note 4)			0.2	V
EN Input-Voltage High	V_{IH}		V_L - 0.4			V
EN Input-Voltage Low	V_{IL}				0.4	V
I/O $V_{L\_}$ Output-Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 10µA	4/5 V_L			V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 20µA, I/O $V_{CC\_}$ < 0.1V			1/5 V_L	V
I/O $V_{CC\_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 10µA	4/5 V_{CC}			V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 20µA, I/O $V_{L\_}$ < 0.1V			1/5	V
RISE/FALL TIME ACCELERATOR STAGE						
Accelerator Pulse Duration		On falling edge		3.5		ns
		On rising edge				
V_L Output Accelerator Source Impedance		V_L = 1.62V		24		Ω
V_{CC} Output Accelerator Source Impedance		V_{CC} = 2.2V		13		Ω
V_L Output Accelerator Source Impedance		V_L = 3.2V		11		Ω
V_{CC} Output Accelerator Source Impedance		V_{CC} = 3.6V		9		Ω
V_L Output Accelerator Sink Impedance		V_L = 1.62V		14		Ω
V_{CC} Output Accelerator Sink Impedance		V_{CC} = 2.2V		11		Ω
V_L Output Accelerator Sink Impedance		V_L = 3.2V		10		Ω
V_{CC} Output Accelerator Sink Impedance		V_{CC} = 3.6V		9		Ω

1.62V to 3.6V, 8-Channel, High-Speed LLT

TIMING CHARACTERISTICS

(+2.2V ≤ V_{CC} ≤ 3.6V, +1.62V ≤ V_L ≤ +3.2V; $C_{I/OVL\_}$ ≤ 15pF, $C_{I/OVCC\_}$ ≤ 10pF; R_{SOURCE} < 150Ω, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Figure 2			2.5	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Figure 2			2.5	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}	Figure 1			2.5	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}	Figure 1			2.5	ns
Propagation Delay (Driving I/O $V_{L\_}$)	$t_{PVL-VCC}$	Figure 2	1		6.5	ns
Propagation Delay (Driving I/O $V_{CC\_}$)	$t_{PVCC-VL}$	Figure 1	1		6.5	ns
Channel-to-Channel Skew	t_{SKEW}				2	ns
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ After EN	t_{EN-VCC}	Figure 3		5		µs
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ After EN	t_{EN-VL}	Figure 3		5		µs
Maximum Data Rate		Push-pull operation	100			Mbps
		Open drain	1			

Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions. It will not latch up.

Note 4: For input thresholds, see the rise/fall time accelerator circuit in Figure 4.

Test Circuits/Timing Diagrams

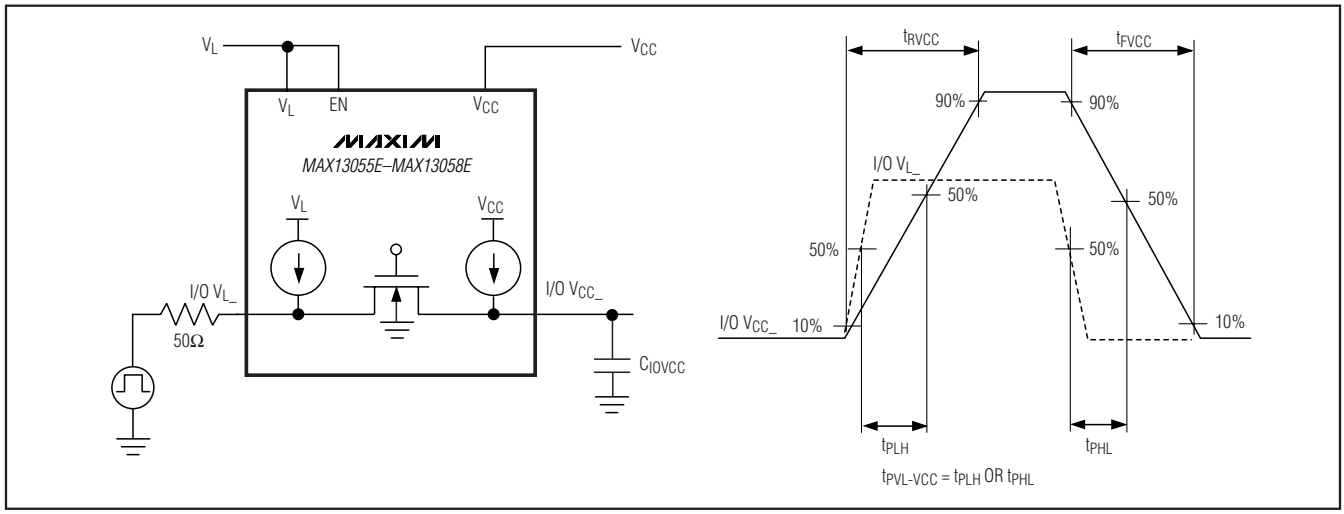


Figure 1. Push-Pull Driving I/O $V_{L\_}$ Test Circuit and Timing

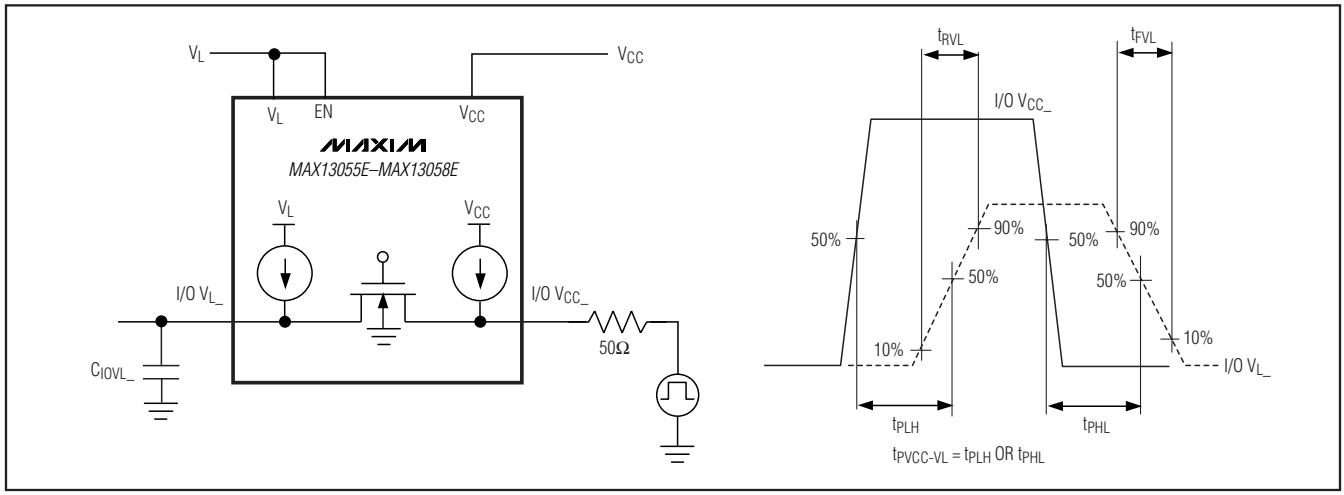


Figure 2. Push-Pull Driving I/O $V_{CC\_}$ Test Circuit and Timing

1.62V to 3.6V, 8-Channel, High-Speed LLT

Test Circuits/Timing Diagrams (continued)

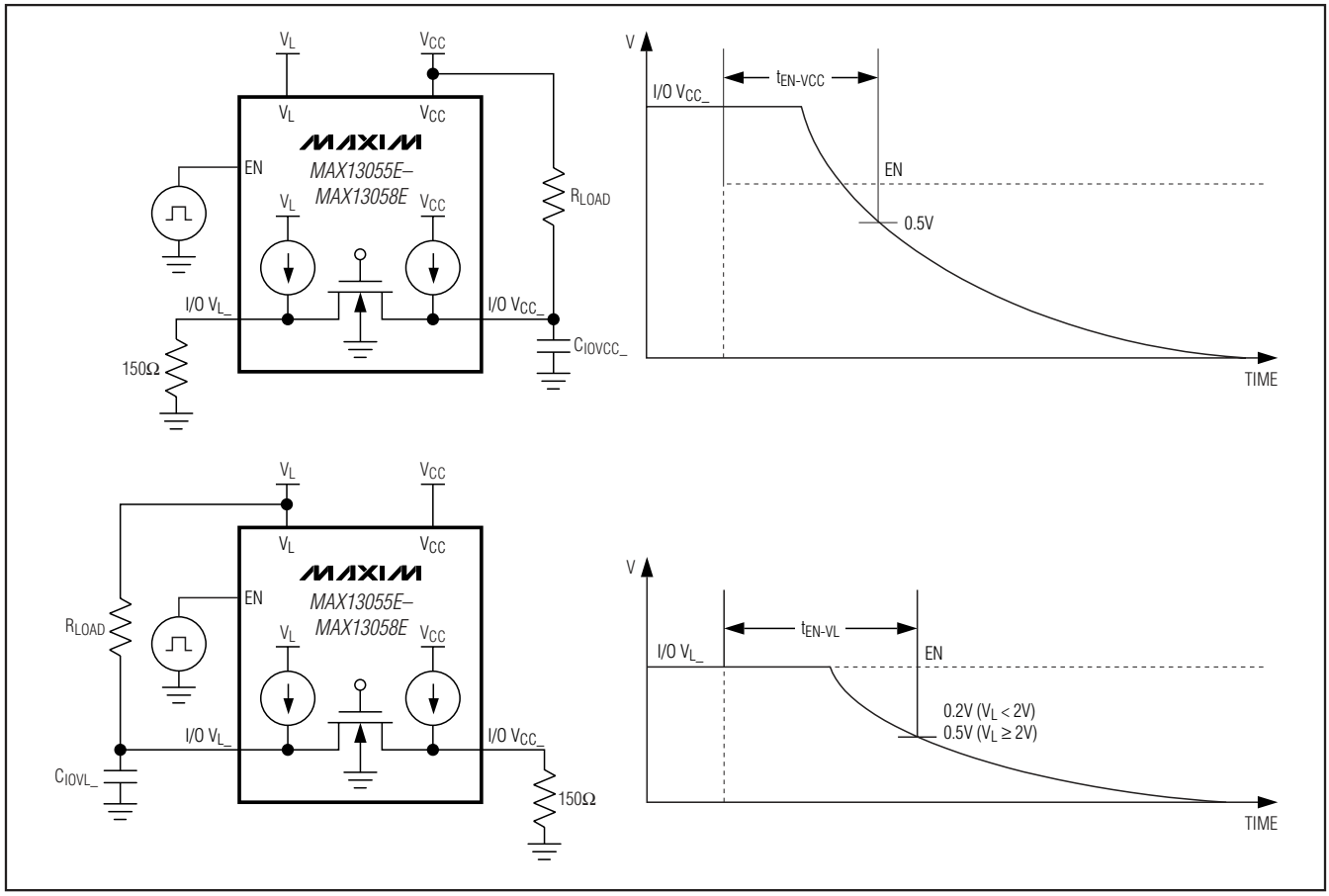
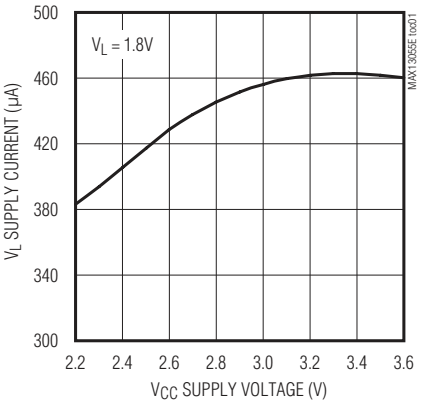


Figure 3. Enable Test Circuit and Timing

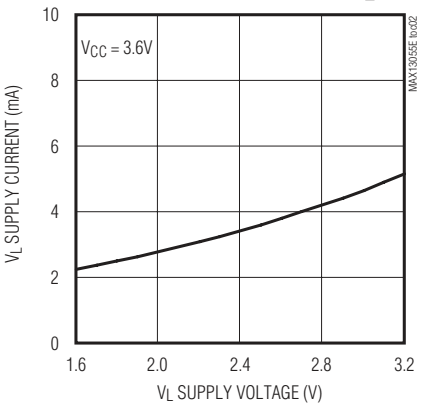
Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = +1.8V, $C_{I/OVCC\_}$ = 10pF, $C_{I/OVL\_}$ = 15pF, R_{SOURCE} = 50Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

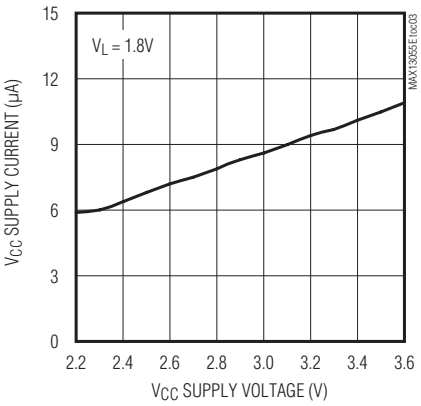
V_L SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O V_L_)



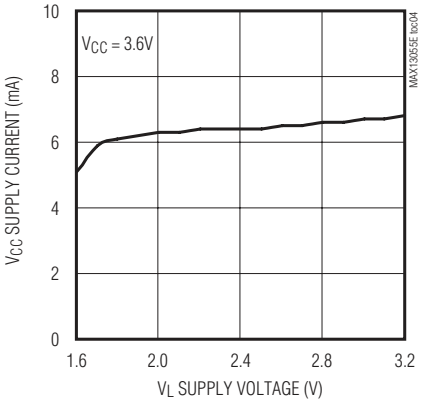
V_L SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O V_{CC}_)



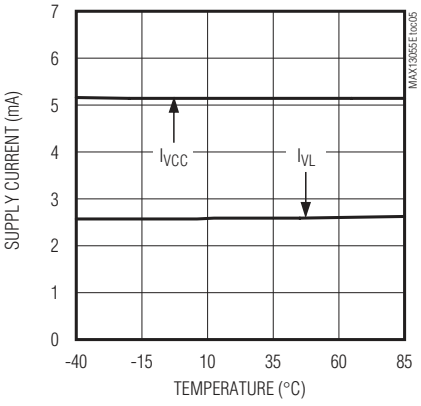
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O V_L_)



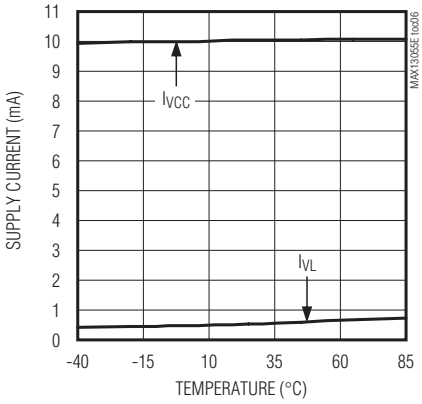
V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O V_{CC}_)



SUPPLY CURRENT vs. TEMPERATURE (DRIVING ONE I/O V_{CC}_)



SUPPLY CURRENT vs. TEMPERATURE (DRIVING ONE I/O V_L_)

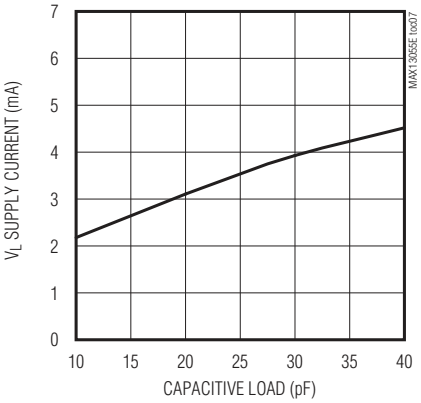


1.62V to 3.6V, 8-Channel, High-Speed LLT

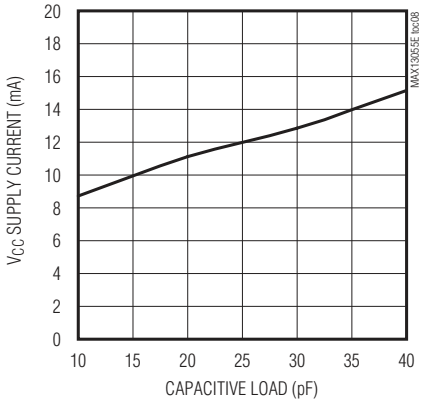
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +1.8V, $C_{I/OVCC\_}$ = 10pF, $C_{I/OVL\_}$ = 15pF, R_{SOURCE} = 50Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

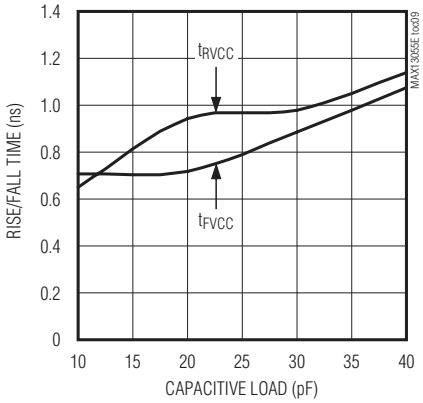
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_L_ (DRIVING ONE I/O V_{CC}_)



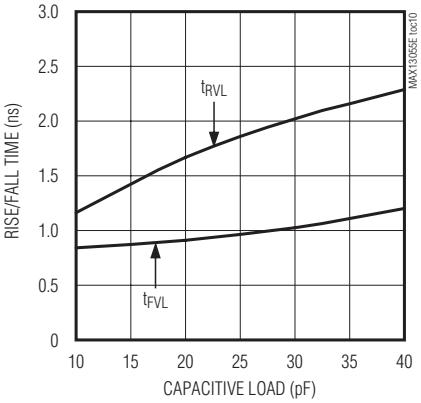
V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC}_ (DRIVING ONE I/O V_L_)



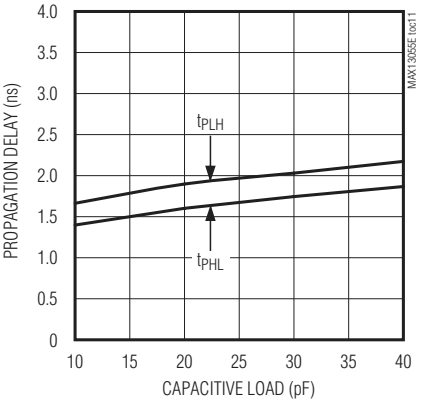
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC}_ (DRIVING I/O V_L_)



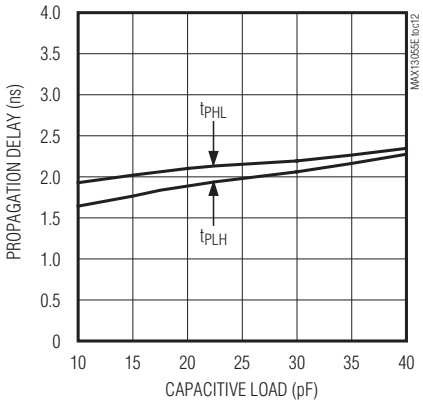
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_L_ (DRIVING I/O V_{CC}_)



PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC}_ (DRIVING I/O V_L_)



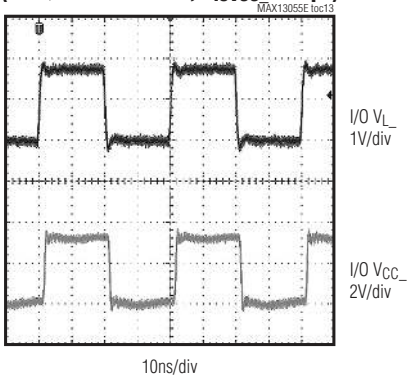
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L_ (DRIVING I/O V_{CC}_)



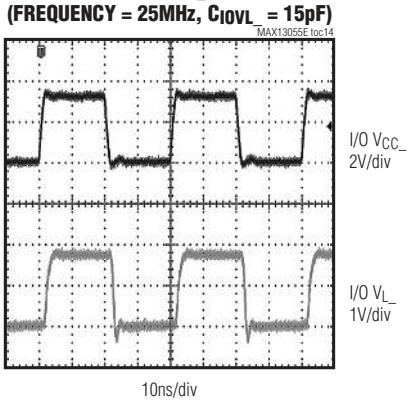
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +1.8V, $C_{I/OVCC\_}$ = 10pF, $C_{I/OVL\_}$ = 15pF, R_{SOURCE} = 50Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

TYPICAL I/O V_L_ DRIVING (FREQUENCY = 25MHz, $C_{IOVCC\_}$ = 40pF)



TYPICAL I/O V_{CC}_ DRIVING (FREQUENCY = 25MHz, $C_{IOVL\_}$ = 15pF)



Pin Description

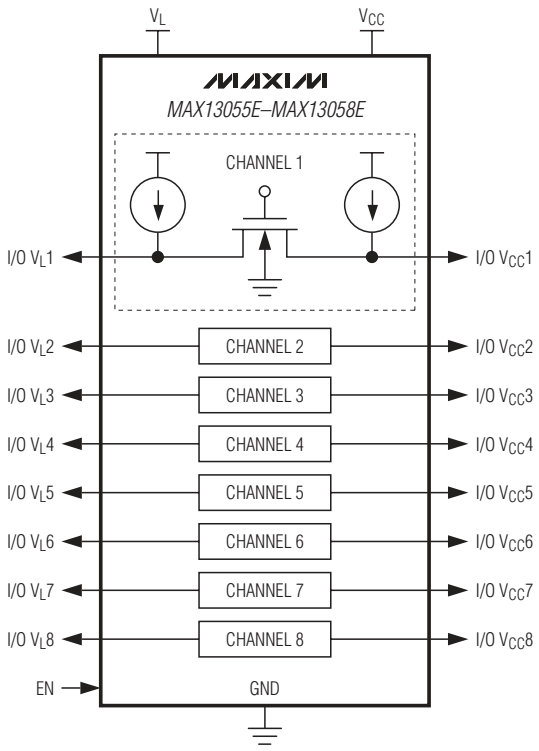
PIN		NAME	FUNCTION
TQFN-EP	WLP		
1, 12, 13, 14, 24, 25, 26, 27	—	N.C.	No Connection. N.C. is not internally connected.
2	B1	I/O V_L1	Input/Output 1 Referenced to V_L
3	A1	I/O V_L2	Input/Output 2 Referenced to V_L
4	A2	I/O V_L3	Input/Output 3 Referenced to V_L
5	A3	I/O V_L4	Input/Output 4 Referenced to V_L
6	B3, B4, B5	GND	Ground
7	A4	I/O V_L5	Input/Output 5 Referenced to V_L
8	A5	I/O V_L6	Input/Output 6 Referenced to V_L
9	A6	I/O V_L7	Input/Output 7 Referenced to V_L
10	B6	I/O V_L8	Input/Output 8 Referenced to V_L
11	C5	EN	Enable Control Input. Drive EN high for normal operation. Drive EN low for shutdown mode.
15	C6	I/O V_{CC}8	Input/Output 8 Referenced to V_{CC}
16	D6	I/O V_{CC}7	Input/Output 7 Referenced to V_{CC}
17	D5	I/O V_{CC}6	Input/Output 6 Referenced to V_{CC}
18	D4	I/O V_{CC}5	Input/Output 5 Referenced to V_{CC}
19	C2, C3, C4	V_{CC}	+2.2V to +3.6V Power-Supply Voltage. Bypass V_{CC} with 1µF and 0.1µF ceramic capacitors located as close to the device as possible.
20	D3	I/O V_{CC}4	Input/Output 4 Referenced to V_{CC}

1.62V to 3.6V, 8-Channel, High-Speed LLT

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN-EP	WLP		
21	D2	I/O $V_{CC}3$	Input/Output 3 Referenced to V_{CC}
22	D1	I/O $V_{CC}2$	Input/Output 2 Referenced to V_{CC}
23	C1	I/O $V_{CC}1$	Input/Output 1 Referenced to V_{CC}
28	B2	V_L	+1.62V to +3.2V Logic-Supply Voltage. Bypass V_L with a 0.1µF ceramic capacitor located as close to the device as possible.
—	—	EP	Exposed Pad. Connect EP to GND.

Functional Diagram



NOTE: EXTERNAL PULLUP RESISTORS NOT RECOMMENDED ON I/O LINES.

Detailed Description

The MAX13055E–MAX13058E 8-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13055E–MAX13058E are ideally suited for level translation in systems with 8 channels. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic-high signals presented on the V_L side of the device appear as a logic-high signal on the V_{CC} side of the device and vice versa.

The MAX13055E–MAX13058E operate at full speed with external drivers that source as little as 4mA output current. Each I/O channel is pulled up to V_{CC} or V_L by an internal 40µA current source, allowing the MAX13055E–MAX13058E to be driven by either push-pull or open-drain drivers.

The MAX13055E–MAX13058E feature an enable (EN) input that places the devices into a low-power shutdown mode when driven low. The MAX13055E–MAX13058E feature an automatic shutdown mode that disables the part when V_{CC} is less than V_L. The state of I/O $V_{CC\_}$ and I/O $V_{L\_}$ during shutdown is chosen by selecting the appropriate part version (see the *Ordering Information/Selector Guide*).

The MAX13055E–MAX13058E operate with V_{CC} voltages from +2.2V to +3.6V and V_L voltages from +1.62V to +3.2V.

Level Translation

For proper operation, ensure that $+2.2V \le V_{CC} \le +3.6V$, $+1.62V \le V_L \le V_{CC} - 0.2V$. When power is supplied to V_L while V_{CC} is missing or less than V_L, the MAX13055E–MAX13058E automatically enter a low-power mode. The devices also enters shutdown mode when V_{EN} = 0V. This allows V_{CC} to be disconnected and still have a known state on I/O $V_{L\_}$. The maximum data rate depends heavily on the load capacitance (see the Rise/Fall Time vs. Capacitive Load graphs in the *Typical Operating Characteristics*), output impedance of the driver, and the operating voltage range.

Input Requirements

The MAX13055E–MAX13058E architecture is based on an nMOS pass gate and rise/fall time accelerator stages (Figure 4). The accelerators are active only when there is a rising/falling edge on a given I/O. A short pulse is then generated where the output accelerator stages become active and charges/discharges the capacitance at the I/Os. Due to its architecture, both input stages become active during the one-shot pulse. This can lead to current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

The MAX13055E–MAX13058E have internal current sources capable of sourcing 40µA to pull up the I/O lines. These internal pullup current sources allow the inputs to be driven with open-drain drivers as well as push-pull drivers. It is not recommended to use external pullup resistors on the I/O lines. The architecture of the MAX13055E–MAX13058E permits either side to be driven with a minimum of 4mA drivers or larger.

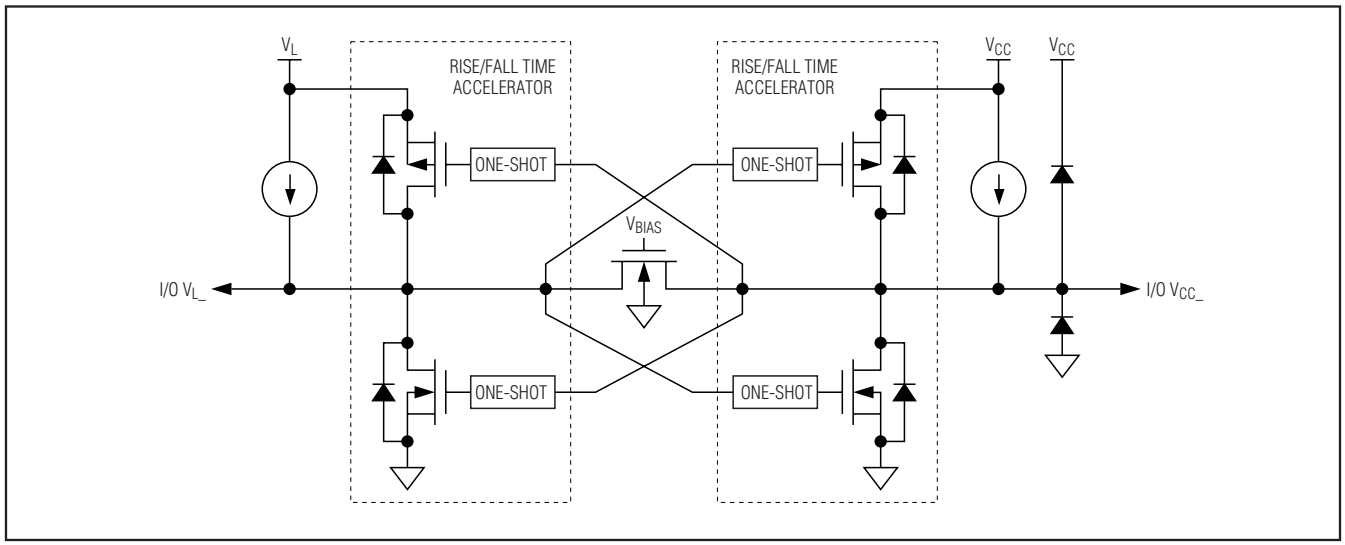


Figure 4. Simplified Functional Diagram for One I/O Line

Output Load Requirements

The MAX13055E–MAX13058E I/O are designed to drive CMOS inputs. Do not load the I/O lines with a resistive load less than 25kΩ. Do not place an RC circuit at the input of these devices to slow down the edges. If a slower rise/fall time is required, refer to the MAX3000E/MAX3001E logic-level translator data sheet.

Shutdown Mode

The MAX13055E–MAX13058E feature an enable (EN) input that places the devices into a low-power shutdown mode when driven low. The MAX13055E–MAX13058E feature an automatic shutdown mode that disables the part when V_{CC} is unconnected or less than V_L.

Applications Information

Layout Recommendations

Use standard high-speed layout practices when laying out a board with the MAX13055E–MAX13058E. For example, to minimize line coupling, place all other signal lines not connected to the MAX13055E–MAX13058E at least 1x the substrate height of the PCB away from the input and output lines of the MAX13055E–MAX13058E.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L and V_{CC} to ground with 0.1µF ceramic capacitors. Place all capacitors as close to the power-supply inputs as possible. For full ESD protection, bypass V_{CC} with a 1µF ceramic capacitor located as close to the V_{CC} input as possible.

Unidirectional vs. Bidirectional Level Translator

The MAX13055E–MAX13058E bidirectional level translators can operate as a unidirectional device to translate signals without inversion. These devices provide a small solution for unidirectional level translation without inversion.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Use with External Pullup/Pulldown Resistors

Due to the architecture of the MAX13055E–MAX13058E, it is not recommended to use external pullup or pulldown resistors on the bus. In certain applications, the use of external pullup or pulldown resistors is desired to have a known bus state when there is no active driver on the bus. The MAX13055E–MAX13058E include internal pullup current sources that set the bus state when the device is enabled. In shutdown mode, the state of I/O $V_{CC\_}$ and I/O $V_{L\_}$ is dependent on the selected part version (see the *Ordering Information/Selector Guide*).

Open-Drain Signaling

The MAX13055E–MAX13058E are designed to pass open-drain as well as CMOS push-pull signals. When used with open-drain signaling, the rise time is dominated by the interaction of the internal pullup current source and the parasitic load capacitance. The MAX13055E–MAX13058E include internal rise-time accelerators to speed up transitions, eliminating any need for external pullup resistors. For applications such as I^2C or 1-Wire® that require an external pullup resistor, refer to the MAX3378E and MAX3396E data sheets.

Human Body Model

Figure 5a shows the Human Body Model and Figure 5b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX13055E–MAX13058E help in designing equipment that meets level 4 (the highest level) of IEC 61000-4-2, without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2, because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 6a shows the IEC 61000-4-2 model and Figure 6b shows the current waveform for the ±8kV, IEC 61000-4-2, level 4, ESD Contact Discharge Method.

The Air Gap Method involves approaching the device with a charged probe. The Contact Discharge Method connects the probe to the device before the probe is energized.

Chip Information

PROCESS: CMOS

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

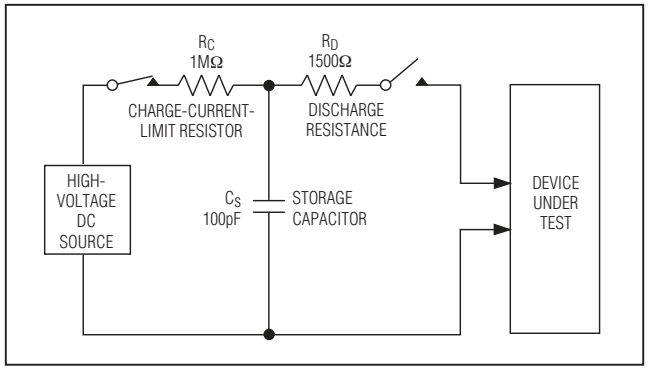


Figure 5a. Human Body ESD Test Model

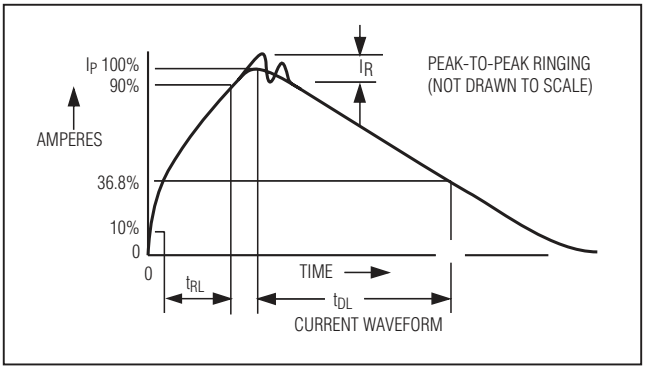


Figure 5b. Human Body Current Waveform

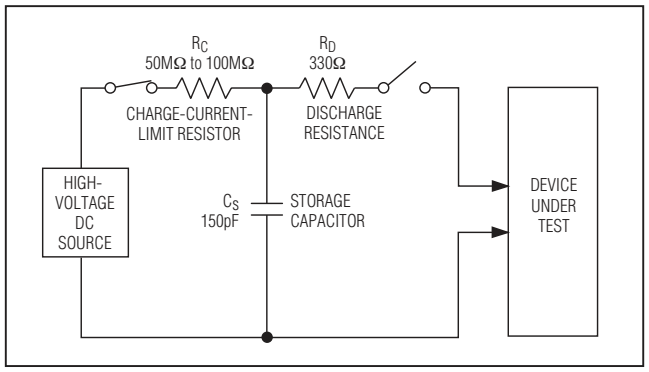


Figure 6a. IEC 61000-4-2 ESD Test Model

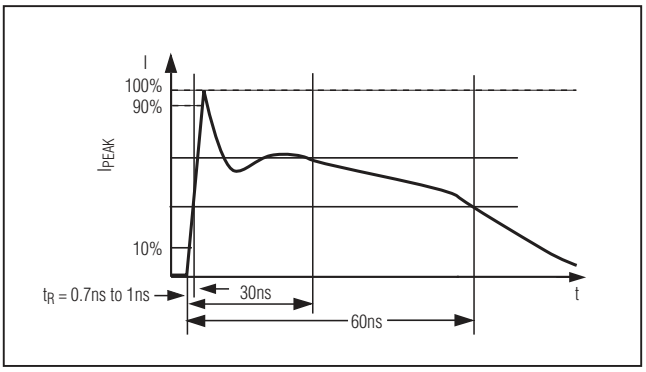


Figure 6b. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information/Selector Guide (continued)

PART	I/O $V_{L\_}$ STATE DURING SHUTDOWN	I/O $V_{CC\_}$ STATE DURING SHUTDOWN	TEMP RANGE	PIN-PACKAGE
MAX13056EEWG+**	Open Drain	10kΩ to GND	-40°C to +85°C	24 WLP
MAX13056EETI+**	Open Drain	10kΩ to GND	-40°C to +85°C	28 TQFN-EP*
MAX13057EEWG+**	10kΩ to GND	Open Drain	-40°C to +85°C	24 WLP
MAX13057EETI+**	10kΩ to GND	Open Drain	-40°C to +85°C	28 TQFN-EP*
MAX13058EEWG+	10kΩ to GND	10kΩ to GND	-40°C to +85°C	24 WLP
MAX13058EETI+	10kΩ to GND	10kΩ to GND	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

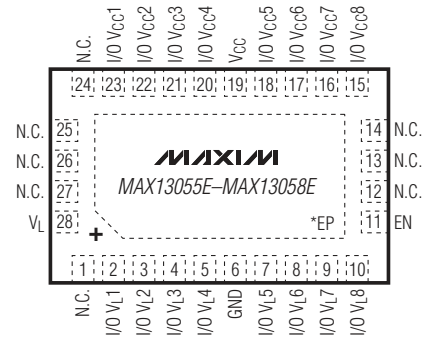
**EP = Exposed pad.*

***Future product—contact factory for availability.*

1.62V to 3.6V, 8-Channel, High-Speed LLT

Pin Configurations

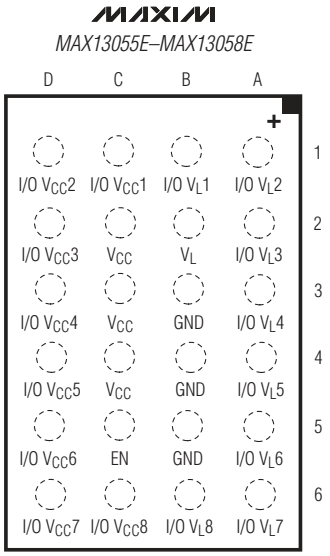
TOP VIEW



TQFN

*CONNECT EXPOSED PAD TO GND.

TOP VIEW
(BUMPS ON BOTTOM)



WLP

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 WLP	W241B2-1	**21-0219**
28 TQFN	T283555-1	**21-0184**