Features

Mar 2006

- Performs ASK (amplitude shift keyed) modulation and demodulation
- 32 kHz carrier frequency
- Up to 2 kbit/s full duplex data transfer rate
- On-chip oscillator
- On-chip tone caller for alerting functions
- Adjustable tone caller frequencies
- Selectable self-loop test mode
- 5V/2.5mA power supply
- ISO^2-CMOS and switched capacitor technologies
- 18 Pin DIP

Applications

- Simultaneous data and voice communication in PABXs
- 2 kbit/s data modem
- "Smart" telephone sets

Ordering Information

MT8840AE	18 Pin PDIP	Tubes
MT8840AS	18 Pin SOIC	Tubes
MT8840ASR	18 Pin SOIC	Tape & Reel
MT8840AE1	18 Pin PDIP*	Tubes
MT8840ASR1	18 Pin SOIC*	Tape & Reel

* Pb Free Matte Tin

0°C to +85°C

Description

The MT8840 is a carrier over voice modem which allows simultaneous transfer of voice and data over a single pair of wires. Data is transferred on an amplitude shift keyed (ASK) 32 kHz carrier. On-chip filters remove voice frequency signals from the received composite voice and data signal prior to demodulation. The modulating signal is a bit stream with a typical data rate of 2 kbit/s. In addition, the device contains a two tone warbler which functions as a telephone ringer. The device is fabricated in Zarlink's double-poly ISO^2-CMOS technology utilizing switched-capacitor techniques.

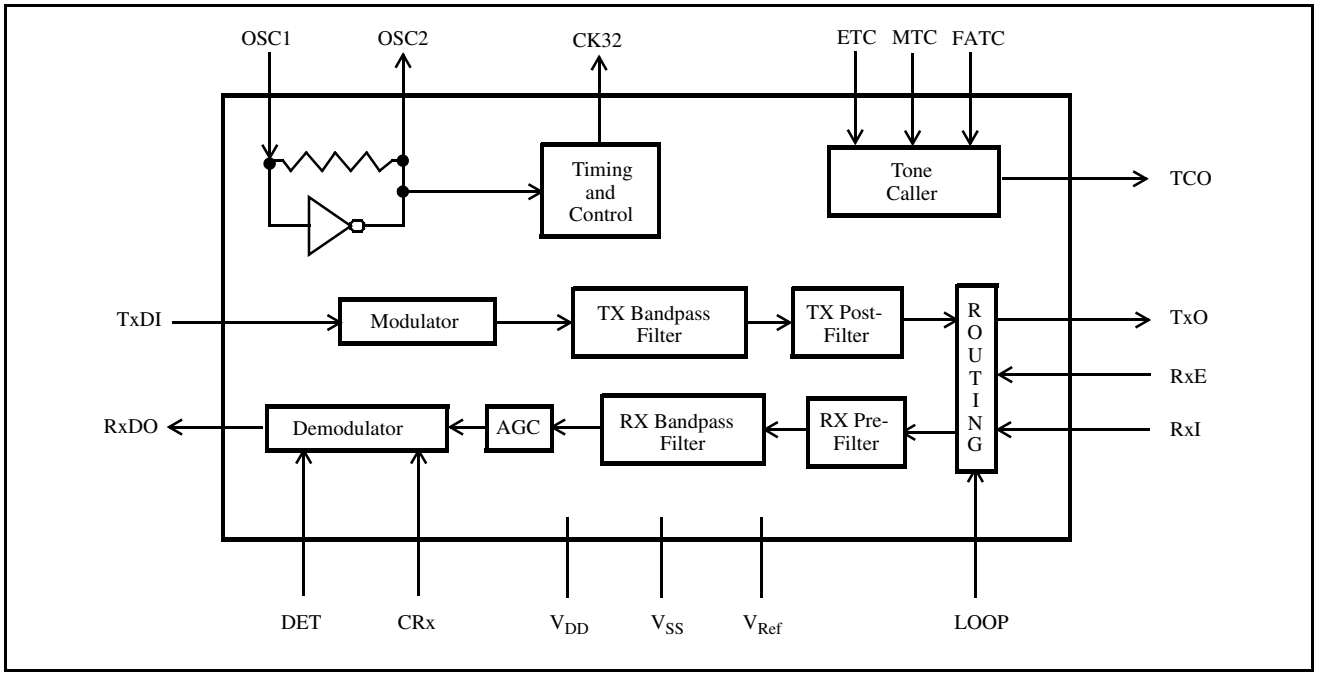
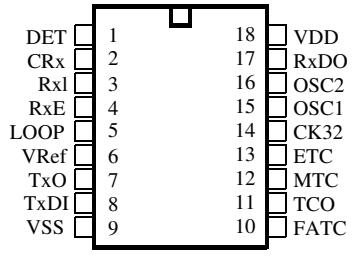


Figure 1 - Functional Block Diagram



18 PIN PLASTIC DIP/SOIC

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description	
1	DET	Demodulator detection level adjust input (Analog). Internal resistor divider applies 2.36 V in open circuit condition. Connection of external resistor will vary detect level.	
2	CRx	External AGC time constant adjust input (Analog). Connect external capacitor to V_{SS}.	
3	RxI	Modulated receive signal input (Analog). Biased at V_{Ref}.	
4	RxE	Receive enable input (Digital) with internal pull up. Active high.	
5	LOOP	Self-test mode select input (Digital) with internal pull down. Active high.	
6	V_{Ref}	Internal reference supply voltage input (Analog) .	
7	TxO	Modulated transmit carrier output (Analog).	
8	TxDI	Transmit data input (Digital).	
9	V_{SS}	Negative power supply.	
10	FATC	Tone caller center frequency adjust input (Analog).	
11	TCO	Tone caller output (Digital).	
12	MTC	Mute tone caller input (Digital) with internal pull down. Active high.	
13	ETC	Enable tone caller input (Digital) with internal pull down. Active high.	
14	CK32	32 kHz data strobe output (Digital).	
15	OSC1	Clock Input	3.579545 MHz crystal connected between these pins completes internal oscillator.
16	OSC2	Clock Output to drive external devices.	
17	RxDO	Receive data output (Digital). Synchronized to CK32.	
18	V_{DD}	Positive power supply.	

Functional Description

The MT8840 contains the modulator and demodulator circuitry for 32 kHz ASK signalling as well as a two-tone warbler (tone caller) to replace the function of the mechanical telephone ringer.

A 32 kHz carrier is 100% amplitude modulated by the digital bit stream applied to input TxDI. This results in an amplitude shift keyed (ASK) 32 kHz carrier. A logical high at TxDI disables the carrier and a logical low enables it. The digitally modulated waveform is shaped by the Tx BANDPASS FILTER and smoothed by the Tx POST FILTER. The signal then enters the routing block where it is transferred to the TxO output.

The modulated 32 kHz receive signal is applied to RxI. With a logical low applied to LOOP and a logical high applied to RxE, receive signals are routed to the Rx PREFILTER. High frequencies are removed by the Rx PREFILTER to prevent aliasing in the switched capacitor Rx BANDPASS FILTER. Voice signals are removed by the bandpass filter which is followed by an AGC circuit. This provides a dynamic range of 20 dB for the receiver. An external 1 μF capacitor connected from CRx to V_{SS} is required to control the AGC attack and decay time constants. Data is recovered from the received signal in the demodulator. The minimum voltage level to which the demodulator responds may be adjusted by connecting a resistor from DET to V_{DD} or V_{Ref}. Since DET is the input to a comparator, noise should be kept to a minimum at this pin. The recovered receive data is synchronized to the leading edge of the 32 kHz clock (available at CK32) before appearing at RxDO.

When in loop around mode, the Rx PREFILTER input is internally disconnected from the RxI input pin and connected to TxO. The transmitter output is still available at TxO.

A two tone warbling audio signal is available at TCO when the tone caller enable input (ETC) is high. TCO is internally clamped to V_{Ref} when the tone caller is disabled. The tone output can be attenuated by 20 dB if a logical high is applied to the tone caller mute input (MTC).

Applications

Figures 3 through 5 show how the MT8840 may be utilized to transfer data and voice simultaneously over a single pair of wires in digital or analog PABXs and "smart" telephone sets. In all three figures a microprocessor sends/receives data to/from the MT8840 via a UART which converts the data format from parallel-to-serial or serial-to-parallel for the transmit and receive directions, respectively. In the receive direction the MT8840 has on-board filters to reject voice-band signals leaving only the 32 kHz carrier. This carrier is then demodulated to recover the received data. In the transmit direction the data to be sent is modulated and passed on to a summing circuit which sums the modulated 32 kHz carrier and voiceband signals for transmission over the telephone line. In the PABX the Filter/Codec has filters which reject the 32 kHz carrier from the received composite voice and data signal allowing only voiceband signals to pass through which are then PCM encoded for digital switching. However, in both the analog PABX and smart telephone set, lowpass filters could be included to bandlimit the received signal leaving only voice signals to be passed on to the switch array or handset earpiece.

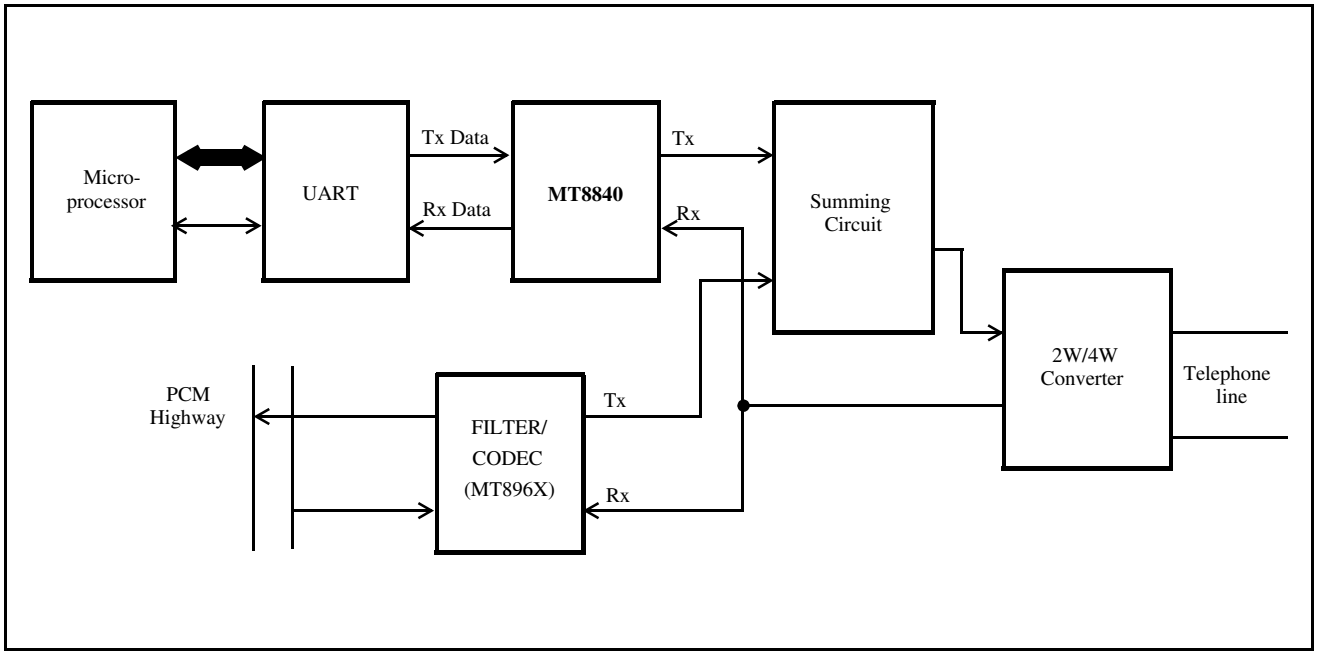


Figure 3 - Digital PABX Block Diagram

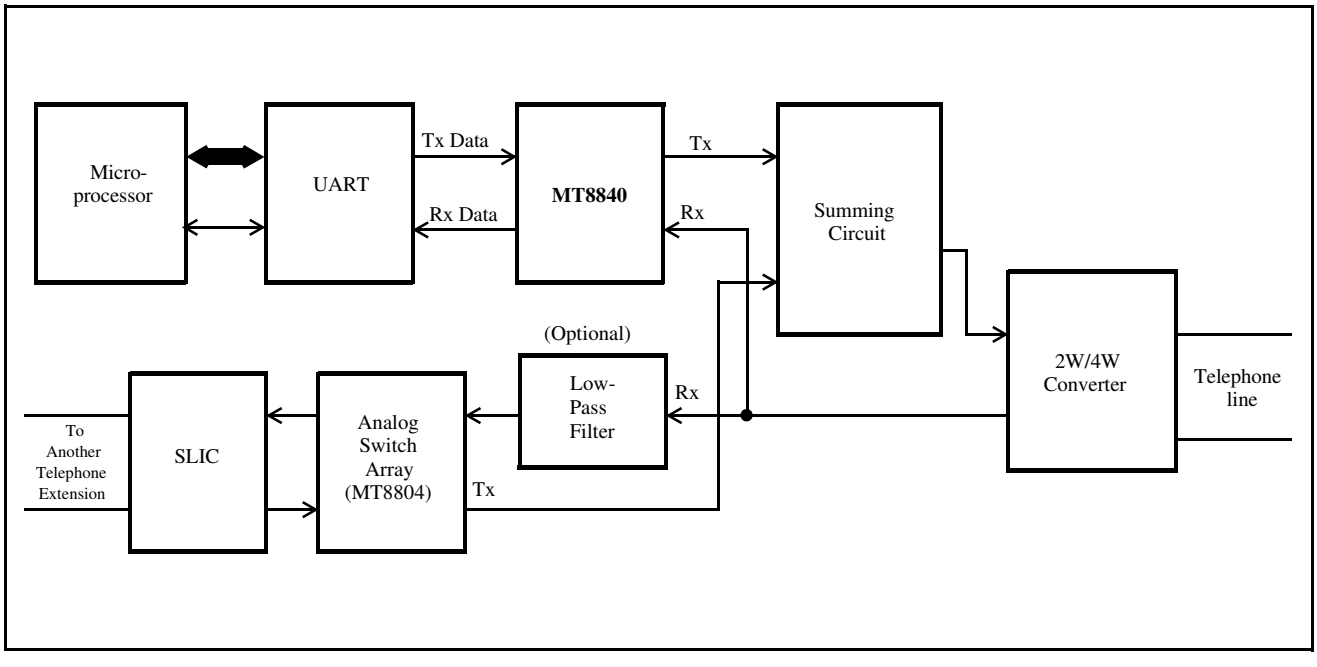


Figure 4 - Analog PABX Block Diagram

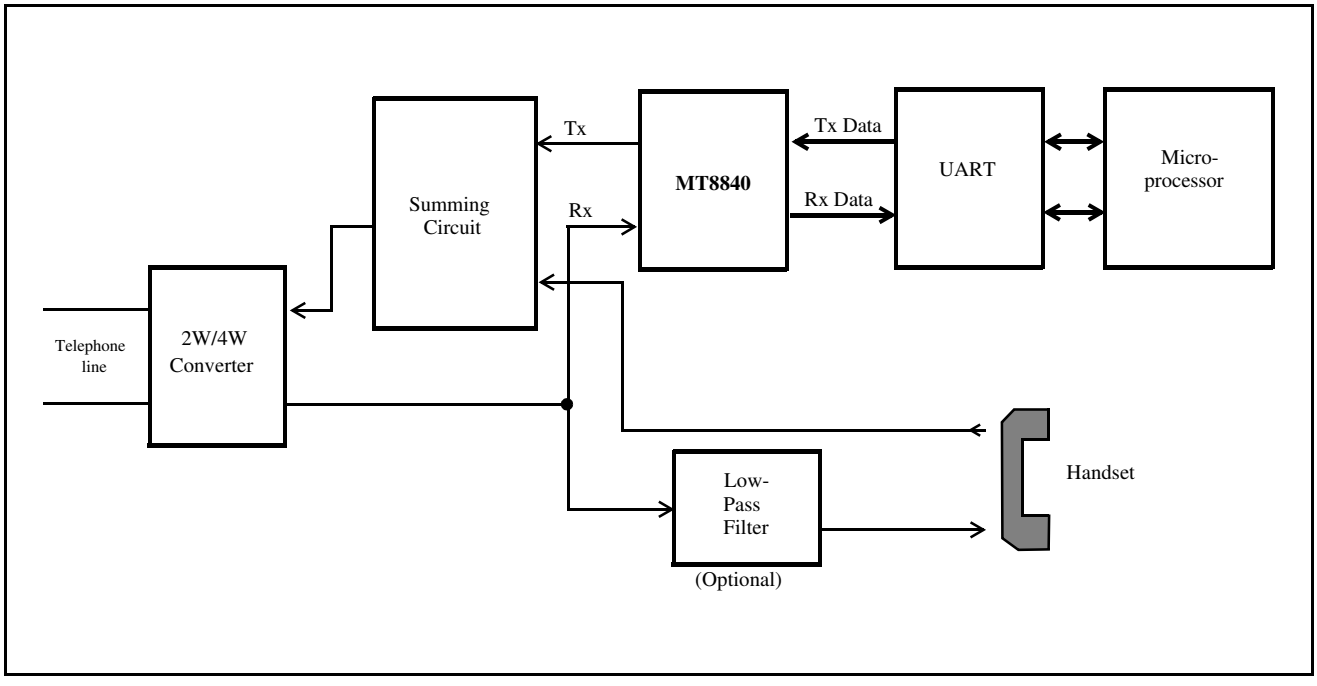
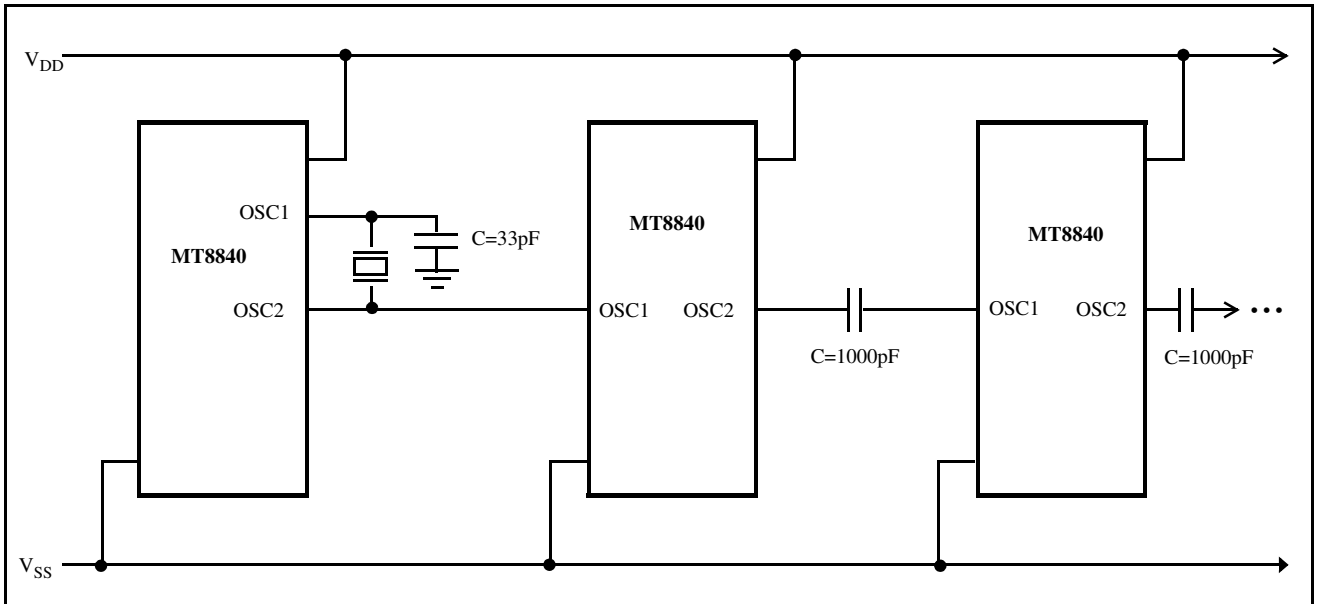


Figure 5 - Smart Telephone Set Block Diagram



When a single crystal is shared among a number of MT8840 devices, OSC1 and OSC2 should be a.c. coupled with a 1000 pF capacitor as shown above. This capacitor is not needed between the device with the crystal and the first driven device. A capacitor should be used in the first stage whenever such a chain of devices is driven from a clock instead of a crystal. A 33 pF capacitor should be connected between OSC1 and VSS to compensate for the load on OSC2.

Figure 6 - Crystal Oscillator Connections for Driving Multiple MT8840s

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Unit
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	+7.0	V
2	Voltage On Any Pin	V_{Max}	V_{SS}-0.3	V_{DD}+0.3	V
3	Current On Any Pin	I_{Max}		20	mA
4	Storage Temperature	T_S	-65	+150	°C
5	Package Power Dissipation	P_{Diss}		850	mW

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Parameter	Symbol	Min.	Typ.	Max.	Unit
1	Operating Supply Voltages	V_{DD}	4.75	5	5.25	V
2		V_{Ref}		0.4V_{DD}		V
3	Operating Supply Currents	I_{DD}		2.5	5.0	mA
4		I_{Ref}			200	µA
5	Operating Temperature	T_O	0		+85	°C
6	Load Capacitance (TxO)	C_L			50	pF
7	Load Resistance (TxO)	R_L	10			KΩ

D.C. Characteristics - V_{DD} = 5.0 V ± 5% V_{SS} =0V T = 0 - 85°C (All voltages are referenced to V_{SS} /GND)

		Characteristics	Sym.	Min.	Typ.	Max.	Unit	Test Conditions
1	DIGITAL I/O	Input Current	I_{IN}			±10	µA	V_{IN} = 0 to V_{DD}
2		Input Low Voltage	V_{IL}	0		1.5	V	
3		Input High Voltage	V_{IH}	3.5		5.0	V	
4		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 0.4mA
5		Output High Voltage	V_{OH}	4.6			V	I_{OH} = 0.4mA
6		Output Drive Current						
7		N Channel Sink (Except OSC2)	I_{OL}	0.4			mA	V_{OL} = 0.4V
8		OSC2		0.1			mA	
9		P Channel Source (Except OSC2)	I_{OH}	0.4			mA	V_{OH} = 4.6V
10		OSC2		0.1			mA	
11	ANALOG I/O	Input Current (RxI, FATC)	I_{IN}			±10	µA	V_{IN} = 0 to 5.0V
12		Input Resistance (FATC)	R_{IN}	500			KΩ	
13		(DET to V_{DD})			170		KΩ	
14		(DET to V_{Ref})			23		KΩ	
15		Input Capacitance (RxI)	C_{IN}		50		pF	
16		(FATC)			10		pF	
17		Any Digital Input			5.0	7.5	pF	
18		Output Resistance (TxO)	R_O		100		Ω	
19		(TCO)			3		KΩ	MTC = 0
20		(TCO)			30		KΩ	MTC = 1
21		Output Offset Voltage (TxO)	V_O		±25	±200	mV	
22		Output Voltage (DET)	V_O	2.20	2.36	2.55	V	See Note 1

Notes: 1. Voltage specified is generated internally and measured with no external components connected to DET

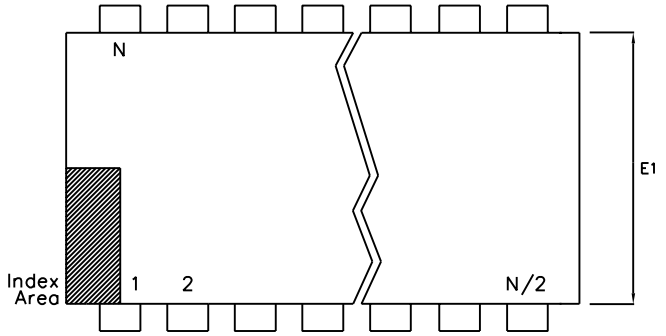
A.C. Characteristics - V_{DD}=5.0V±5% V_{SS}=0V T=0 - 85°C (All voltages are referenced to V_{SS}/GND)

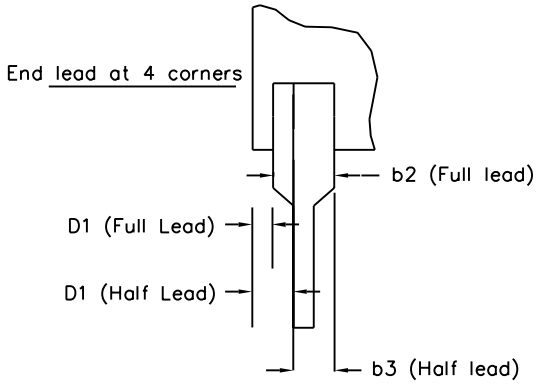
		Characteristics	Sym.	Min.	Typ.	Max.	Unit	Test Conditions
1	DIGITAL I/O	Crystal/Clock Frequency	f_C	3.5759	3.5795	3.5831	MHz	OSC1, OSC2
2		Clock Input (OSC 1)						
3		Rise Time	t_{LHCI}			100	ns	10% - 90% of (V_{DD} - V_{SS})
4		Fall Time	t_{HLCI}			100	ns	
5		Duty Cycle	DC_{CI}	40	50	60	%	
6		Clock Output (OSC 2)						
7		Rise Time	t_{LHCO}		100		ns	C_L = 30pF, 3.58MHz ext.
8		Fall Time	t_{HLCO}		100		ns	clock to OSC1
9		Duty Cycle	DC_{CO}		50		%	
10		Capacitive Load	C_{LCO}			30	pF	
11		Clock Output (CK32)	F_{C32}	32508	32541	32574	Hz	fc = 3.5795MHz
12		Rise Time	t_{LH32}		100		ns	10% - 90% of (V_{DD} - V_{SS})
13		Fall Time	t_{HL32}		100		ns	C_L = 100pF
14		Duty Cycle	DC_{32}		50		%	
15		Capacitive Load	C_{L32}			100	pF	
16	TONE CALLER	Warbler Frequency (TCO)	f_W	7.935	7.945	7.955	Hz	fc = 3.5795MHz ± 0.1%
17		Low Tone Frequency	f_{LT}	352	390	428	Hz	FATC = 0, f_c= 3.5795MHz
18				1036	1148	1260	Hz	FATC = V_{DD}, f_c= 3.5795MHz
19		High Tone Frequency	f_{HT}	440	487	535	Hz	FATC = 0, f_c= 3.5795MHz
20				1295	1434	1574	Hz	FATC = V_{DD}, f_c= 3.5795MHz
21		Harmonic Relationship	f_{HT}/f_{LT}		1.25			
22		Warbler Output (TCO)						
23		Rise Time	t_{LHWO}		500		ns	100KΩ load to V_{Ref}
24		Fall Time	t_{HLWO}		500		ns	C_L = 30pF, MTC = 0
25		Duty Cycle	DC_{WO}		50		%	
26		Output Level (TCO)	V_{TCC}		V_{DD}		V_{pp}	MTC = 0
27					0.625		V_{pp}	MTC = 1 (100KΩ load to V_{Ref})
28	MODULATOR	Modulated Frequency	f_{MOD}		32541		Hz	
29		Output Level (TxO)	V_{TxO}	225	250	270	mV_{pp}	V_{DD} = 5V
30		Output Level (TxO)						
31		variation vs. V_{DD}	V_{TxO}		100		%	
32		Transmit Data Input (TxDI)						
33		Rise Time	t_{LHTxDI}			100	ns	
34		Fall Time	t_{HLTxDI}			100	ns	
35		Data Rate (TxDI)	f_{Data}		2		k/bits	See Note 1

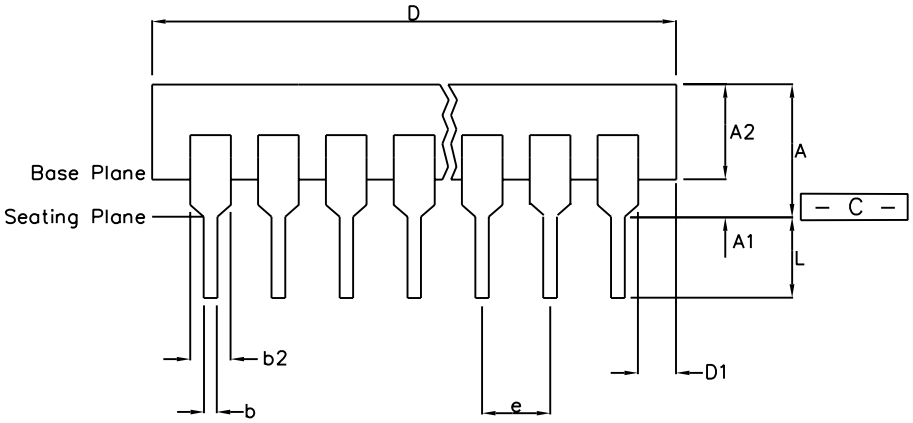
A.C. Characteristics - V_{DD}=5.0V±5% V_{SS}=0V T=0 - 85°C (All voltages are referenced to V_{SS}/GND)

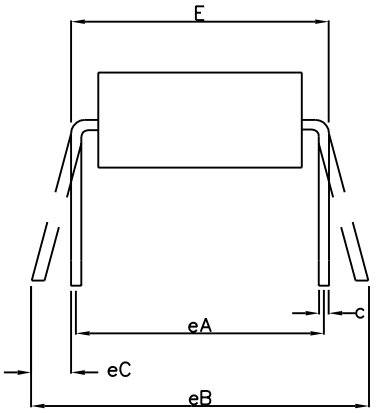
		Characteristics	Sym.	Min.	Typ.	Max.	Unit	Test Conditions
36	DEMODULATOR	Input Impedance (RxI)	Z_{IN}		50		KΩ	32 kHz Input Frequency
37		Valid Input Level - Data (RxI)	V_{RxI}	40		400	mV_{pp}	See Note 2
38		Valid Input Level - Data + Voice	V_{RxI}			3.0	V_{pp}	
39		Receive Data Output (RxDO)	f_{Data}		2		kbit/s	
40		Rise Time			100		ns	10% - 90% of (V_{DD} - V_{SS})
41		Fall Time			100		ns	C_L = 100pF
42		Capacitive Load				100	pF	
43		Duty Cycle		40	50	60	%	
44	DEMOD	Inband Noise Rejection (S/N)		12			dB	Input Sig. (RxI) = 400mV_{pp}
45		Attenuation to Voice Signals		40			dB	f_{in} = 0 - 5KHz
46		Detect Filter Q	Q		3.8			
47		Detector Center Frequency			32		kHz	

Notes: 1. All A.C. parameters are based on a typical data rate of 2 kbit/s.
2. Measured with no external resistor to DET input. Detection level internally set to 2.36 V typical.









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	22.35	23.37	0.880	0.920
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	18		18	
Conforms to Jedec MS-001AC Issue D				

Notes:
1. Leadframe Material: Copper
2. Leadframe finish: Solder Plate
3. Dimensions D, D1 & E1 do not include mould flash or protrusions.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
5. Dimensions eB & eC are measured with the leads unconstrained
6. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
7. N is the maximum of terminal positions.

This drawing supersedes: –
Plymouth/Swindon drawing # 418/ED/39502/004

ISSUE	1	2		
ACN	202563	212483		
DATE	9Jun97	5Apr02		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
DP / E

Package Code DA

Package Outline for
18 Lead PDIP

GPD00348

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