

HEXFET® Power MOSFET

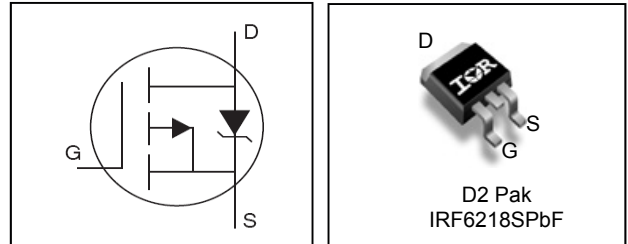
Applications

- Reset Switch for Active Clamp Reset DC-DC converters

V_{DSS}	$R_{DS(on)}$ (max)	I_D
-150V	150mΩ @ $V_{GS} = -10V$	-27A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current
- Lead-Free



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF6218SPbF	D2-Pak	Tube	50	IRF6218SPbF
		Tape and Reel Left	800	IRF6218STRLPbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-150	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	- 27	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-19	
I_{DM}	Pulsed Drain Current ①	- 110	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	250	W
	Linear Derating Factor	1.6	W/°C
dv/dt	Peak Diode Recovery dv/dt③	8.2	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}			

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.61	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑥	—	40	

Notes ① through ⑥ are on page 2

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-150	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.17	—	V/°C	Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	120	150	mΩ	V _{GS} = -10V, I _D = -16A ④
V _{GS(th)}	Gate Threshold Voltage	-3.0	—	-5.0	V	V _{DS} = V _{GS} , I _D = -250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -120V, V _{GS} = 0V
		—	—	-250		V _{DS} = -120V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} = 20V

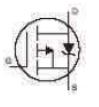
Dynamic @ T_J = 25°C (unless otherwise specified)

g _{fs}	Forward Trans conductance	11	—	—	S	V _{DS} = -50V, I _D = -16A
Q _g	Total Gate Charge	—	71	110	nC	I _D = -16A
Q _{gs}	Gate-to-Source Charge	—	21	—		V _{DS} = -120V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	32	—		V _{GS} = -10V ④
t _{d(on)}	Turn-On Delay Time	—	21	—	ns	V _{DD} = -75V
t _r	Rise Time	—	70	—		I _D = -16A
t _{d(off)}	Turn-Off Delay Time	—	35	—		R _G = 3.9Ω
t _f	Fall Time	—	30	—		V _{GS} = -10V ④
C _{iss}	Input Capacitance	—	2210	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	370	—		V _{DS} = -25V
C _{riss}	Reverse Transfer Capacitance	—	89	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	2220	—		V _{GS} = 0V, V _{DS} = -1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	170	—		V _{GS} = 0V, V _{DS} = -120V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	340	—		V _{GS} = 0V, V _{DS} = 0V to -120V

Avalanche Characteristics

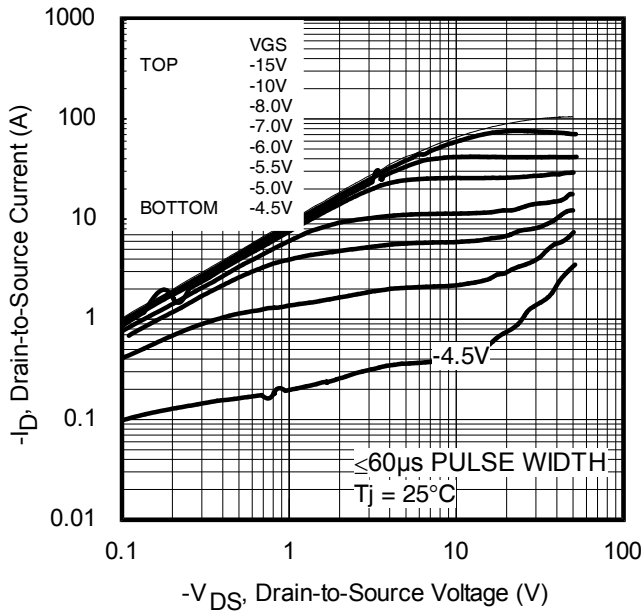
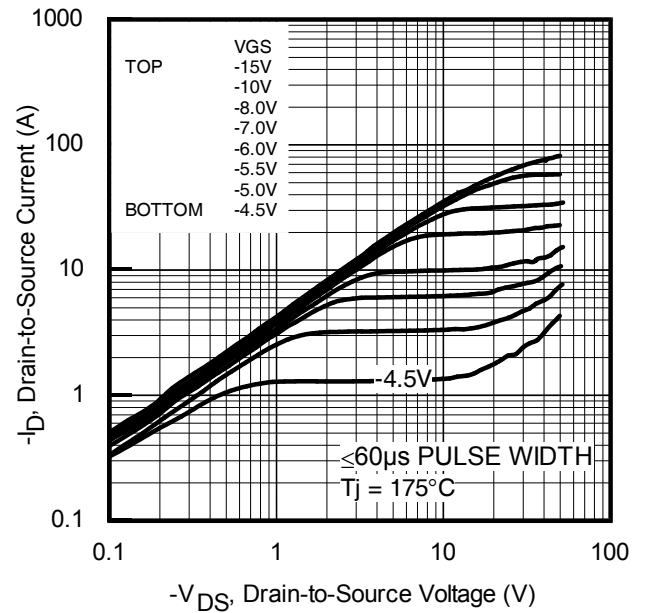
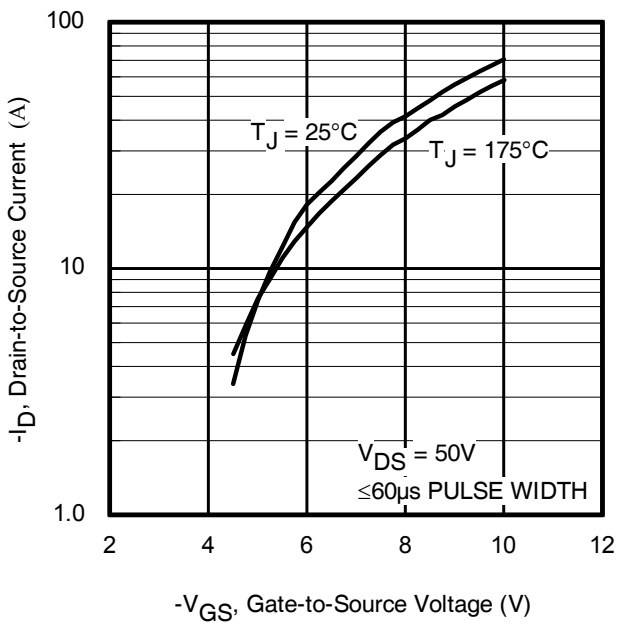
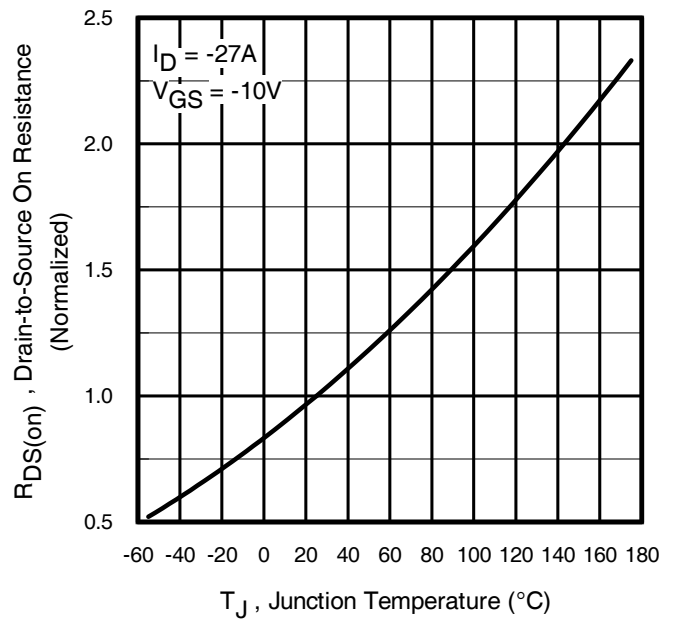
	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	210	mJ
I _{AR}	Avalanche Current ①	—	-16	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-27	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-110		
V _{SD}	Diode Forward Voltage	—	—	-1.6	V	T _J = 25°C, I _S = -16A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	150	—	ns	T _J = 25°C, I _F = -16A, V _{DD} = -25V
Q _{rr}	Reverse Recovery Charge	—	860	—	nC	di/dt = 100A/μs ④

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② starting T_J = 25°C, L = 1.6mH, R_G = 25Ω, I_{AS} = -17A
- ③ I_{SD} ≤ -17A, di/dt ≤ -520A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ R_θ is measured at T_J of approximately 90°C.
- ⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

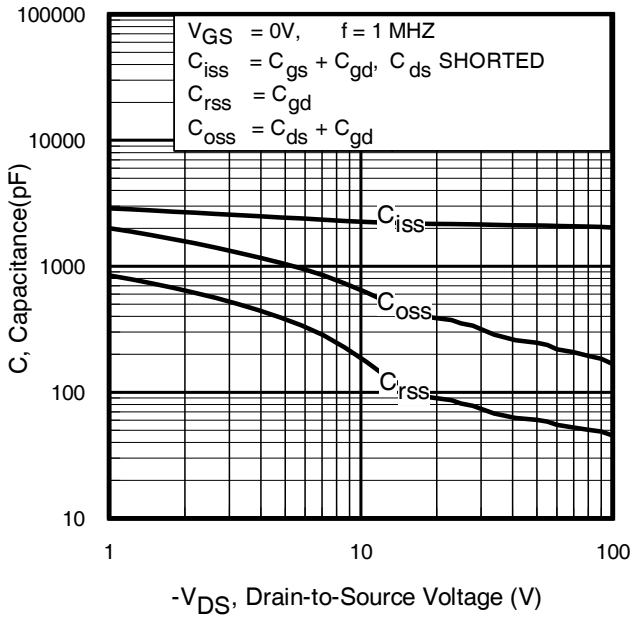


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

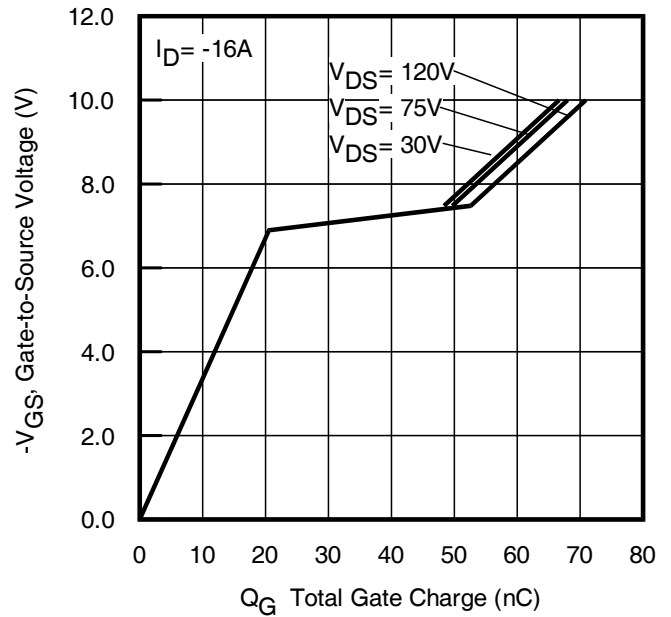


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

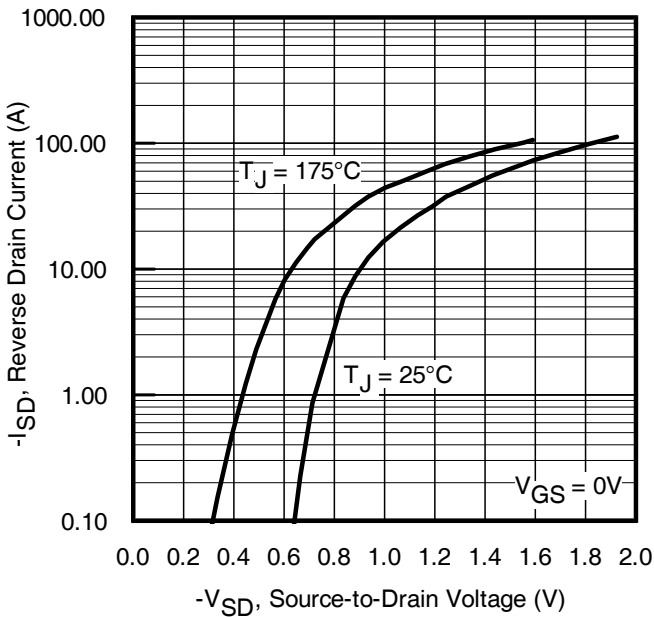


Fig 7. Typical Source-to-Drain Diode Forward Voltage

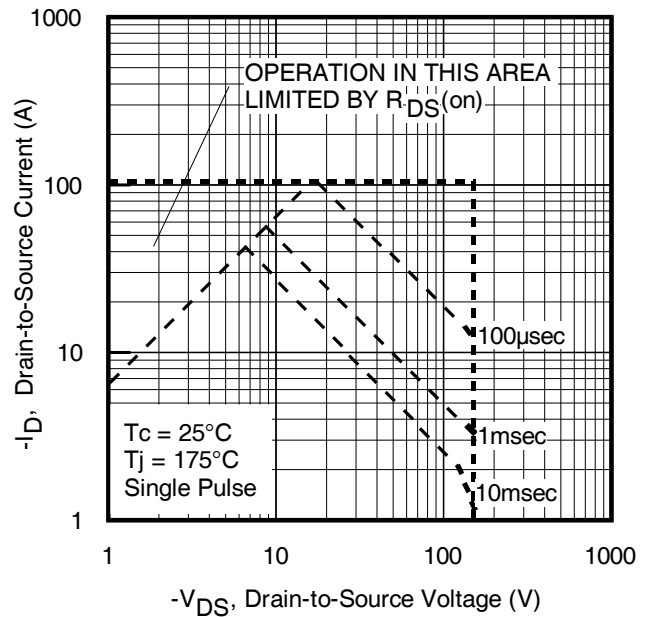
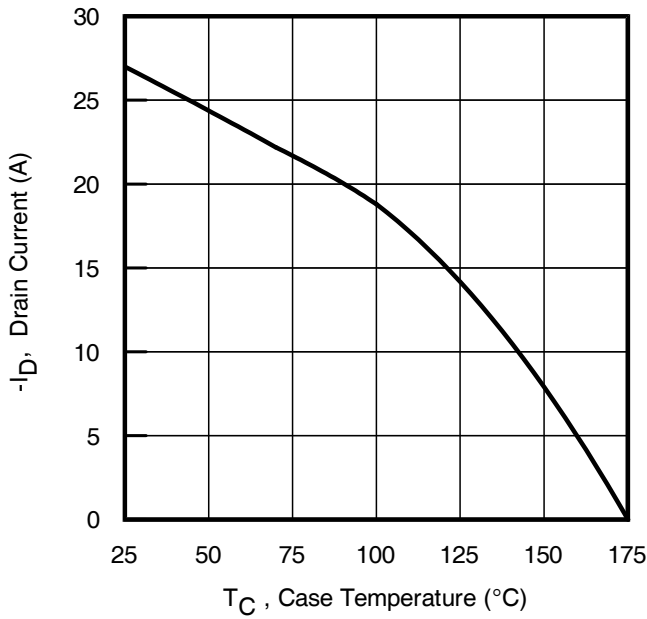
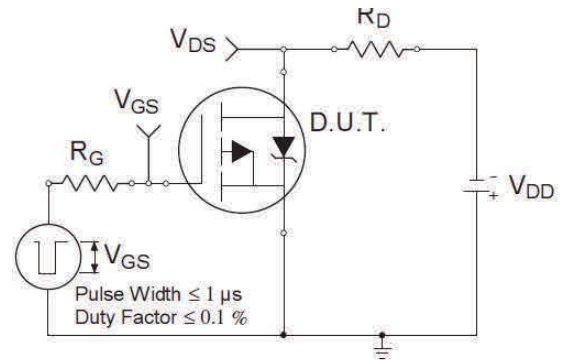
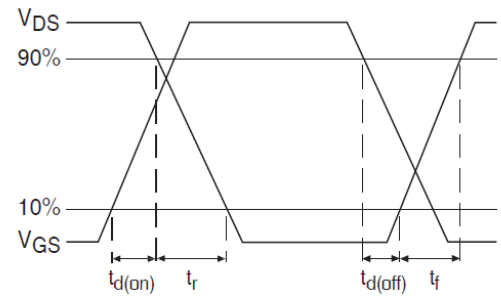
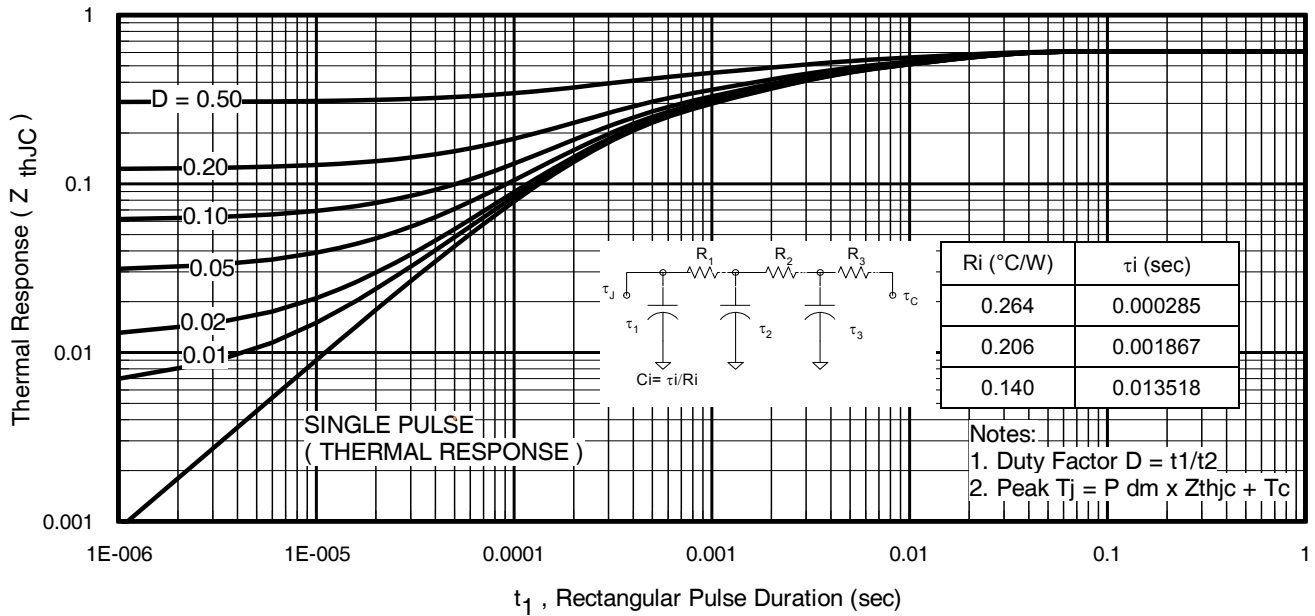
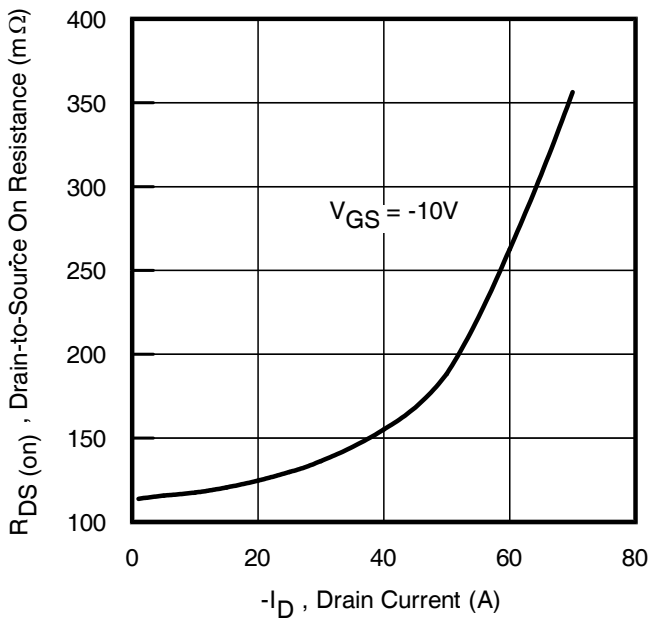
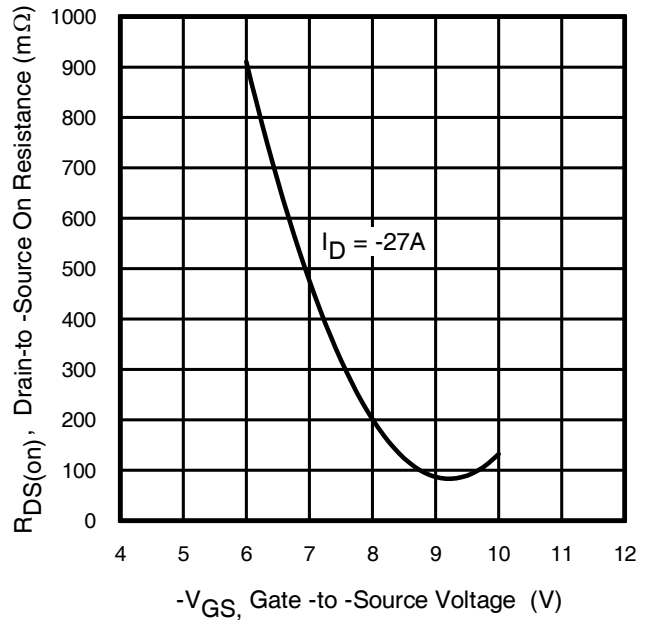
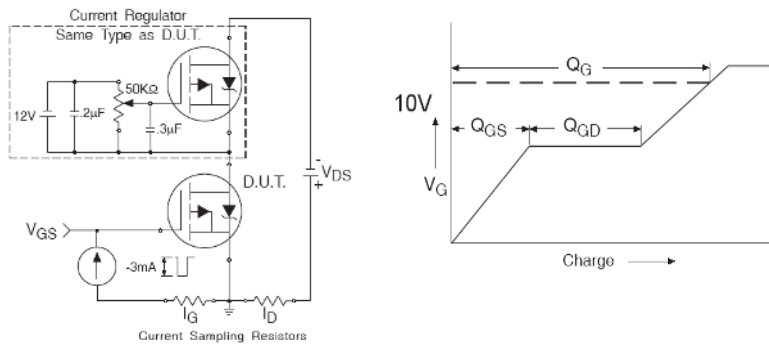
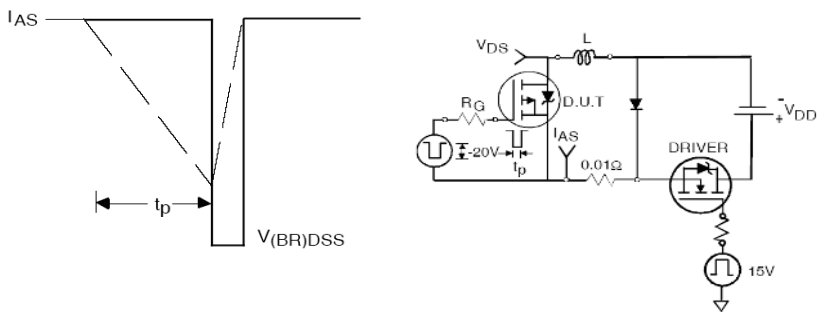
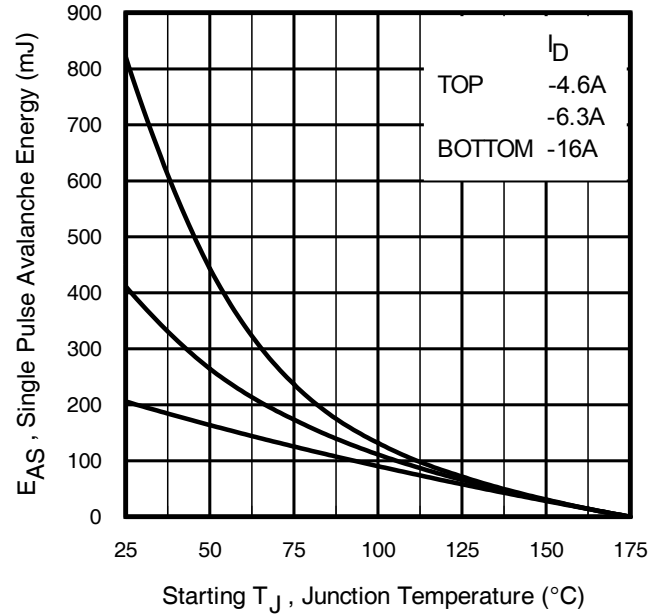
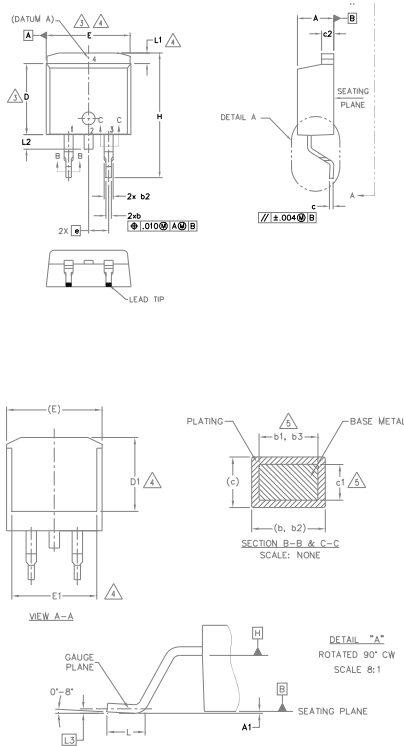


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12. On-Resistance vs. Drain Current

Fig 13. On-Resistance vs. Gate Voltage

Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

Fig 15c. Maximum Avalanche Energy vs. Drain Current

D2-Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [".005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	4
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS
DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

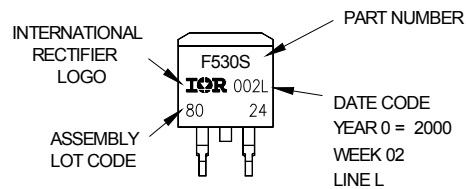
IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

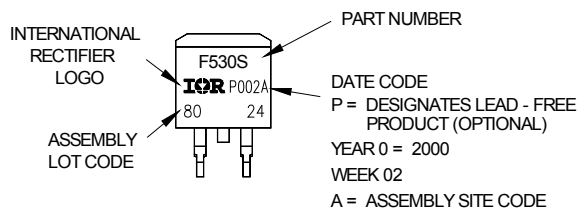
D2-Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

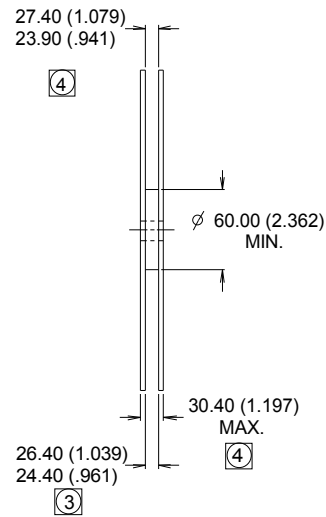
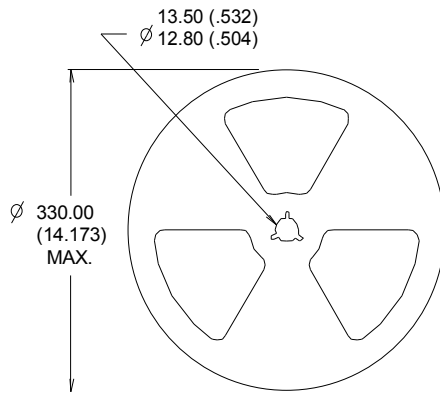
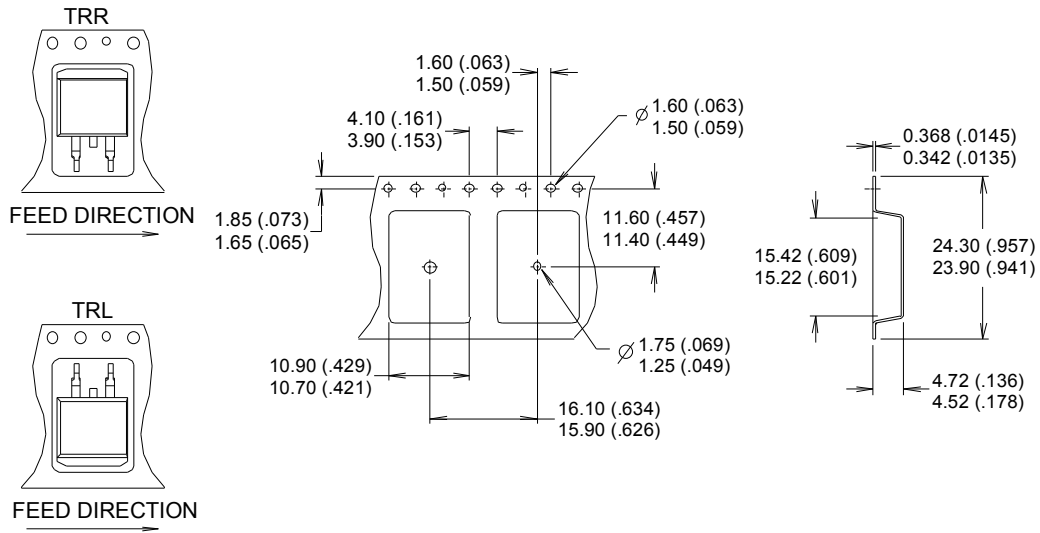
Note: "P" in assembly line position
indicates "Lead - Free"



OR



Note: For the most current drawing please refer to Infineon's web site www.infineon.com

D2-Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))

NOTES :

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D2-Pak	MSL1 (per JEDEC J-STD-020D) ††
RoHS Compliant	Yes	

† Qualification standards can be found at Infineon's web site www.infineon.com

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
3/25/2015	<ul style="list-style-type: none"> Updated datasheet based on IR corporate template. Updated package outline and part marking on page 7. Removed TO-262 Pak (IRF6218LPbF) from datasheet-all pages
5/26/2016	<ul style="list-style-type: none"> Updated datasheet with corporate template. Added disclaimer on last page.

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