AOZ6605PI

EZBuck™ 5A Synchronous Buck Regulator

General Description

The AOZ6605PI works from 4.5V to 18V input voltage range, and provides up to 5A of continuous output current with an output voltage adjustable down to 0.8V.

The AOZ6605PI comes in EPAD-SO8 package and is rated over a -40°C to +85°C operating ambient temperature range.

Features

- 4.5V to 18V operating input voltage range
- Synchronous Buck with internal low $R_{DS(ON)}$ (55mΩ/ 12mΩ) high-side and low-side MOSFETs
- External program soft start
- U-PEM (pulse energy mode) enables 86% plus efficiency with Io=10mA (Vin=12V, Vo=5V)
- Adjacent pin short protection
- Output voltage adjustable to 0.8V
- Adjacent pin short protection
- 5A continuous output current
- 650kHz PWM operation
- Cycle-by-cycle current limit
- Pre-bias start-up
- Extensive protection features
- EPAD-SO8 package

Applications

- High reliable DC/DC converters
- High performance LCD TV
- High performance cable modems

Green Product

Typical Application

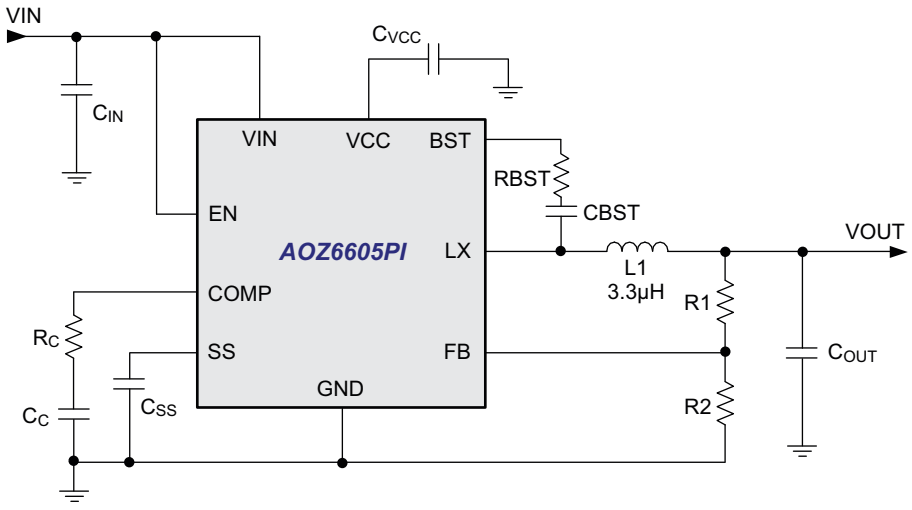


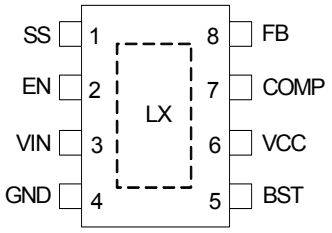
Figure 1. 5A Synchronous Buck Regulator, Fs = 650kHz

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ6605PI	-40°C to +85°C	8-Pin EPAD SO-8	Green Product

AOS Green Products use reduced levels of Halogens and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1	SS	Soft Start Pin.
2	EN	Enable pin. Logic high to enable the device.
3	VIN	Supply voltage input. When VIN rises above the UVLO threshold and EN is logic high, the device starts up.
4	GND	Power ground.
5	BST	Bootstrap. Requires a capacitor connected between LX and BST to form a floating supply across the high-side switch driver.
6	VCC	Internal LDO output.
7	COMP	External loop compensation pin. Connect a RC network between COMP and GND to compensate the control loop.
8	FB	Feedback input. The FB pin is used to set the output voltage via a resistive voltage divider between the output and GND.
Exposed Pad	LX	Switching node. LX is the drain of the internal low-side power FETs.

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN}), EN (V_{EN})	+20V
LX to GND	-0.7V to V_{IN}+0.3V
LX to GND (20ns)	-5V to 22V
VCC, FB, COMP to GND	-0.3V to 6V
VBST to LX	6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(1)	2kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating ratings.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 18V
Output Voltage Range	0.8V to 0.85*V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance EPAD SO8 (θ_{JA})(2)	40°C/W

Note:

2. The value of θ_{JA} is measured with the device mounted on a 1-in^2 FR-4 four layer board with 2oz copper and Vias, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specification board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C. These specifications are guaranteed by design.

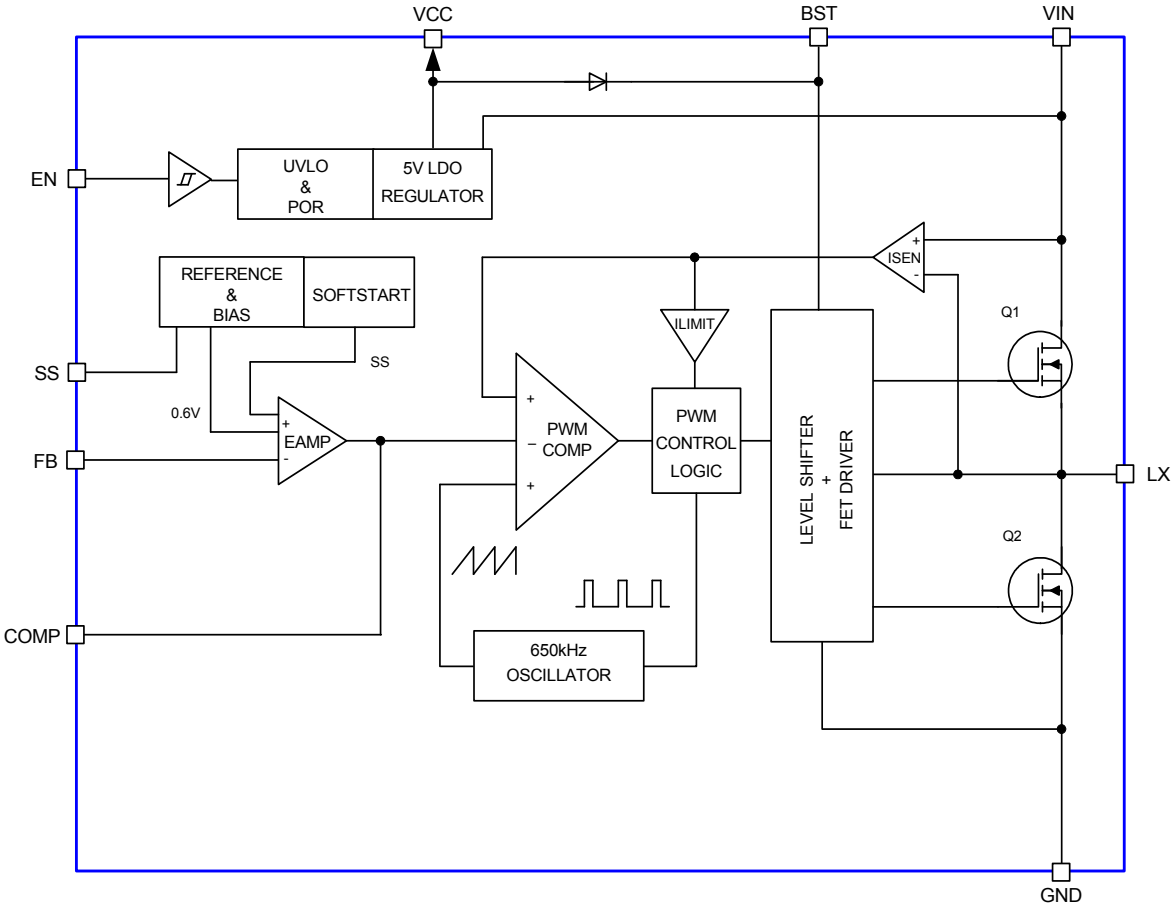
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	Supply Voltage		**4.5**		**18**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} rising V_{IN} falling	 **3.3**	4.0 3.7	**4.45**	V V
V_{CC}	VCC Regulator			5		V
	VCC Load Regulator	I_{CC} = 5mA		3		%
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0A		250		µA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		**1**	**10**	µA
				0.1	1	µA
V_{FB}	Feedback Voltage	T_A = 25°C	0.598	0.607	0.616	V
R_O	Load Regulation	PWM mode 1A < ILoad < 5A		0.5		%
S_V	Line Regulation	4.5V < V_{IN} < 18V		1		%
I_{FB}	Feedback Voltage Input Current				200	nA
V_{EN}	EN Input Threshold	Off threshold On threshold -40°C < $T_{Junction}$ < 125°C	 **2**		**0.6**	V V
V_{HYS}	EN Input Hysteresis			300		mV
I_{EN}	EN Input Current	V_{EN} = 5V			**5**	µA
t_{SS}	SS Time	C_{SS} = 22nF		2.5		ms
Modulator						
f_O	Frequency		550	650	750	kHz
D_{MAX}	Maximum Duty Cycle		85			%
T_{MIN}	Controllable Minimum On-Time				110	ns

Electrical Characteristics

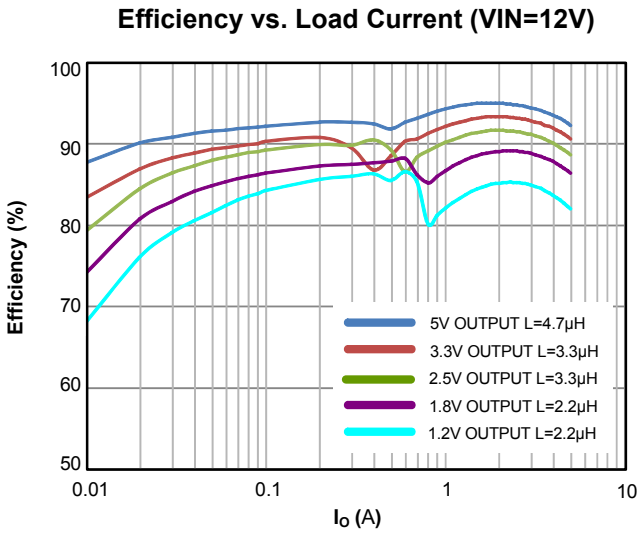
T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C. These specifications are guaranteed by design.

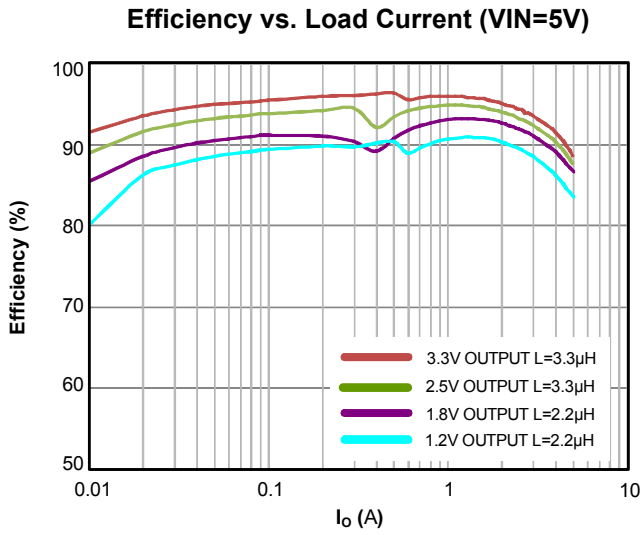
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Gm_{cs}	Current Sense Transconductance			8		A/V
Gm_a	Error Amplifier Transconductance			400		µA/V
I_{CH}	Charging Current of Error Amplifier			40		µA
Protection						
I_{LIM}	Current Limit		5.5	6		A
V_{OVP}	Over Voltage Protection	Off threshold On threshold		720 620		mV
T_{OTP}	Over-temperature Shutdown LImit	T_J rising T_J falling		150 100		°C °C
Output Stage						
R_H	High-Side Switch On-Resistance	V_{BST-LX} = 5V		55		mΩ
R_L	Low-Side Switch On-Resistance	V_{CC} = 5V		12		mΩ

Functional Block Diagram

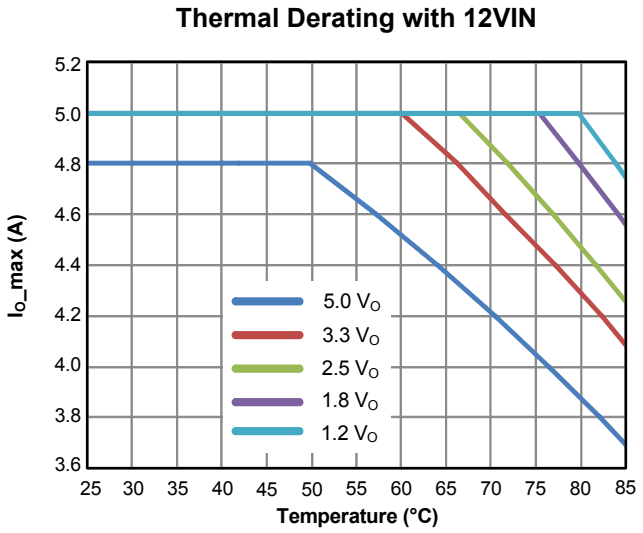


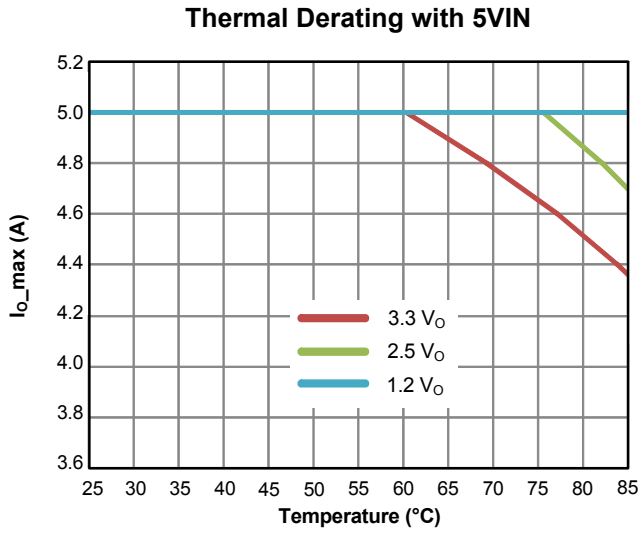
Efficiency





Thermal Derating

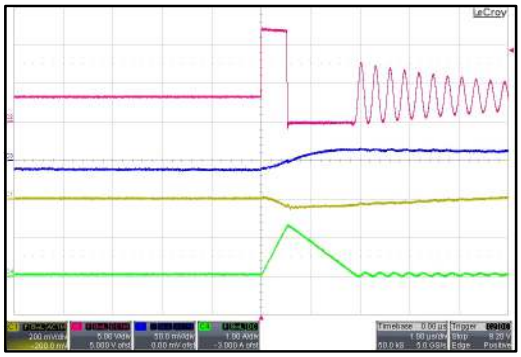




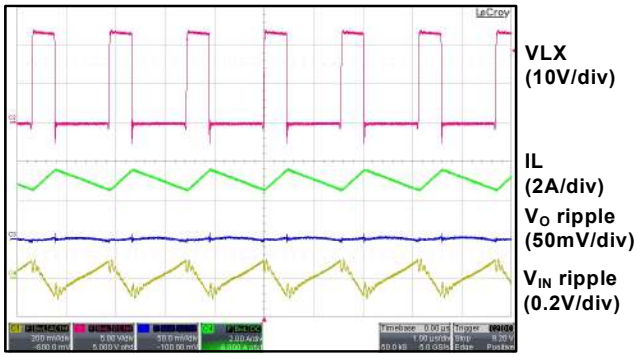
Typical Characteristics

Circuit of Typical Application. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, unless otherwise specified.

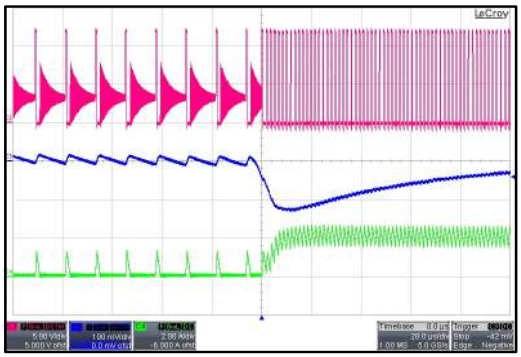
Light Load Operation



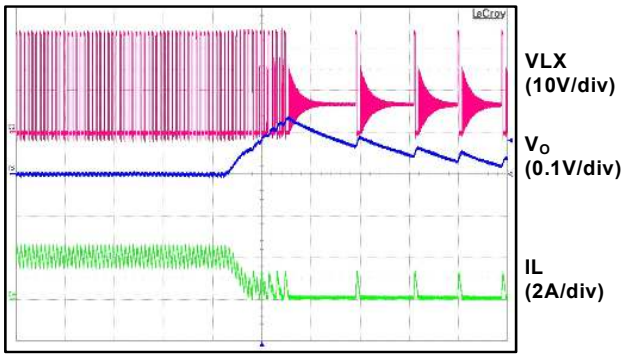
Full Load Operation



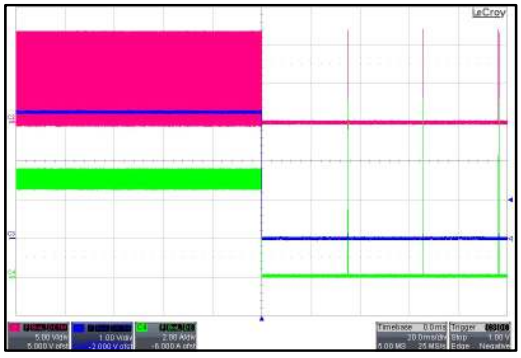
PWM to PEM Mode Change



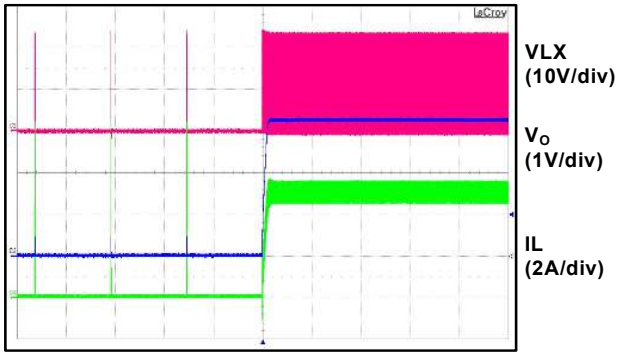
PEM to PWM Mode Change



Short Protection



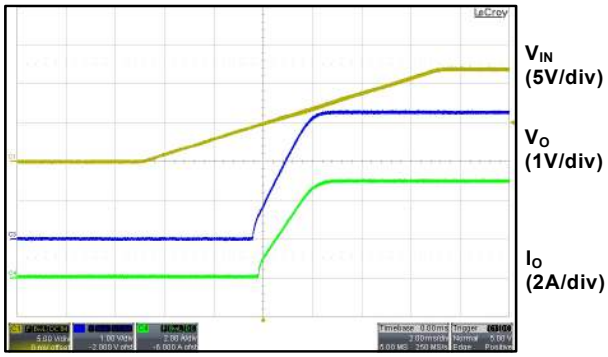
Short Protection Recovery



Typical Characteristics (continued)

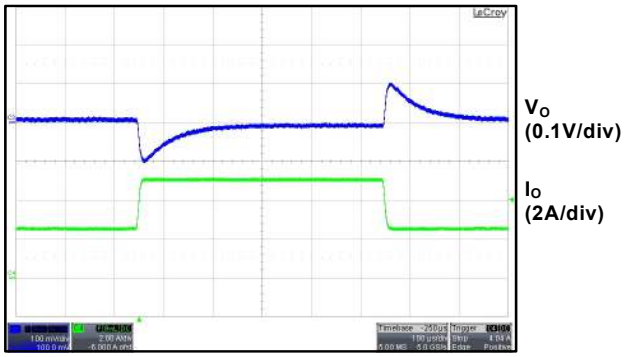
Circuit of Typical Application. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, unless otherwise specified.

Start-up to Full Load



2ms/div

50% to 100% Load Transient



100µs/div

Detailed Description

The AOZ6605PI is a current-mode step down regulator with integrated high-side NMOS switch and low-side NMOS switch. It operates from a 4.5V to 18V input voltage range and supplies up to 5A of load current. Features include, enable control, Power-On Reset, input under voltage lockout, output over voltage protection, external soft-start and thermal shut down.

The AOZ6605PI is available in EPAD-SO8 package.

Enable and Soft Start

The AOZ6605PI has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.1V and voltage on EN pin is HIGH. The soft start time is programmed by external soft start capacitor, and can be calculated by below equation:

$$T_{SS(ms)} = \frac{Css(nF)x0.6V}{5uA}$$

The EN pin of the AOZ6605PI is active high. Connect the EN pin to VIN if enable function is not used. Pull it to ground will disable the AOZ6605PI. Do not leave it open. The voltage on EN pin must be above 2 V to enable the AOZ6605PI. When voltage on EN pin falls below 0.6V, the AOZ6605PI is disabled.

Light Load and PWM Operation

Under low output current settings, the AOZ6605PI will operate with pulse energy mode to obtain high efficiency. In pulse energy mode, the PWM will not turn off until the inductor current reaches to 800 mA and the current signal exceeds the error voltage.

Steady-State Operation

Under heavy load steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ6605PI integrates an internal N-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal low-side N-MOSFET switch to output. The internal adaptive FET driver guarantees no turn on overlap of both high-side and low-side switch.

Comparing with regulators using freewheeling Schottky diodes, the AOZ6605PI uses freewheeling NMOSFET to realize synchronous rectification. It greatly improves the converter efficiency and reduces power loss in the low-side switch.

The AOZ6605PI uses a N-Channel MOSFET as the high-side switch. Since the NMOSFET requires a gate voltage higher than the input voltage, a boost capacitor is needed between LX pin and BST pin to drive the gate. The boost capacitor is charged while LX is low.

Output voltage can be set by feeding back the output to the FB pin by using a resistor divider network. In the application circuit shown in Figure 1. The T-type resistor divider network includes R_1 R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R1 with equation below.

$$V_O = 0.6 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R_1, R_2 and most used output voltage values are listed in Table 1.

VO (V)	R1 (kΩ)	R2 (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	68.1	15
5.0	110	15

Table 1.

Combination of R1 and R2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Protection Features

The AOZ6605PI has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ6605PI employs peak current mode control, during over current conditions, the peak inductor current is automatically limited to cycle-by cycle, and if output drop to some level after current limit, then the AOZ6605PI will shut down and auto restart with hiccup mode.

Power-On Reset (POR)

A power-on reset circuit monitors the VIN voltage. When the VIN voltage exceeds 4V, the converter starts operation. When VIN voltage falls below 3.7V, the converter will be shut down.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side NMOS if the junction temperature exceeds 150ºC. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100ºC.

Application Information

The basic AOZ6605PI application circuit is show in Figure 1. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the V_{IN} pin and GND pin of AOZ6605PI to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below::

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure. 2 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_O$.

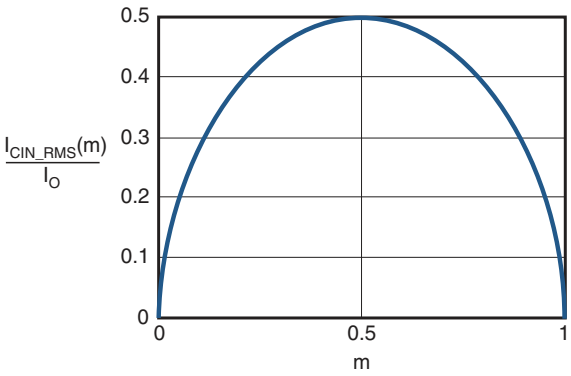


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary in practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 40% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor need to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times (ESR_{CO} + \frac{1}{8 \times f \times C_O})$$

where C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor. When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

The AOZ6605PI employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where

C_O is the output filter capacitor;

R_L is load resistor value;

ESR_{CO} is the equivalent series resistance of output capacitor;

The compensation design is actually to shape the converter control loop transfer function to get desired gain and phase. Several different types of compensation network can be used for the AOZ6605PI. For most cases a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ6605PI, FB pin and COMP pin are the inverting input and the output of internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{p2} = \frac{G_{EA}}{2\pi \times Cc \times G_{VEA}}$$

Where

G_{EA} is the error amplifier transconductance,

G_{VEA} is the error amplifier voltage gain,

C_c is compensation capacitor in Figure 1;

The zero given by the external compensation network, capacitor C_2 and resistor R_3, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_c \times R_c}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover is the also called the converter

bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of switching frequency.

The strategy for choosing R_c and Cc is to set the cross over frequency with Rc and set the compensator zero with C_c. Using selected crossover frequency, f_C, to calculate R_3:

$$R_c = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_o}{G_{EA} \times G_{CS}}$$

where f_C is desired crossover frequency. For best performance, fc is set to be about 1/10 of switching frequency:

V_{FB} is 0.6V;

G_{EA} is the error amplifier transconductance,

G_{CS} is the current sense circuit transconductance, which is 8 A/V;

The compensation capacitor C_c and resistor R_c together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_2 can is selected by:

Equation above can also be simplified to:

$$C_c = \frac{C_O \times R_L}{Rc}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Consideration

In the AOZ6605PI buck regulator circuit high pulsing current flows through two circuit loops. The first loop starts from the input capacitors to the VIN pin, to the LX pad, to the filter inductor to the output capacitor and load and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side NMOSFET. Current flows in the second loop when the low side NMOSFET is on.

In PCB layout minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor and GND pin of the AOZ6605PI.

In the AOZ6605PI buck regulator circuit, the major power dissipating components are the AOZ6605PI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ6605PI and thermal impedance from junction to ambient.

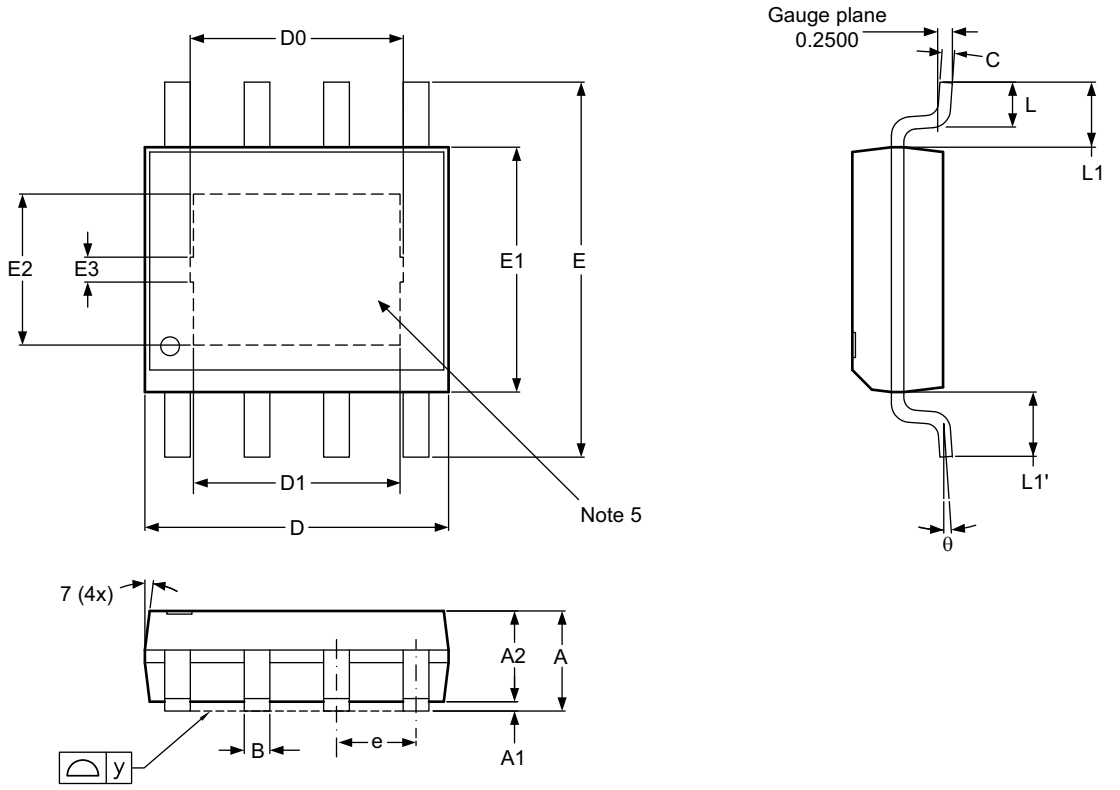
$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA}$$

The maximum junction temperature of AOZ6605PI is 150ºC, which limits the maximum load current capability.

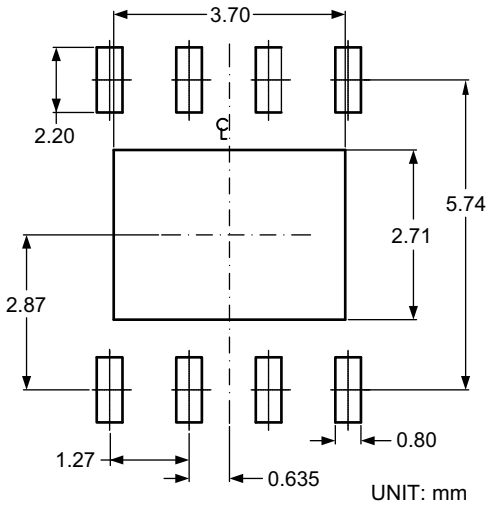
The thermal performance of the AOZ6605PI is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

1. The exposed pad (LX) is connected to internal Highside FET source and Low-side FET drains. Connect a large copper plane to LX pin to help thermal dissipation.
2. Do not use thermal relief connection to the VIN and the GND pin. Pour a maximized copper area to the GND pin and the VIN pin to help thermal dissipation.
3. Input capacitor should be connected to the VIN pin and the GND pin as close as possible.
4. Make the current trace from LX pins to L to Co to the GND as short as possible.
5. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
6. Keep sensitive signal trace away from the LX pad.

Package Dimensions, SO-8 EP1



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.40	1.55	1.70
A1	0.00	0.05	0.10
A2	1.40	1.50	1.60
B	0.31	0.406	0.51
C	0.17	—	0.25
D	4.80	4.96	5.00
D0	3.20	3.40	3.60
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
e	—	1.27	—
E1	3.80	3.90	4.00
E2	2.21	2.41	2.61
E3	0.40 REF		
L	0.40	0.95	1.27
y	—	—	0.10
θ	0°	3°	8°
| L1–L1' |	—	0.04	0.12
L1	1.04 REF		

Dimensions in inches

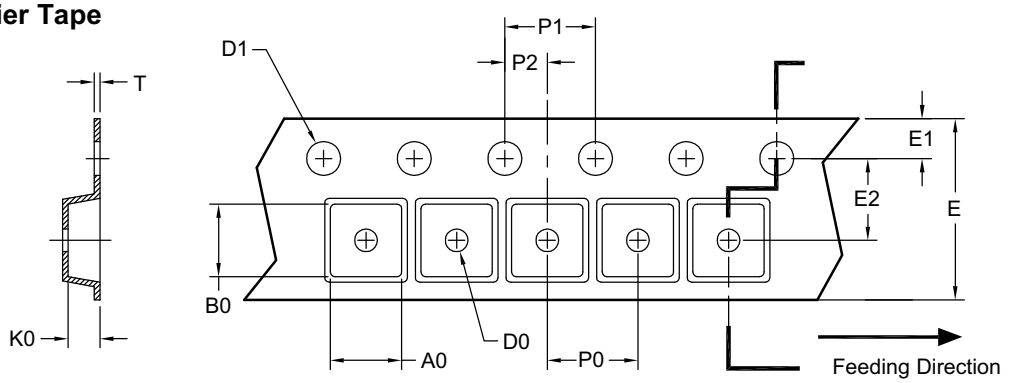
Symbols	Min.	Nom.	Max.
A	0.055	0.061	0.067
A1	0.000	0.002	0.004
A2	0.055	0.059	0.063
B	0.012	0.016	0.020
C	0.007	—	0.010
D	0.189	0.195	0.197
D0	0.126	0.134	0.142
D1	0.122	0.130	0.138
E	0.228	0.236	0.244
e	—	0.050	—
E1	0.150	0.153	0.157
E2	0.087	0.095	0.103
E3	0.016 REF		
L	0.016	0.037	0.050
y	—	—	0.004
θ	0°	3°	8°
| L1–L1' |	—	0.002	0.005
L1	0.041 REF		

Notes:

1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gauge plane.
3. Tolerance 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Followed from JEDEC MS-012

Tape and Reel Dimensions, SO-8, EP1

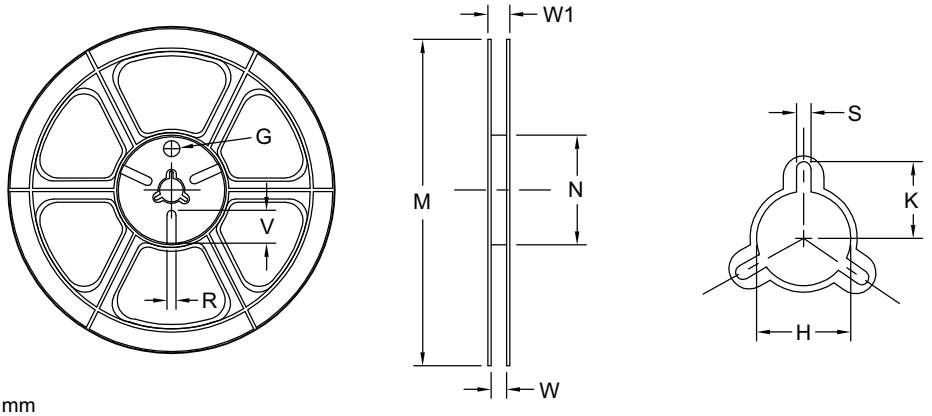
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

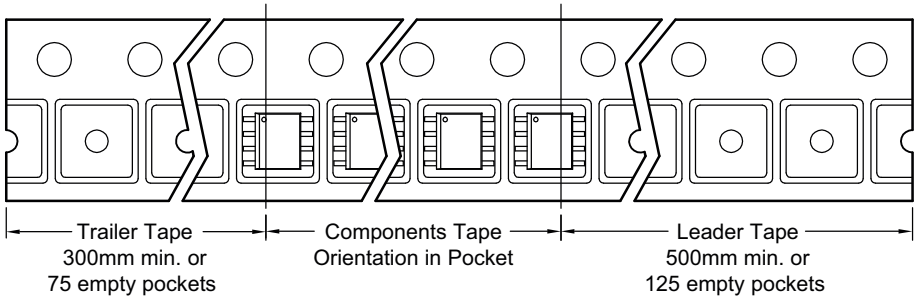
Reel



UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation



Part Marking