A Product Line of
Diodes Incorporated

PI2DPX2023

1.8V 20Gbps DP2.0 Linear ReDriver with AUX Listener & Pin Strap control

Features

- 4-to-4 linear ReDriver™ channel configuration with CTLE gain compensation up to 13.8dB @20Gbps
- Supports 4-lane DP2.0 (UHBR20/UHBR13/UHBR10)/HBR3/HBR2/HBR/RBR
- Ultra low latency (< 300ps) for better interoperability and data throughput
- 4 level controls on CTLE Gain (7.1 to 13.8dB), Flat Gain (-4 to +2dB)
- Integrated AUX channel listener for D3 power saving mode.
- Low Power - DisplayPort active - 324mW typical, D3 power down mode - 1.8mW typical, Disable Power - 27uW typical
- Single Power Supply: 1.8V +/-5%
- Industrial Temperature Support: -40°C to +85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - Tiny 32-pin, WLGA (FLA) 2.85 x 4.5 mm (0.4 mm pitch, 0.7mm max height)

Description

The DIODES™ PI2DPX2023 is a 20Gbps DP2.0/DP1.4 linear ReDriver in a 4-to-4 configuration operated by a 1.8V power supply. The device supports UHBR20 (DP2.0 20Gbps), UHBR13.5 (DP2.0 13.5Gbps), UHBR10 (DP2.0 10Gbps), HBR3 (DP1.4 8.1Gbps), HBR2 (DP1.2 5.4Gbps), HBR(DP1.1 2.7Gbps) and RBR(DP1.0 1.62Gbps) under various DisplayPort speeds. With the on-chip AUX channel listener, the device can automatically monitor the system operation status to enter D3 power saving mode.

The non-blocking linear redriver design ensures that the differential signals conveying pre-shoot and de-emphasis equalization waveforms from the transmitter side to the receiver side help optimize the overall channel link adjustment conducted by the system transmitter and receiver that has been equipped with DFE. The CTLE equalizers are implemented at the inputs of the redriver to compensate the channel loss and reduce the ISI jitters. The flat gain adjustments support the eye diagram opening. The CTLE EQ gains and flat gains are tuned via pin strap control.

Applications

- Graphics Add In Cards
- Laptop, Desktop and AIO PCs
- Workstation and Servers
- Docking Station
- Display Monitors
- Gaming Console
- Active Cables

Ordering Information

Ordering Number	Package Code	Description
PI2DPX2023FLAEX	FLA	32-Pin, W-LGA4528-32

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

Revision History

Date	Revision	Description
March 2021	1	Preliminary Datasheet Release Updated Pin Description & Block Diagram
April 2021	2	Update Pin Description
October 2021	3	Updated Section Description, Feature Updated Section Pin Description Updated Section CTLE Equalization, Flat Gain, and Chip Enable Control Updated Section Power Consumption Updated Section AC/DC Specifications
July 2022	4	Datasheet Release Updated Graphics Add In Card Application Updated Section Pin Description Updated Section Part Marking Updated Section Packaging Mechanical Updated Figure 9 Channel Measurement Setup

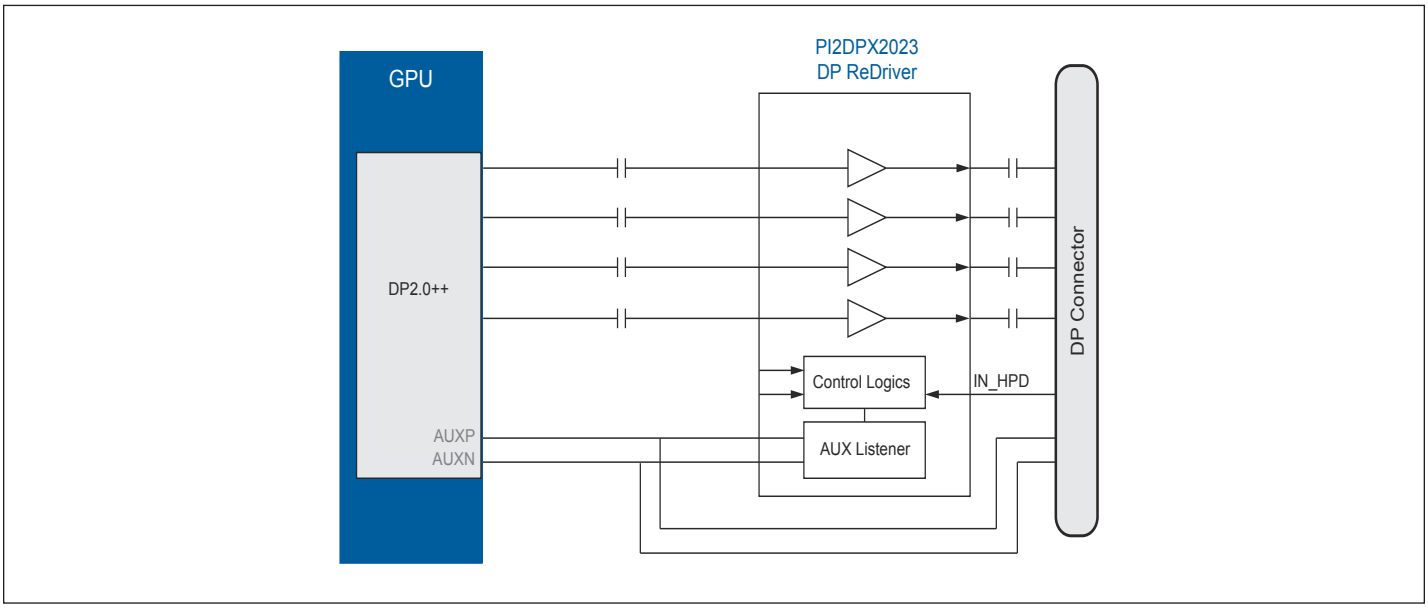
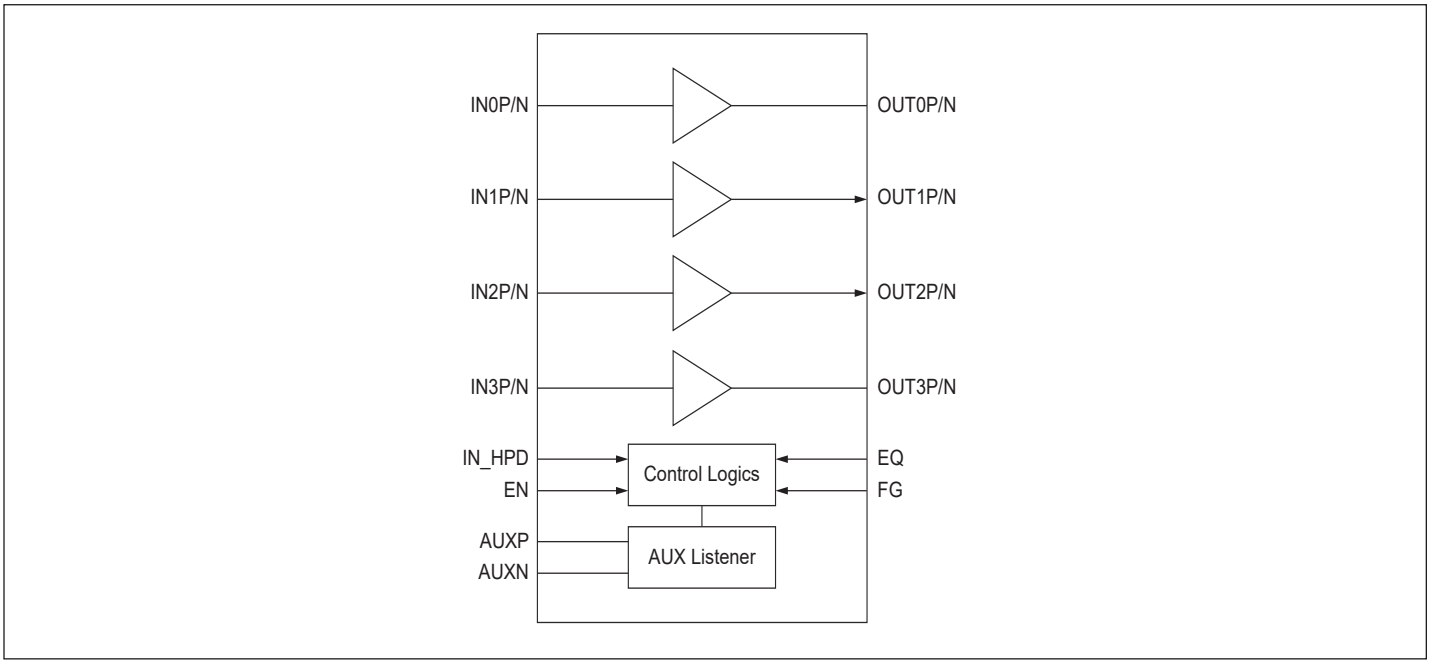
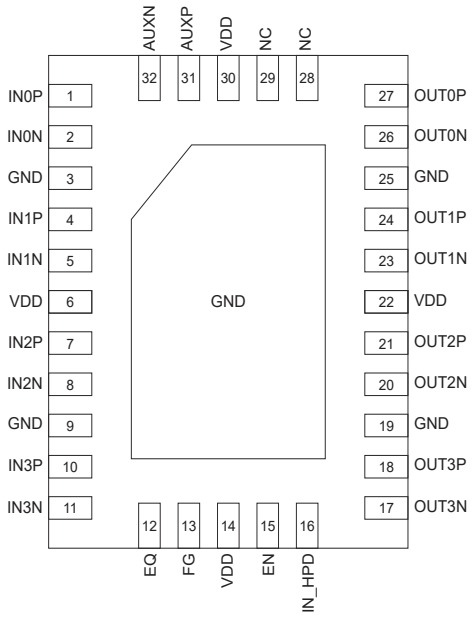


Figure 1. Graphics Add In Card Application

Block Diagram



Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
Power and GND			
6, 14, 22, 30	VDD	Power	1.8V power supply, ±5%
3, 9, 19, 25, Center Pad	GND	Ground	Supply ground
Control Pins			
12	EQ	I	Equalization selection. It is a 4-level input (See Table 3) with internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
13	FG	I	Flat Gain Selection. It is a 4-level input (See Table 4) with internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
15	EN	I	Chip Enable. With internal 300kΩ pull-up resistor. "Low": Chip Power Down "High": Normal Operation (Default)
16	IN_HPD	I	Hot Plug Detection from Sink. With internal 300kΩ pull-down resistor.
High Speed I/O Pins			
18, 17 27, 26	OUT3P, OUT3N OUT0P, OUT0N	O	Channel CML output terminals. With selectable output termination between 50Ω to VDD or Hi-Z

Pin Description Cont.

Pin #	Pin Name	Type	Description
21, 20 24, 23	OUT2P, OUT2N OUT1P, OUT1N	O	Channel CML output terminals. With selectable output termination between 50Ω to VDD or Hi-Z
1, 2 10, 11	IN0P, IN0N IN3P, IN3N	I	CML input terminals. With selectable input termination between 50Ω to internal VbiasRx or 78kΩ to internal VbiasRx.
4, 5 7, 8	IN1P, IN1N IN2P, IN2N	I	CML input terminals. With selectable input termination between 50Ω to internal VbiasRx or 78kΩ to internal VbiasRx.
Side Band Signal Pins			
29, 28	NC	I/O	No connect. Leave it floating.
31, 32	AUXP, AUXN	I/O	DisplayPort AUX CH differential signal connections

Operation Mode

I/O Termination Resistance under Different Conditions

Symbol	Parameter	Resistance	Units
RX Terminal			
R_{in-pd}	Input res at EN=0	78k to VbiasRx	Ω
$R_{in-Active}$	Input res at active mode condition	50 to VbiasRx1	Ω
$R_{in-DP-standby}$	Input res in DP standby mode	78k to VbiasRx	Ω
$R_{in-DP-active}$	Input res in DP active mode	50 to VbiasRx1	Ω
$R_{in-DP-D3}$	Input res in DP D3 mode	78k to VbiasRx	Ω
TX Terminal			
R_{out-pd}	Output res at EN=0	78k to VbiasTx	Ω
$R_{out-Active}$	Output res at active mode condition	50 to VDD	Ω
$R_{out-DP-standby}$	Output res in DP standby mode	78k to VbiasTx	Ω
$R_{out-DP-active}$	Output res in DP active mode	50 to VDD	Ω
$R_{out-DP-D3}$	Output res in DP D3 mode	78k to VbiasTx	Ω

Notes:
1) The value of Rin will be updated only after the receiver evaluation. Thus, the value can be 50Ω or 78kΩ.
2) The value of Rout will be updated only after the receiver evaluation. Thus, the value can be 50Ω or 6kΩ.

DisplayPort Mode

By default, all channels will go to active mode if HPD bit = 1. The ON/OFF of each DP channel is controlled by the Aux lane count.

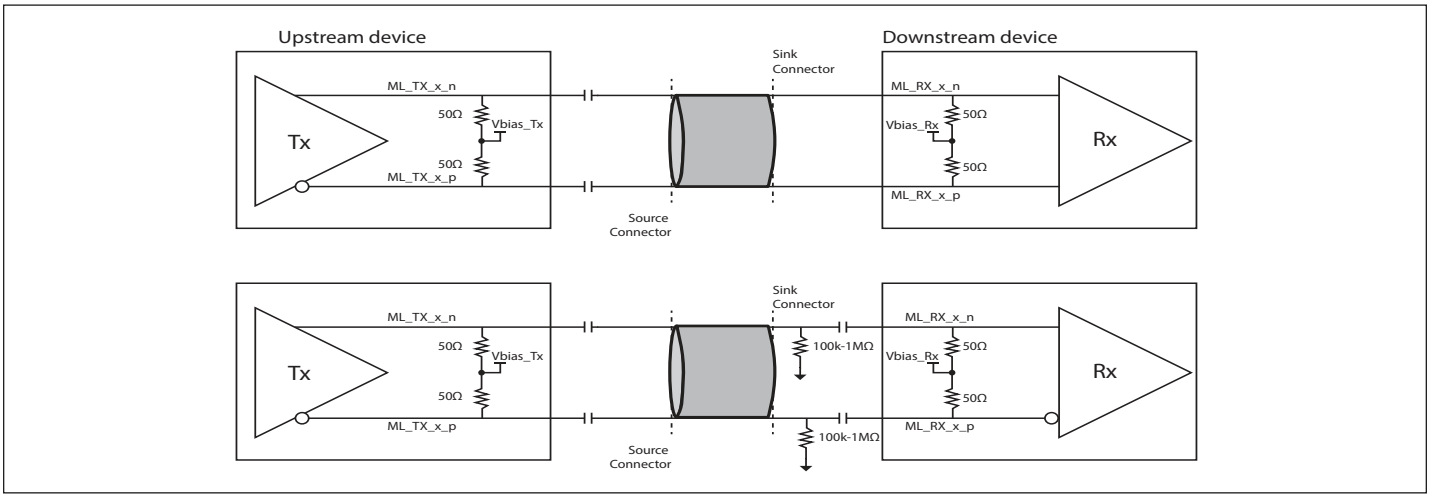


Figure 2. DisplayPort Main Link Connection Diagram

DisplayPort Main Link

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DP TX drives doubly terminated, AC-coupled differential pairs in a manner compliant with the Main-Link Transmitter electrical specification.

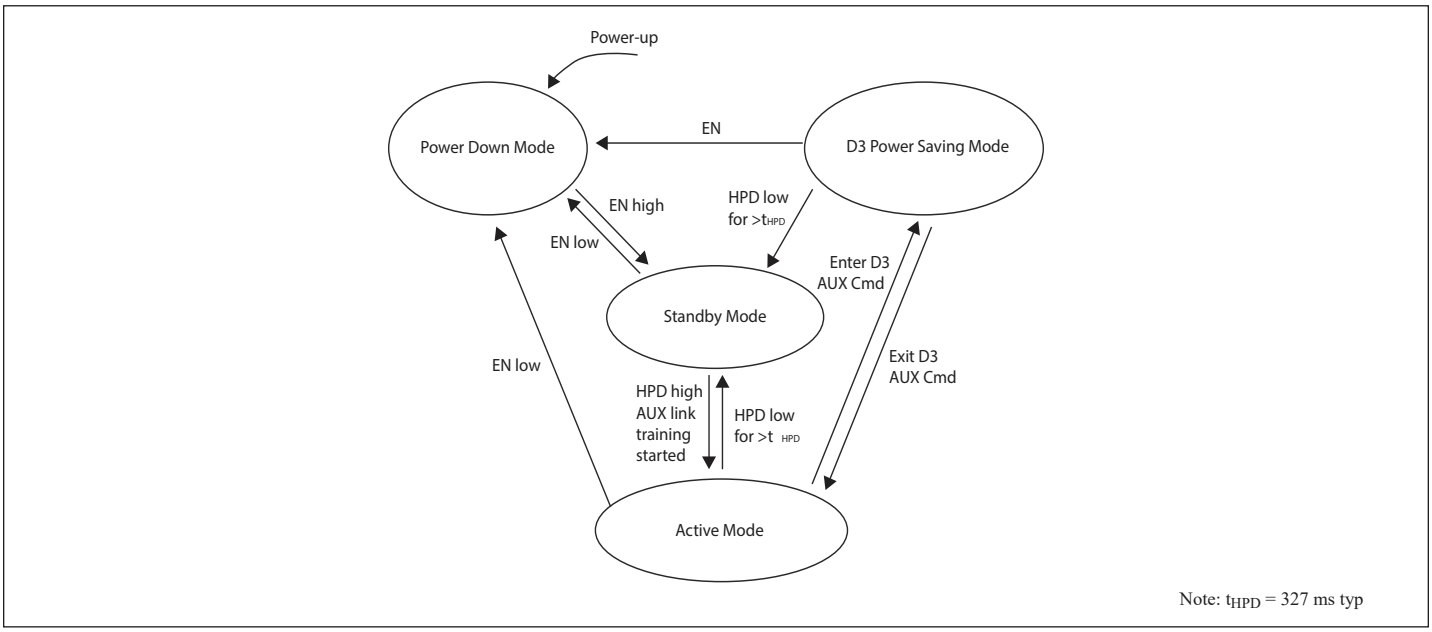


Figure 3. DisplayPort Operation Modes

Table 2. Description of DP Operating Mode

State	Mode	Description
1	Power Down Mode	Lowest power consumption (most circuitries are off); all outputs are high-impedance; All inputs are ignored. AUX listener is turned OFF.
2	Standby Mode	Low power consumption (AUX listener is OFF); Main Link outputs are disabled
3	Active Mode	Data transfer (normal operation); AUX listener is active. The AUX listener is actively monitoring for Link Training. At power-up all Main Link outputs are enabled by default.
4	D3 Power Saving Mode	Low power consumption(AUX listener is active); Main Link outputs are disabled

CTLE Equalization, Flat Gain and Chip Enable Controls

Table 3. CTLE Equalization Gain (Typical Values at FG = 0dB)

EQ	Equalizer Setting (dB)					
	@1.35GHz	@2.5GHz	@4GHz	@5GHz	@6.7GHz	@10GHz
0	-0.010	0.329	1.070	1.783	3.354	7.126
R	0.104	0.742	1.898	2.931	5.061	9.614
F	0.283	1.357	3.012	4.364	6.943	11.858
1	0.577	2.256	4.445	6.067	8.923	13.783

Note: R=0.33VDD. F=0.67VDD.

Table 4. Flat Gain Setting (FG)

FG	Flat Gain Setting
0	-4 dB
R	-2 dB
F	+0 dB (Default)
1	+2 dB

Note: R=0.33VDD. F=0.67VDD.

Table 5. Chip Enable Control

EN Pin	Channel Operation
0	Disabled
1	Enabled (Default)

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . +125°C
Supply Voltage to Ground Potential . . . . . –0.5V to VDD+0.3V
Voltage Input to High Speed Differential Pins . . . . . –0.5V to VDD
Voltage Input to Low Speed Pins (SCL, SDA) . . . . . –0.5V to +3.3V
Voltage Input to Low Speed Pins (AUXP/N). . . . . –0.5V to 3.3V
Voltage Input to Low Speed Pins (EN). . . . . –0.5V to VDD+0.3V
ESD, HBM. . . . . ±4000V
ESD CDM . . . . . ±1000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Information

Symbol	Parameter	32-Pin WLGA Package	Units
Theta JA	Junction to Ambient Thermal Resistance	TBD	°C/W

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	1.71	1.8	1.89	V
V_{DD_Noise}	Power Supply Noise Up to 50MHz	—	—	50	mVpp
V_{RX_CM}	Input Source Common-Mode Noise	—	—	150	mVpp
$C_{ac\_coupling}$	System AC Coupling Capacitance	75	—	265	nF
T_A	Ambient Temperature	-40(1)	—	+85	°C

Note:
1. The minimum temperature -40°C guaranteed by design

Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{ON_4DP}	4-lane DP2.0	—	160	220	mA
I_{D3}	DisplayPort D3 power down mode	—	0.9	1.6	mA
I_{ENB}	Disabled mode (EN=Low)	—	8	30	uA
I_{Stdby}	IN_HPD = Low	—	1	1.7	mA

AC/DC Characteristics
(VDD = 1.8 ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	—	1.71	1.8	1.89	V

AC/DC Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Receiver (RX) (100 Ω Differential) Electrical Specification						
$R_{RX-DIFF-DC}$	DC Differential Input Impedance		72	—	120	Ω
$R_{RX-SINGLE-DC}$	DC single ended input impedance to guarantee RxDet	Measured with respect to GND over a voltage of 500mV max	18	—	30	Ω
$Z_{RX-HIZ-DC-PD}$	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25	—	—	kΩ
$C_{ac\_coupling}$	AC coupling capacitance		75	—	265	nF
$V_{RX-CM-AC-P}$	Rx common mode peak voltage	AC up to 5GHz	—	—	150	mVpeak
$V_{RX-CM-DC-Active-Idle-Delta-P}$	Common mode peak voltage $\lvert Avg_{U0} (\lvert V_{TX-D+} + V_{TX-D-} \rvert)/2 - Avg_{U1} (\lvert V_{TX-D+} + V_{TX-D-} \rvert)/2 \rvert$		—	—	200	mVpeak
Transmitter (TX) Electrical Specification						
$V_{TX-DIFF-PP}$	Output differential p-p voltage Swing	Differential Swing $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	—	—	1	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance		72	—	120	Ω
$V_{TX-RCV-DET}$	The amount of Voltage change allowed during RxDet	Type-C Tx Spec +/-60mA	—	—	600	mV
$C_{ac-coupling}$	AC coupling capacitance		75	—	265	nF
$R_{TX-DC-CM}$	Common mode DC output Impedance		18	—	30	Ω
$I_{TX-SHORT}$	Transmitter short circuit current limit		—	—	60	mA
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	VDD-1V	—	VDD	V
$V_{TX-DC-CM}$	Instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	0	—	VDD	V
$V_{TX-CM-AC-PP-Active}$	Active mode TX AC common mode voltage	$V_{TX-D+} + V_{TX-D-}$ for both time and amplitude	—	—	100	mVpp
$V_{TX-Idle-Diff-AC-pp}$	Idle mode AC common mode delta voltage $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	Between D+ and D- in idle mode. Use the HPF to remove DC components. =1/LPF.	—	—	10	mVppd
$V_{TX-Idle-Diff-DC}$	Idle mode DC common mode delta voltage $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	Between D+ and D- in idle mode. Use the LPF to remove AC components. =1/HPF.	—	—	10	mV
Channel Performance						
T_{pd}	Latency	From input to output	—	25	150	ps

AC/DC Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
G_P	Peaking gain (Compensation at 10GHz, relative to 100MHz, 100mVp-p sine wave input)	EQ = 0 EQ = R EQ = F EQ= 1	—	7.1 9.6 11.8 13.7	—	dB
		Variation around typical	-2	—	+2	dB
G_F	Flat gain (100MHz, EQ<2:0>=000)	FG= 0 FG= R FG= F FG= 1	—	-4 -2 0 +2	—	dB
		Variation around typical	-2	—	+2	dB
V_{sw_100M}	Output linear swing (at 100MHz)	EQ= 0	—	910	—	mVppd
V_{sw_10G}	Output linear swing (at 10GHz)	EQ= 0	—	800	—	mVppd
D_{DNEXT}	Differential near-end crosstalk	100MHz to 10GHz, Fig. 6(1)	—	-30	-20	dB
D_{DFEXT}(2)	Differential far-end crosstalk	100MHz to 10GHz, Fig. 7(1)	—	-30	-20	dB
V_{NOISE_IN}	Input-referred noise	100MHz to 10GHz, EQ=0, FG=F, Fig. 7.5	—	0.6	—	mV_{RMS}
		100MHz to 10GHz, EQ=1, FG=F, Fig. 8	—	0.3	—	
V_{NOISE_OUT}	Output-referred noise	100MHz to 10GHz, EQ=0, FG=F, Fig. 8	—	0.3	—	mV_{RMS}
		100MHz to 10GHz, EQ=1, FG=F, Fig. 8	—	0.5	—	
$S11_{DM}$	Input differential mode return loss	10MHz to 10GHz differential mode	—	-11.5	-8.1	dB
$S11_{CM}$	Input common mode return loss	1GHz to 10GHz common mode	—	-11.1	-5	dB
$S22_{DM}$	Output differential mode return loss	10MHz to 10GHz differential mode	—	-12.7	-8.1	dB
$S22_{CM}$	Output common mode return loss	1GHz to 10GHz common mode	—	-11.3	-4	dB
DisplayPort Electrical Specification						
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	VDD-1V	—	VDD	V
$V_{TX-AC-CM\_HBR\_RBR}$	TX AC common mode voltage for HRB and RBR	Measured using an 8b/10b pattern with 50% transition density	—	—	20	mV_{RMS}
$V_{TX-AC-CM\_HBR2}$	TX AC common mode voltage for HBR2		—	—	30	mV_{RMS}

AC/DC Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{TX-DIFFp-p-Level0}$	Differential peak-to-peak output voltage swing Level 0	Tested with Pre-emphasis at Level 0= 0dB Level 1= 3.5dB Level 2= 6.0 dB	0.34	0.4	0.46	V
$V_{TX-DIFFp-p-Level1}$	Differential peak-to-peak output voltage swing Level 1		0.51	0.6	0.68	V
$V_{TX-DIFFp-p-Level2}$	Differential peak-to-peak output voltage swing Level 2		0.69	0.8	0.92	V
Tj TX Total Jitter	UHBR20(20Gbps) TP2	Measured at Transmit output. Prechannel loss from 2.5dB to 13dB	—	—	0.45	UI
	UHBR13(13.5Gbps) TP2		—	—	0.45	UI
	UHBR10(10Gbps) TP2		—	—	0.38	UI
	HBR3 (8.1Gbps)		—	—	0.27	UI
	HBR2 (5.4Gbps)		—	—	0.27	UI
	HBR (2.7Gbps)		—	—	0.294	UI
	RBR (1.62Gbps)		—	—	0.18	UI
AUX Listener Electrical Specification						
C_{in}	Input capacitance at , AUXP or AUXN		—	—	10	pF
$VT_{(AUX\_listener)}$	Threshold of the AUX listener	VCC = 1.8V	100	—	220	mV_{PPd}

Note:

1. Measured using a vector-network analyzer (VNA) with -30dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Subtract the channel gain from the total gain to derive the actual crosstalk

Control Pin Specifications

(VDD = 1.8 ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
2-level Control Pins					
V_{IH}	DC input logic high	VDD*0.65	—	—	V
V_{IL}	DC input logic low	—	—	VDD*0.35	V
I_{IH}	Input high current	—	—	50	uA
I_{IL}	Input Low current	-50	—	—	uA
4-level Control Pins					
V_{IH}	DC input logic “High”	0.92*VDD	VDD	—	V
V_{IF}	DC input logic “Float”F	0.59*VDD	0.67*VDD	0.75*VDD	V
V_{IR}	DC input logic “With Rext to GND” R	0.25*VDD	0.33*VDD	0.41*VDD	V
V_{IL}	DC input logic “Low”	—	GND	0.08*VDD	V
I_{IH}	Input high current	—	—	50	uA

Control Pin Specifications Cont.

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{IL}	Input Low current	-75	—	—	uA
Rext	External resistance connects to GND (+/-5%)	64.6	68	71.4	kΩ
IN_HPD Input Pins					
V_{IH}	DC input logic high	2	—	—	V
V_{IL}	DC input logic low	—	—	0.8	V
Rin	Termination to GND	100	—		kΩ

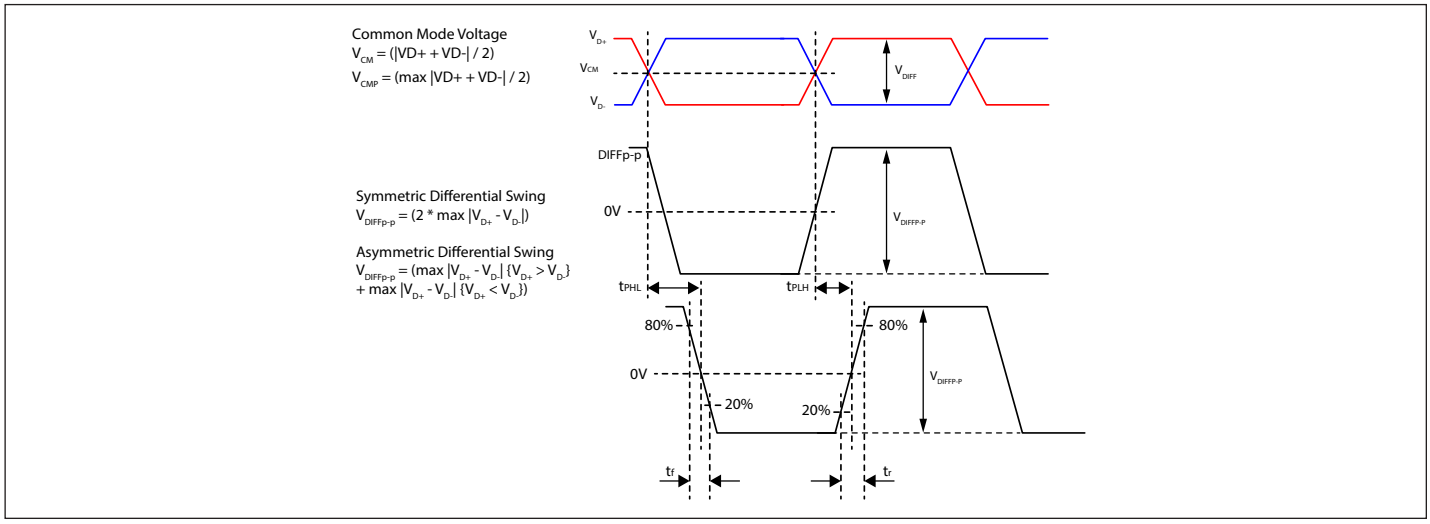


Figure 4. Definition of Peak-to-peak Differential Voltage

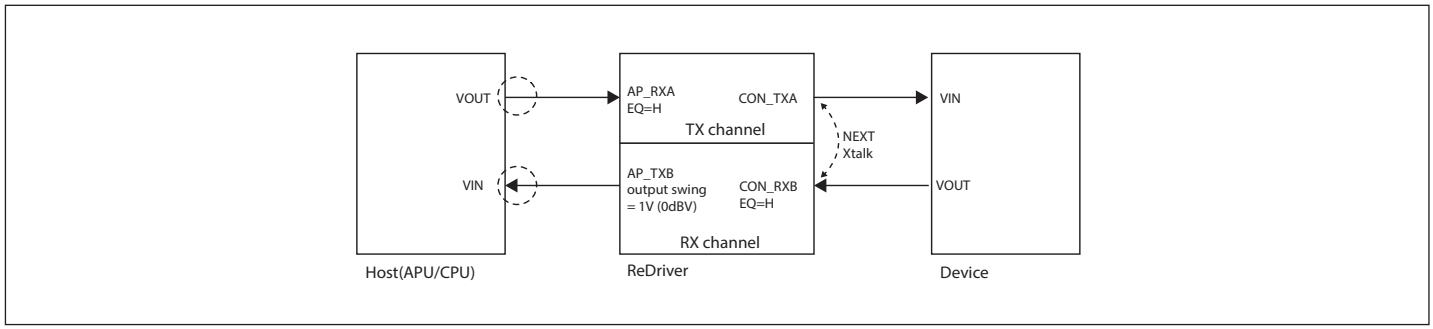


Figure 5. NEXT Crosstalk Definition

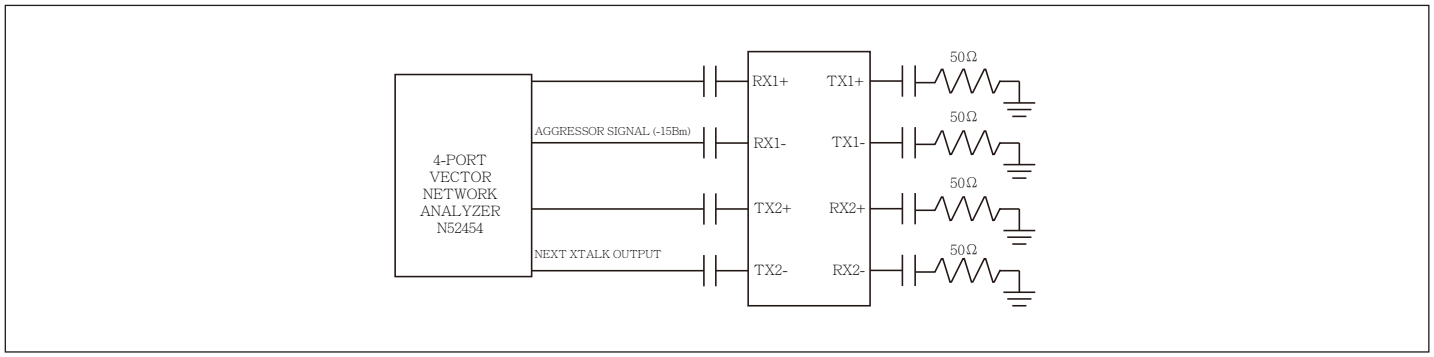


Figure 6. NEXT Channel-isolation Test Configuration

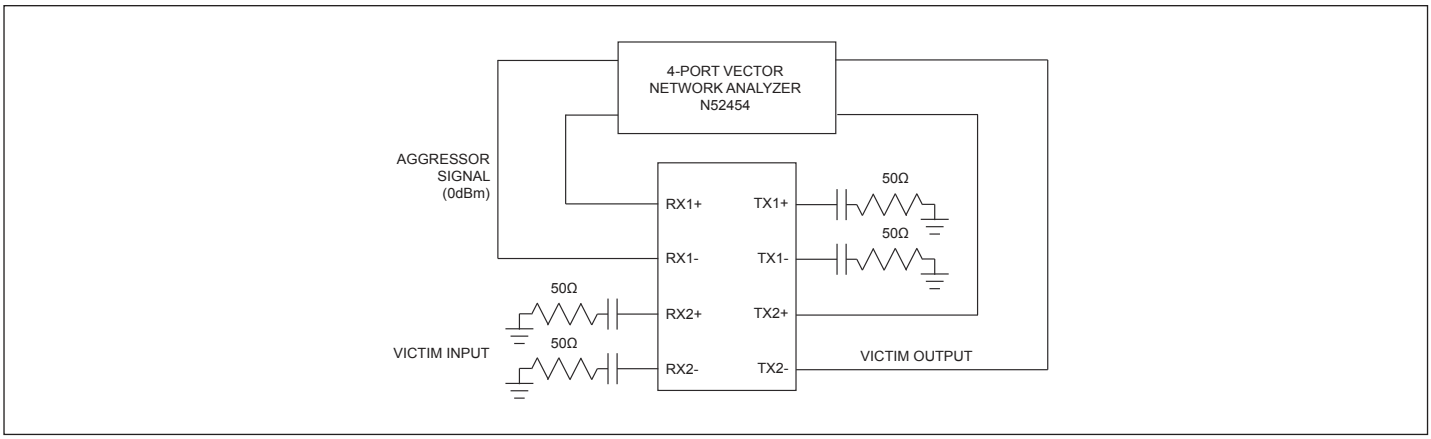


Figure 7. NEXT Channel-isolation Test Configuration

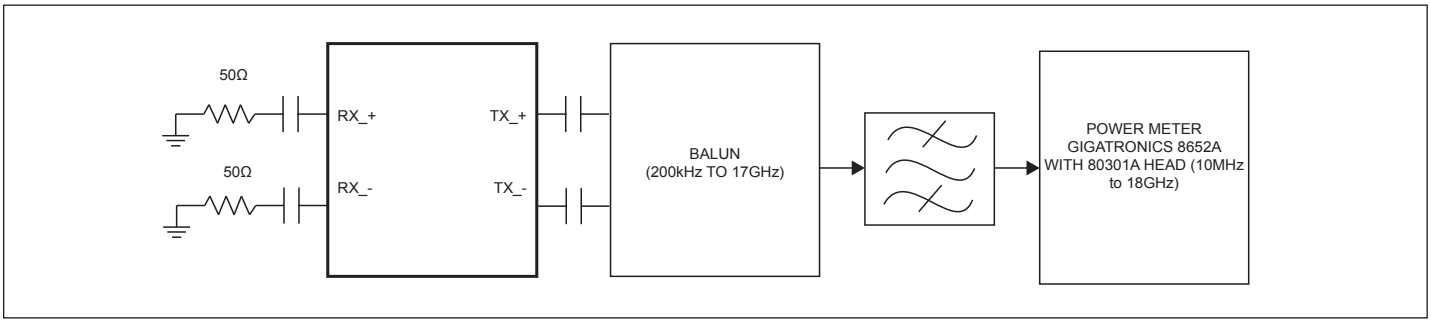
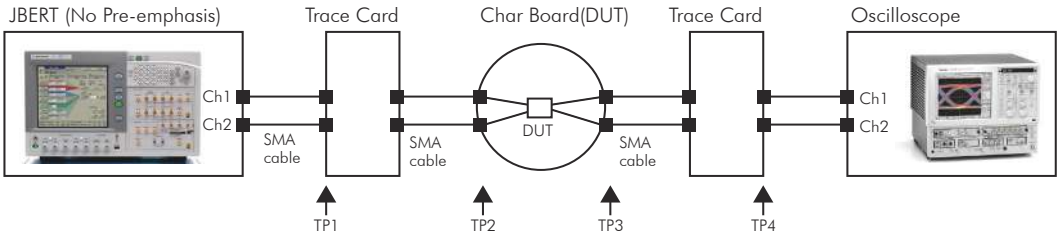


Figure 8. Noise Test Configuration



1) Trace card between TP1 and TP2 is designed to emulate 6-48" of FR4. Trace width -4 mils,100Ω differnetial impedance
2) All jitter is measured at a BER of 10-9
3) Residual jitter reflects the total jitter measured at TP4 jitter minus TP1 jitter
4) VDD = 1.8V, RT = 50Ω
5) The input signal from JBERT does not have any pre-emphasis.

Figure 9. Channel Measurement Setup

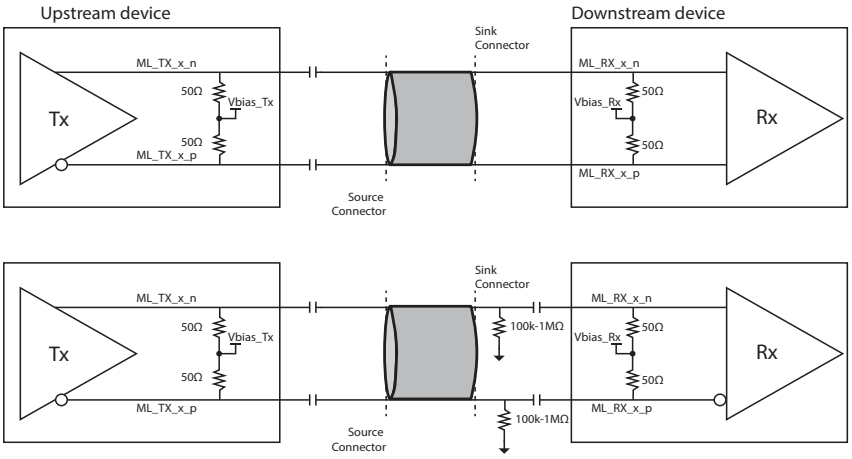


Figure 10. High-speed Channel Test Circuit

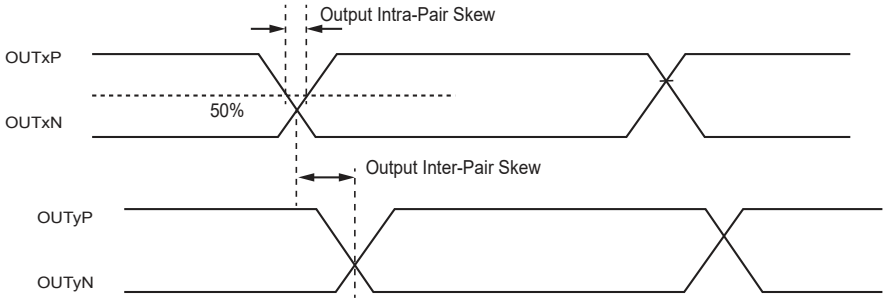
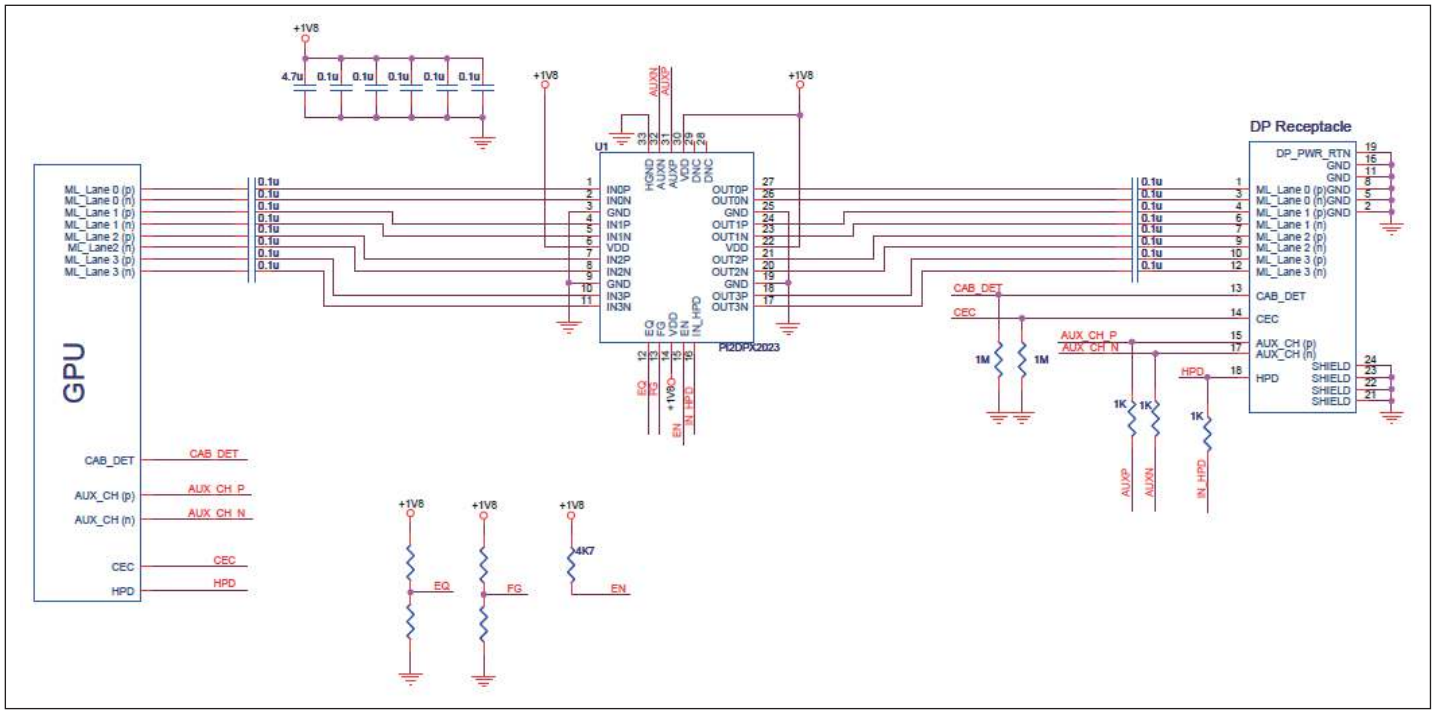


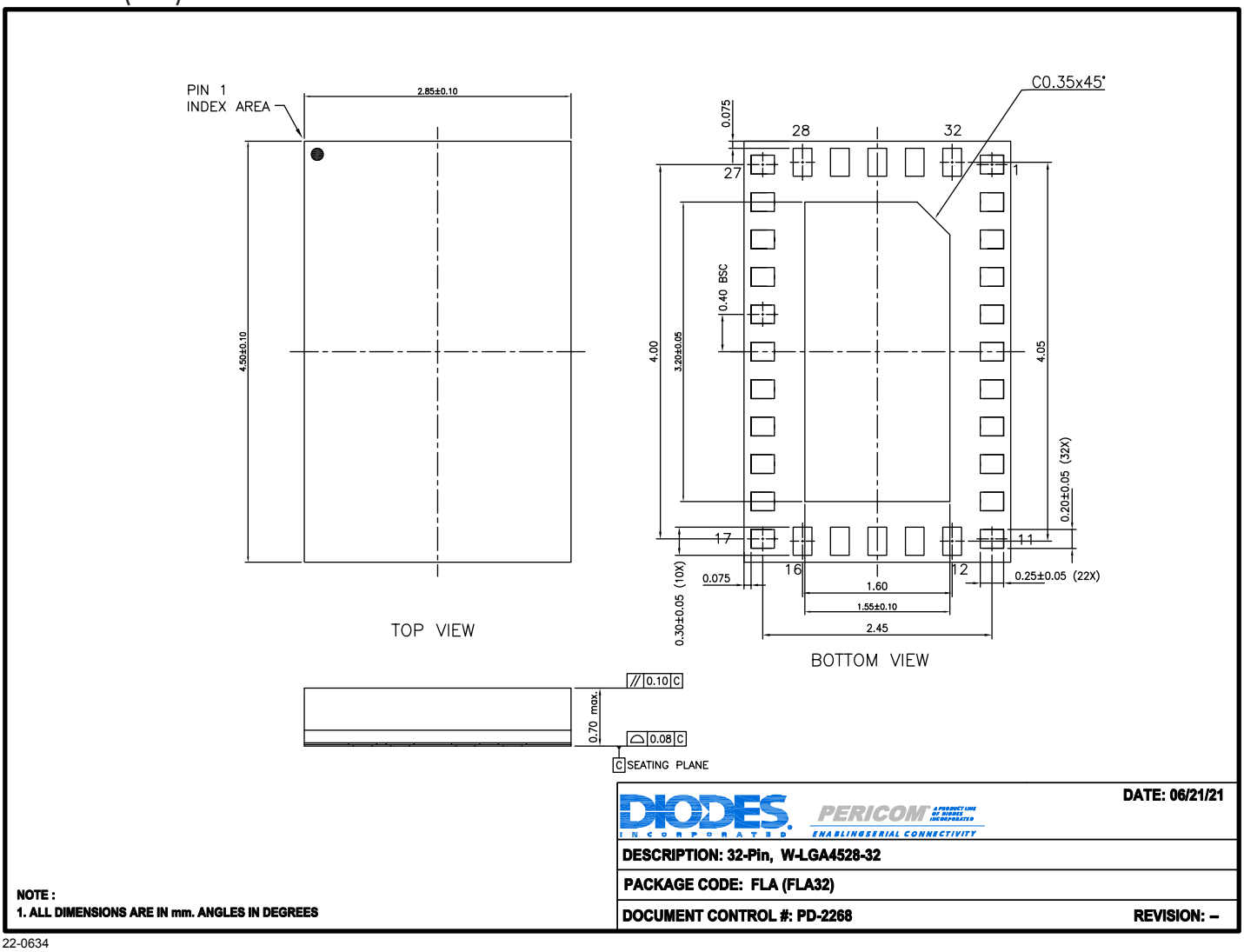
Figure 11. Intra and Inter-pair Differential Skew Definition

Application Schematics



Packaging Mechanical

32-WLGA (FLA)



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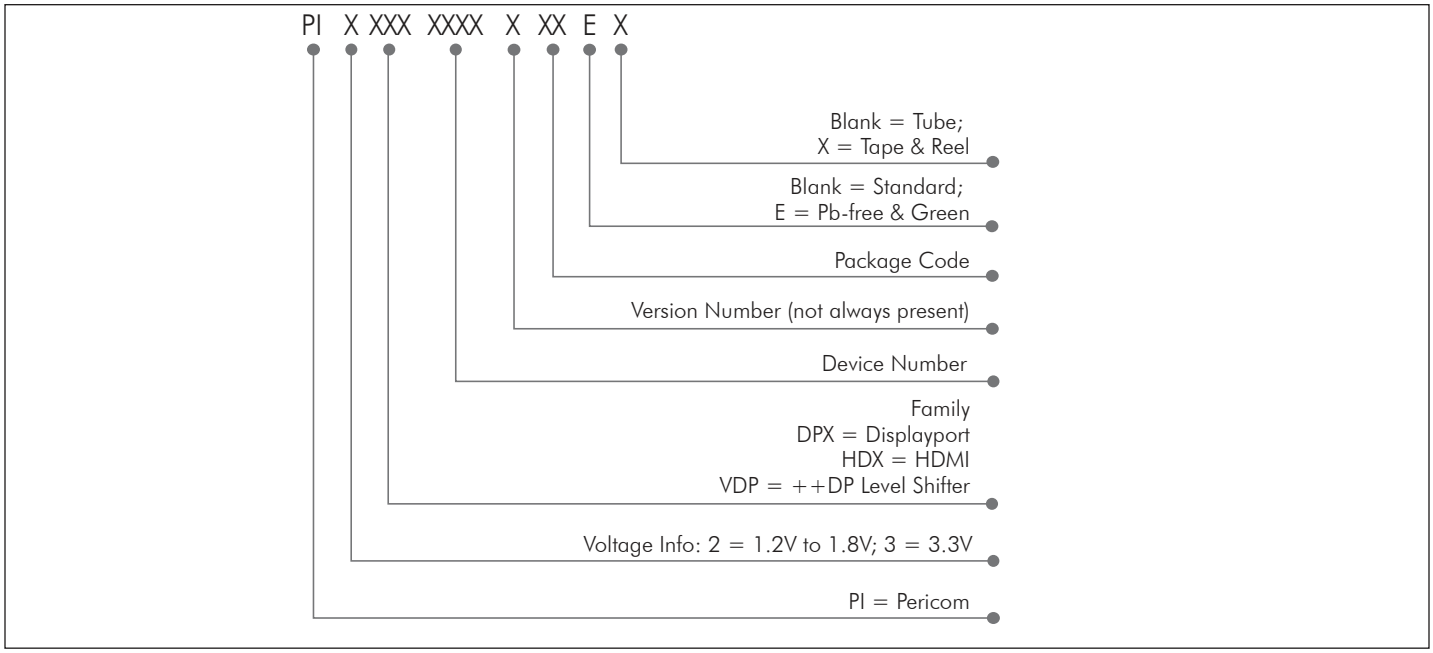
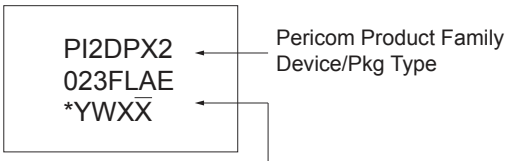
For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Device Naming Information



Part Marking



*: Die Rev
Y: Year
W: Week
1st X: Assembly Code
2nd X: Fab Code
Note: Date code per MA-1251

Tape & Reel Materials and Design

Carrier Tape

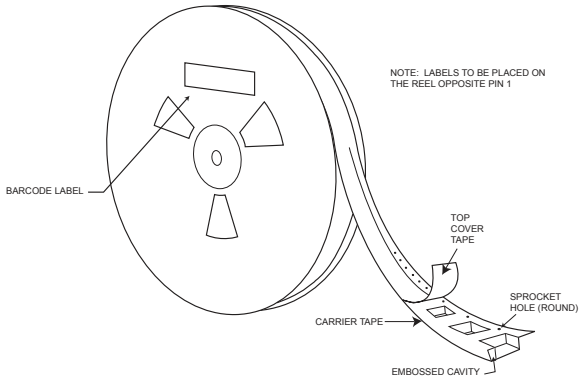
The pocketed carrier tape is made of conductive polystyrene plus carbon material (or equivalent). The surface resistivity is 106Ω/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See figures 3 and 4 for carrier tape dimensions.

Cover Tape

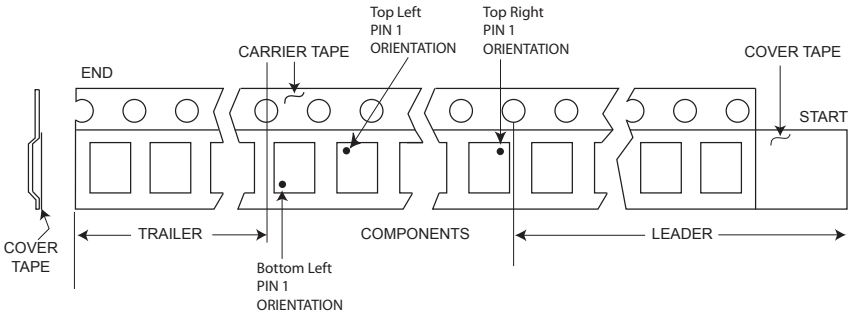
Cover tape is made of anti-static transparent polyester film. The surface resistivity is 107Ω/sq. Minimum to 1011Ω/sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20gm to 80gm (2N to 0.8N).

Reel

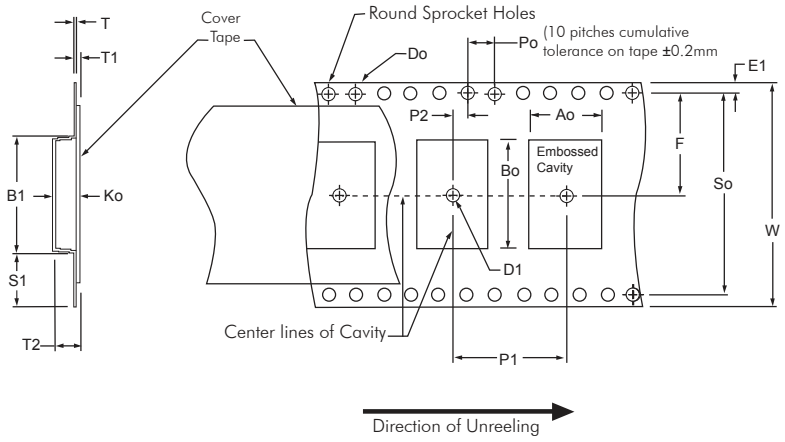
The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 107Ω/sq. minimum to 1011Ω/sq. maximum.



Tape & Reel Label Information



Tape Leader and Trailer Pin 1 Orientations



Standard Embossed Carrier Tape Dimensions

Tape & Reel Dimensions

Constant Dimensions

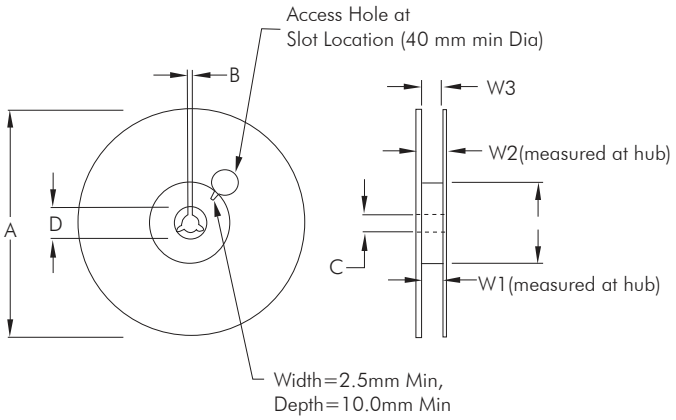
TAPE SIZE	D_0	D_1 (Min)	E_1	P_0	P_2	R (2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1-0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (3)		
44mm					2.0 ± 0.15				

Variable Dimensions

TAPE SIZE	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max)	W (Max)	A_0, B_0 &K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) or visit www.diodes.com/assets/MediaList-Attachments/Diodes-Tape-Reel-Tube.pdf	4.35	6.25	3.5 ± 0.05	N/A (4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4 ± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:

1. A_0, B_0, and K_0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16mm, 24mm, 32mm, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16mm through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S_1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where $D_o \geq S_1$.
4. S_o does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.



Reel Dimensions By Tape Size

TAPE SIZE	A	N (Min) (1)	W_1	W_2 (Max)	W_3	B (Min)	C	D (Min)
8mm	178 ± 2.0mm or 330 ± 2.0mm	60 ± 2.0mm or 100 ± 2.0mm	8.4 +1.5/-0.0mm	14.4mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0mm	18.4mm				
16mm	330 ± 2.0mm	100 ± 2.0mm	16.4 +2.0/-0.0mm	22.4mm				
24mm			24.4 +2.0/-0.0mm	30.4mm				
32mm			32.4 +2.0/-0.0mm	38.4mm				
44mm			44.4 +2.0/-0.0mm	50.4mm				

NOTE:
1. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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