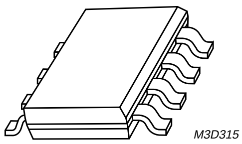



# PHK4NQ20T

TrenchMOS™ standard level FET

**Rev. 01 — 20 January 2003** **Product data**

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHK4NQ20T in SOT96-1 (SO8).

### 1.2 Features

- Low on-state resistance
- Surface mount package.

### 1.3 Applications

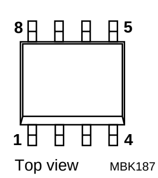
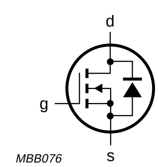
- DC-DC primary side switching
- General purpose switch.

### 1.4 Quick reference data

- $V_{DS} \leq 200$ V
- $I_D \leq 4$ A
- $P_{tot} \leq 6.25$ W
- $R_{DSon} \leq 130$ mΩ

## 2. Pinning information

**Table 1: Pinning - SOT96-1, simplified outline and symbol**

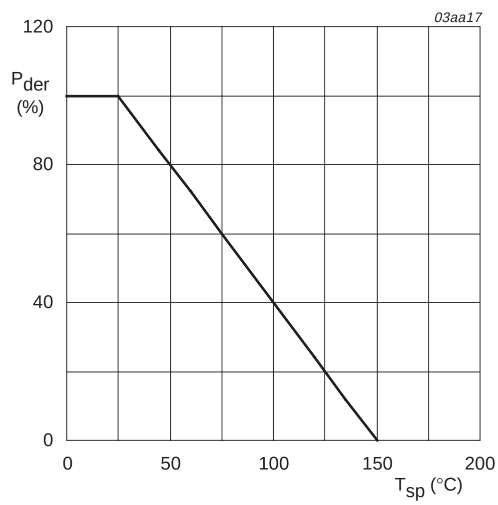
| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1,2,3 | source (s) |  SOT96-1 |  |
| 4 | gate (g) | | |
| 5,6,7,8 | drain (d) | | |

# 3. Limiting values

**Table 2: Limiting values**

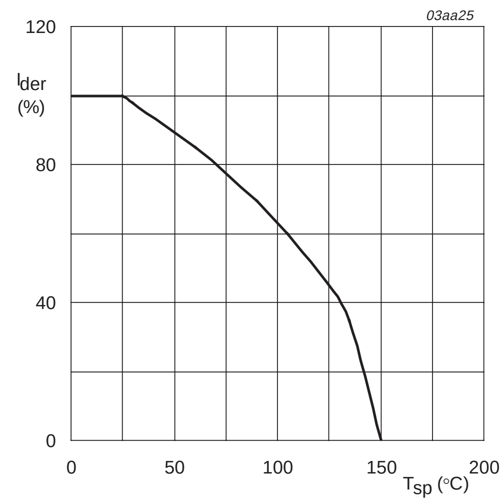
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C | - | 200 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | - | 200 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±20 | V |
| $I_D$ | drain current (DC) | $T_{sp}$ = 25 °C; $V_{GS}$ = 10 V; Figure 2 and 3 | - | 4 | A |
| | | $T_{sp}$ = 100 °C; $V_{GS}$ = 10 V; Figure 2 | - | 2.58 | A |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Figure 3 | - | 16 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C; Figure 1 | - | 6.25 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source (diode forward) current (DC) | $T_{sp}$ = 25 °C | - | 4 | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | - | 16 | A |




$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

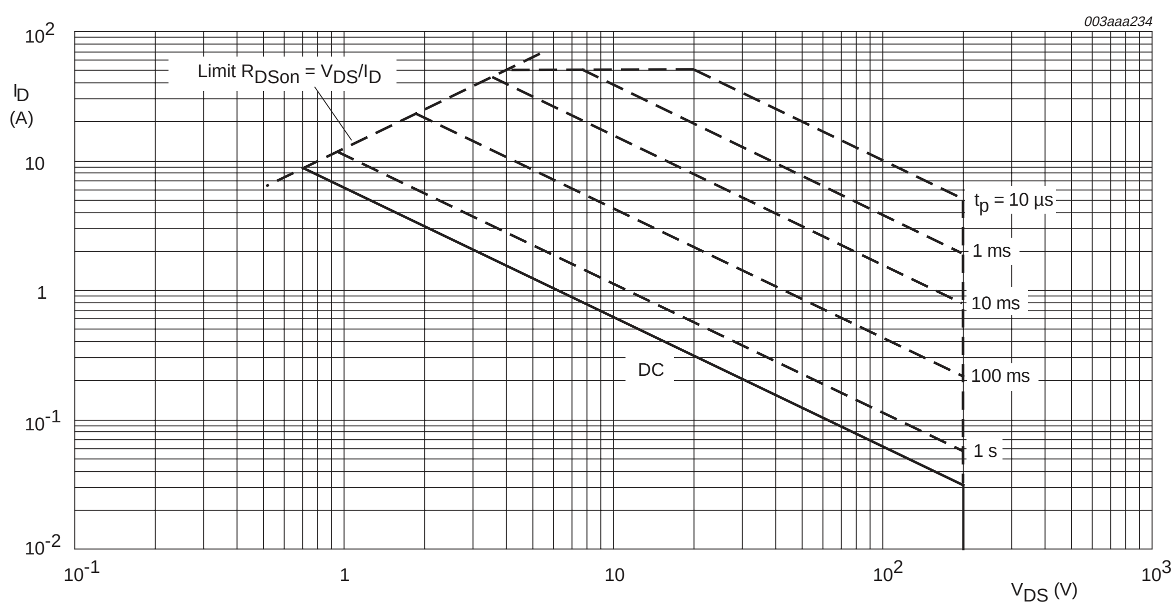
**Fig 1. Normalized total power dissipation as a function of solder point temperature.**




$V_{GS} \geq 10$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of solder point temperature.**




$T_{sp}$ = 25 °C; $I_{DM}$ is single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

# 4. Thermal characteristics

**Table 3: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | Figure 4 | - | - | 20 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint; mounted on printed-circuit board | - | 70 | - | K/W |

## 4.1 Transient thermal impedance

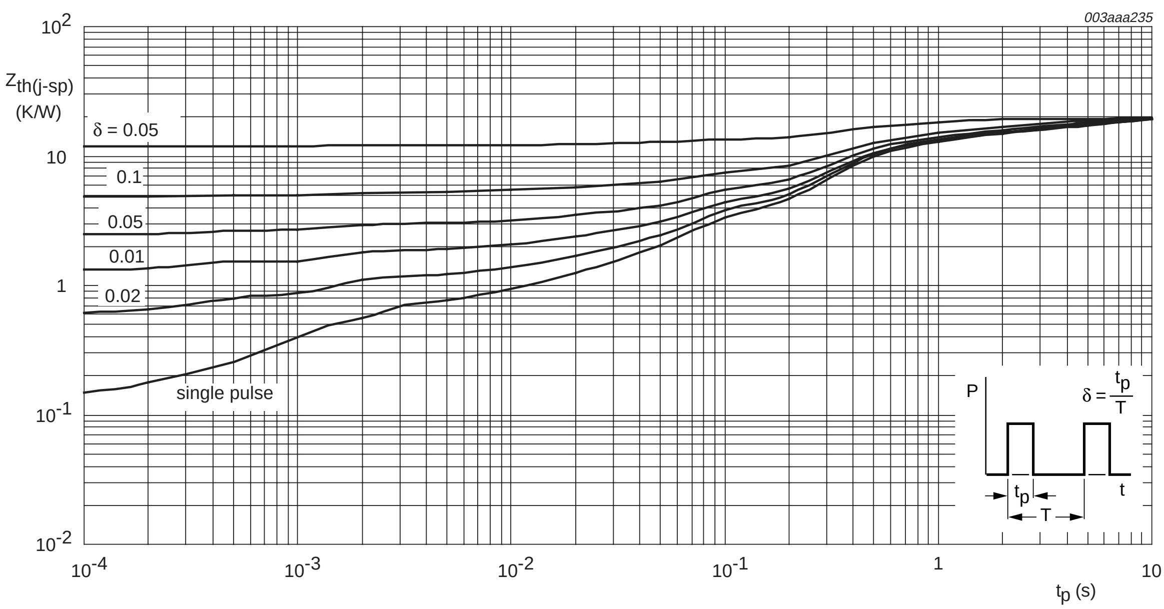


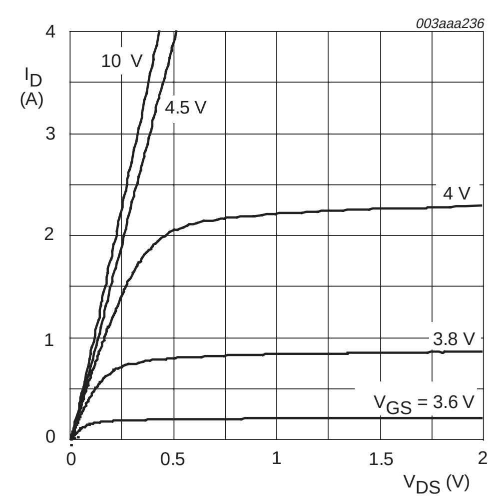

**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.**

## 5. Characteristics

**Table 4: Characteristics**

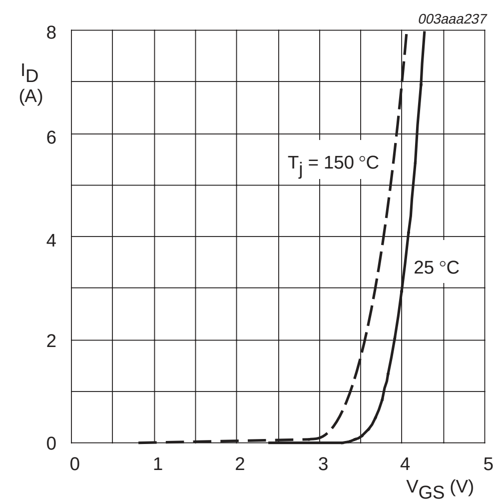
*$T_j$ = 25 °C unless otherwise specified*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 200 | - | - | V |
| | | $T_j$ = –55 °C | 178 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; Figure 9 | | | | |
| | | $T_j$ = 25 °C | 2 | 3 | 4 | V |
| | | $T_j$ = 150 °C | 1.2 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 4.5 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 160 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | 1 | µA |
| | | $T_j$ = 150 °C | - | - | 100 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±10 V; $V_{DS}$ = 0 V | - | 10 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 4 A; Figure 7 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 108 | 130 | mΩ |
| | | $T_j$ = 150 °C | - | 260 | 312 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 3 A | - | 110 | 150 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 4 A; $V_{DD}$ = 100 V; $V_{GS}$ = 10 V; Figure 13 | - | 26 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 4 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 8.7 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; Figure 12 | - | 1230 | - | pF |
| $C_{oss}$ | output capacitance | | - | 155 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 48 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 100 V; $I_D$ = 4 A; $V_{GS}$ = 10 V; $R_G$ = 6 Ω | - | 13 | - | ns |
| $t_r$ | rise time | | - | 10 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 35 | - | ns |
| $t_f$ | fall time | | - | 14 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 4 A; $V_{GS}$ = 0 V; Figure 11 | - | 0.81 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 4 A; $dI_S/dt$ = –100 A/µs; $V_R$ = 120 V; $V_{GS}$ = 0 V | - | 104 | - | ns |
| $Q_r$ | recovered charge | | - | 245 | - | nC |



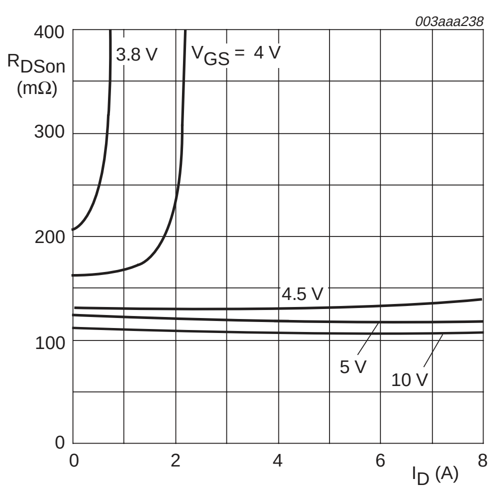

$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



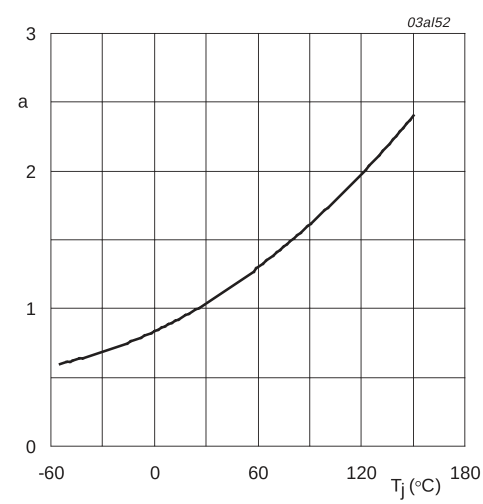

$T_j$ = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



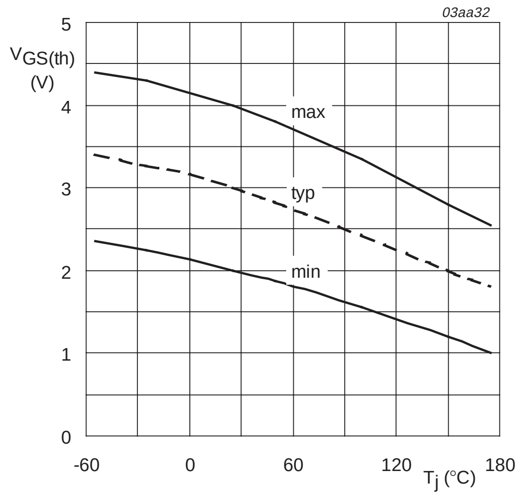

$T_j$ = 25 °C

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



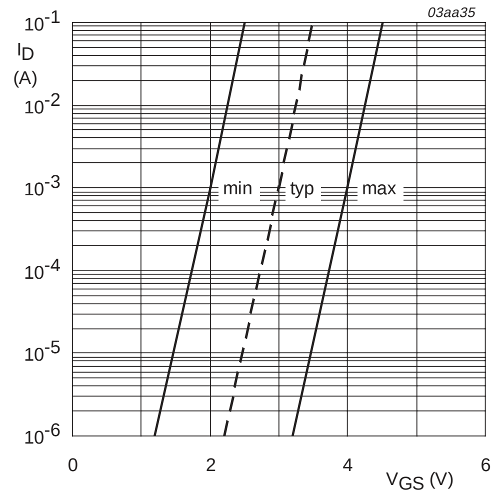

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



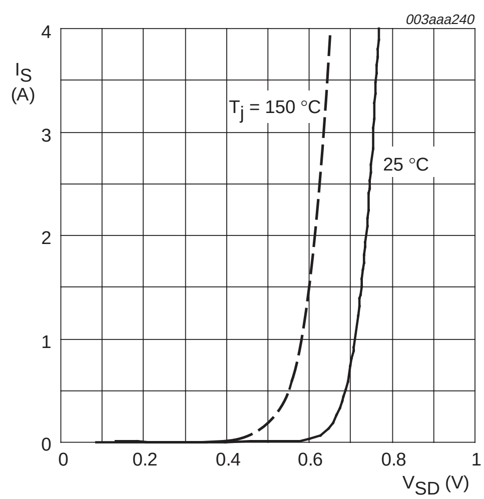

$I_D$ = 1 mA; $V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



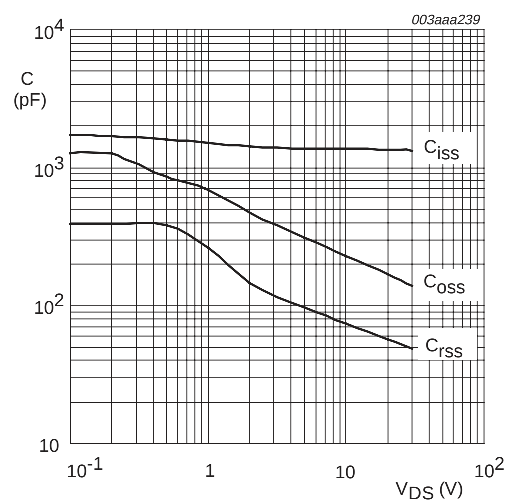

$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



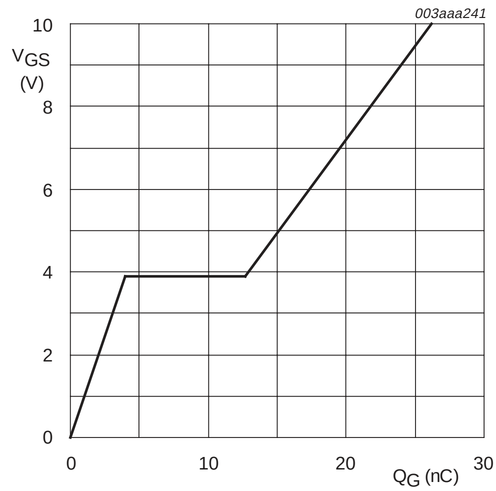

$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 11. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**




$V_{GS}$ = 0 V; f = 1 MHz.

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**

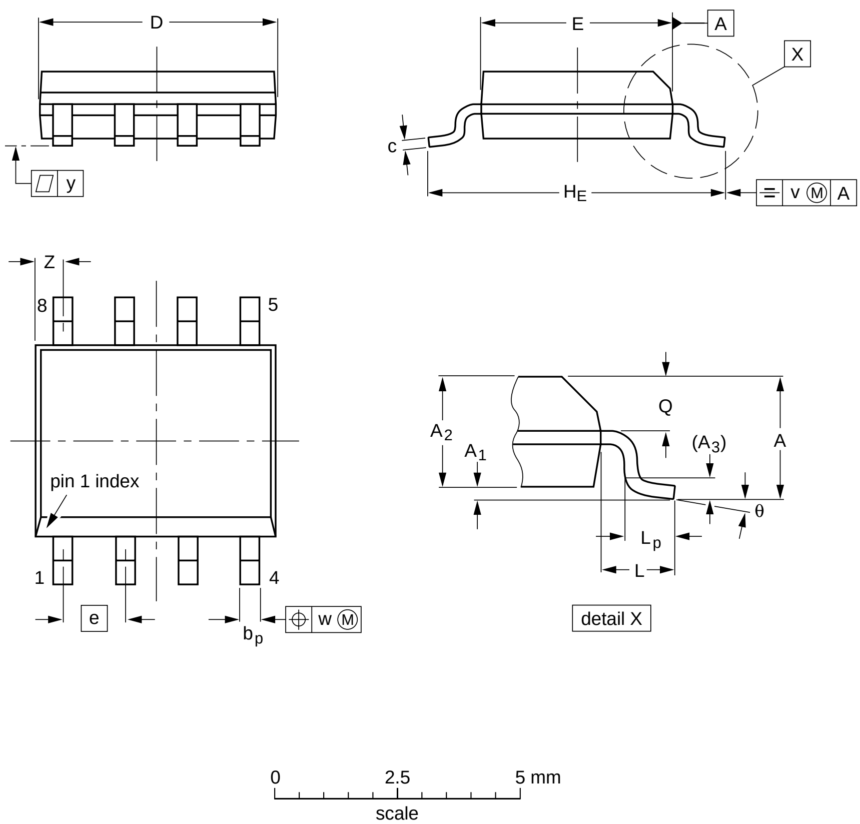



$I_D$ = 4 A; $V_{DD}$ = 100 V

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

## 6. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~97-05-22~~<br>99-12-27 |

**Fig 14. SOT96-1 (SO8).**

# 7. Revision history

**Table 5: Revision history**

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 01 | 20030120 | - | Product data (9397 750 10773) |

# 8. Data sheet status

| Level | Data sheet status[1] | Product status[2][3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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