

ADVANCE INFORMATION

December 1996

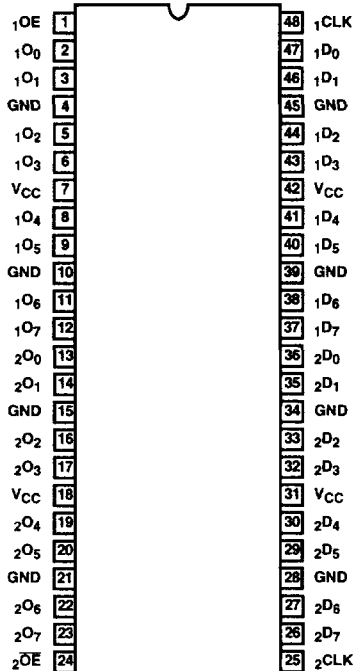
Fast CMOS 16-Bit Register (Three-State)

Features

- Advanced 0.6 micron CMOS Technology
- $V_{CC} = 5V \pm 10\%$
- Balanced Output Drivers: $\pm 12mA$
- Output Impedance 35Ω (Typical)
- Typical V_{OLP} (Output Ground Bounce) $< 0.5V$ at $V_{CC} = 5V, T_A = 25^\circ C$
- Bus Hold Retains Last Active Bus State During Three-State
- Hysteresis on All Inputs

Pinout

CD74FCT162Q374T
(SSOP, TSSOP)
TOP VIEW



Description

The CD74FCT162Q374T is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and three-state outputs. The Output Enable ($\chi\overline{OE}$) and clock (χCLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When \overline{OE} is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the χO_x outputs on the LOW-to-HIGH transition of the clock input.

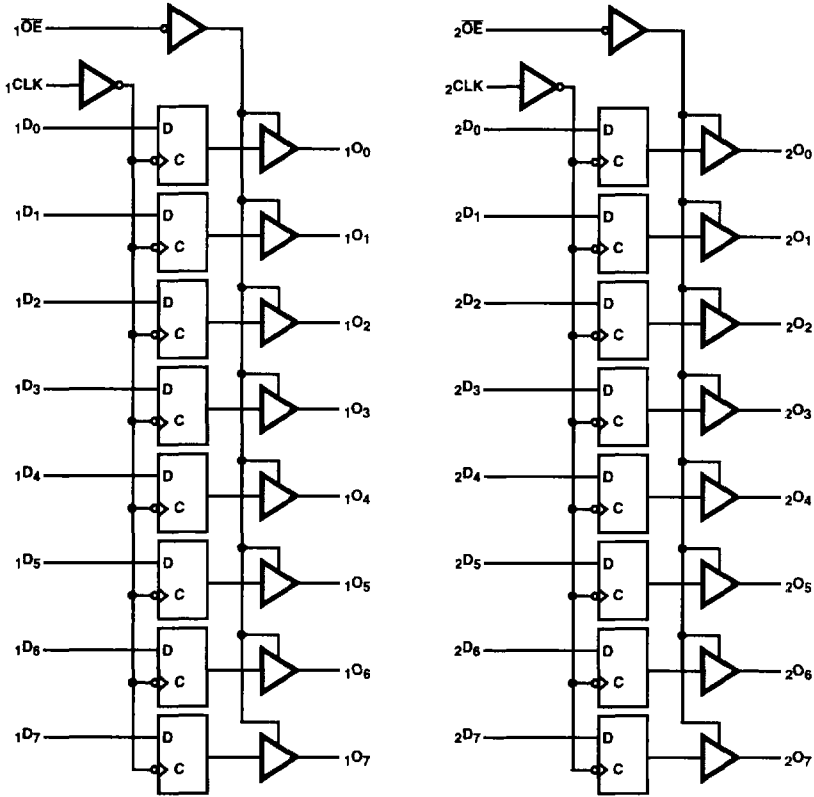
The CD74FCT162Q374T is designed with current limited resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This device features a typical output impedance of 35Ω eliminating the need for external terminating resistors for most bus interface applications. This noise suppression benefit is designated by the letter "Q" (for quiet) in the part number.

The CD74FCT162Q374T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT162Q374TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374ETSM	-40 to 85	48 Ld SSOP	M48.300-P

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS
	$x\overline{D}_x$	$x\overline{CLK}$	$x\overline{OE}$	xO_x
High-Z	X	L	H	Z
	X	H	4H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance
- ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$x\overline{CLK}$	Clock Inputs
$x\overline{D}_x$	Inputs (Note 2)
$x\overline{O}_x$	Three-State Outputs
GND	Ground
VCC	Power

NOTE:

- 2. For the CD74FCT162Q374T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

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 D.D. 5V FCT
 QUIET SERIES

CD74FCT162Q374T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS	
CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$							
Input Capacitance (Note 9)	C_{IN}	$V_{IN} = 0\text{V}$	-	4.5	6	pF	
Output Capacitance (Note 9)	C_{OUT}	$V_{OUT} = 0\text{V}$	-	5.5	8	pF	
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or V_{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	$V_{CC} = \text{Max}$, Outputs Open $\chi_{OE} = \text{GND}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	60	100	$\mu\text{A}/\text{MHz}$
Total Power Supply Current (Note 13)	I_C	$V_{CC} = \text{Max}$, Outputs Open $f_{CP} = 10\text{MHz}$, 50% Duty Cycle $\chi_{OE} = \text{GND}$ $f_I = 5\text{MHz}$, 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.6	1.5 (Note 12)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	1.1	3.0 (Note 12)	mA
		$V_{CC} = \text{Max}$, Outputs Open $f_{CP} = 10\text{MHz}$, 50% Duty Cycle $\chi_{OE} = \text{GND}$ 16 Bits Toggling $f_I = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.0	5.5 (Note 12)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	7.5	19.0 (Note 12)	mA

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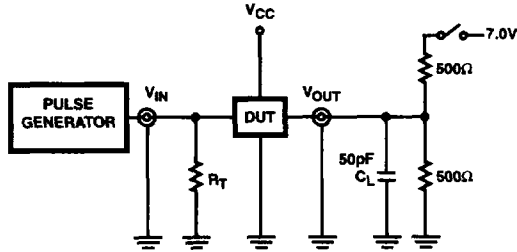
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $x\overline{D}_X$ to xO_X	t_{PLH} , t_{PHL}	$C_L = 50$ pF $R_L = 500\Omega$	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
Propagation Delay xLE to xO_X	t_{PLH} , t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	4.0	ns
Output Enable Time $x\overline{OE}$ to xO_X	t_{PZH} , t_{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.8	ns
Output Disable Time (Note 16) $x\overline{OE}$ to xO_X	t_{PHZ} , t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	4.0	ns
Setup Time HIGH or LOW, $x\overline{D}_X$ to xLE	t_{SU}		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns
Hold Time HIGH or LOW, $x\overline{D}_X$ to xLE	t_H		1.5	-	1.5	-	1.5	-	1.0	-	3.0	-	ns
xLE Pulse Width HIGH (Note 16)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	-	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at $V_{CC} = 5.0V$, $25^\circ C$ ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ} , t_{PZL}	Closed
t_{PHZ} , t_{PZH} , t_{PLH} , t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 t_r , $t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

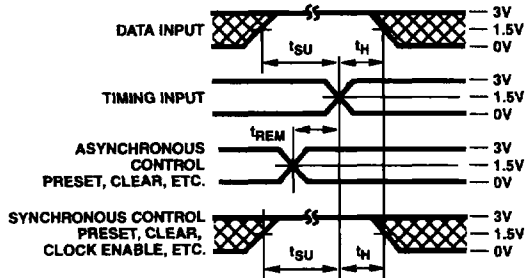


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

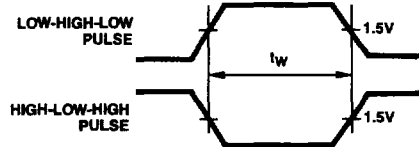


FIGURE 3. PULSE WIDTH

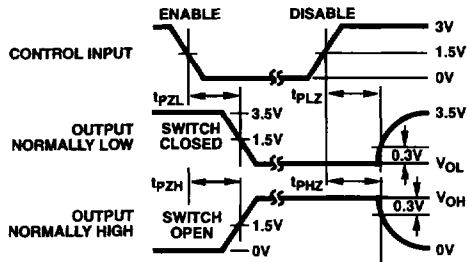


FIGURE 4. ENABLE AND DISABLE TIMING

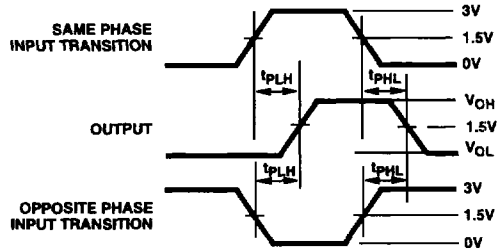


FIGURE 5. PROPAGATION DELAY

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