User's Guide

TIOx1x2x Evaluation Module

ABSTRACT

This user guide describes the features and operation of the TIOx1x2xEVM Evaluation Module. It can be used as a reference to help designers through the device performance evaluation process, and also promotes fast product development. The TIOx1x2xEVM can be configured to support all devices in the TIOL11xx and TIOS10xx product families and comes with both a TIOL1123 and TIOS1023 device installed by default. The EVM contains an industry standard 4-pin M12 connector in a Class A 2-channel configuration with one IO-Link communication channel and one digital output (DO) channel. The low-voltage digital input and output signals are easily accessible for connection to a microcontroller and test equipment through both header pins and test points. The board can also be directly connected to a number of TI microcontroller boards.

Table of Contents

Trademarks

1 Introduction

1.1 Features

This EVM supports the following features:

- TIOL1123 IO-Link Device Transceiver with Low Residual Voltage and Integrated Surge Protection with 3.3-V LDO
- Can also be assembled for evaluation with the following IO-Link transceivers TIOL112, TIOL1125, TIOL111, TIOL1113, TIOL1115
- TIOS1023 Digital Sensor Output Driver with Integrated Surge Protection and 3.3 V LDO
- Can also be assembled for evaluation with the following Digital Sensor Output Drivers TIOS102, TIOS1025, TIOS101, TIOS1013, TIOS1015
- Industry standard 4-pin M12 connector for a 2-channel configuration (one IO-Link plus one DO)
- Footprints for TVS diodes or extra filtering components to protect from noise and transient pulses
- Current limits are configurable with potentiometers or a dedicated resistor option selected with a jumper
- Fault conditions visually indicated with LEDs

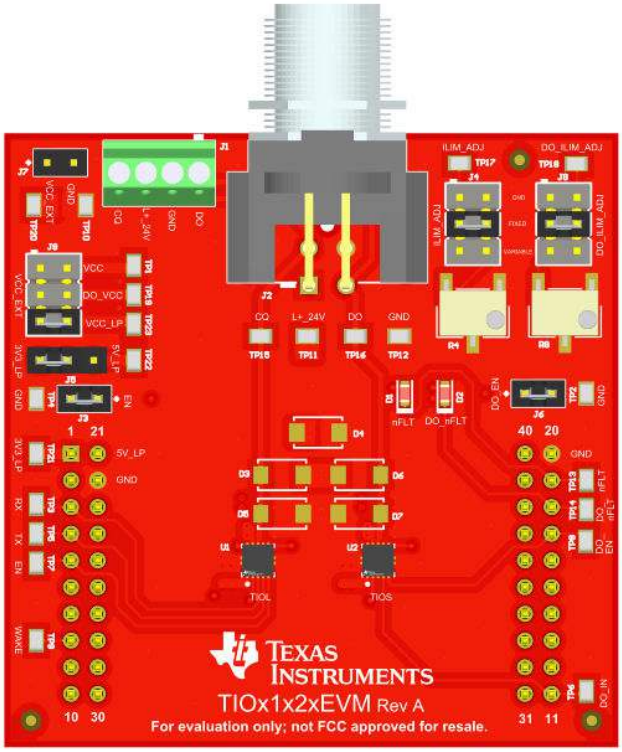


Figure 1-1. TIOx1x2xEVM Image

1.2 Description

The TIOx1x2xEVM provides user with the ability to evaluate all features of the TIOL1123 and TIOL1023 devices. The EVM can accept any of the other devices in the TIOL11xx and TIOS10xx product families if a different version of the device needs to be evaluated.

The EVM contains an industry standard 4-pin M12 connector with a Class A 2-channel configuration implementing one IO-Link communication channel from the TIOL1123 and one digital output channel from the TIOS1023. A screw terminal block for bare wire connections or external loads is also provided for the L+_24V, GND, CQ, and DO nets.

The low-voltage digital input and output signals are easily accessible for connection to test equipment or a microcontroller through both header pins and test points. The profile of the board also allows it to be directly connected to a number of TI microcontroller boards for rapid prototyping.

2 EVM Setup and Features Explained

2.1 Evaluation Equipment

The following equipment can be used to evaluate the performance of the TIOL11xx and TIOS10xx devices.

- A power supply capable of supplying 24 V across L+ (supply) and GND (ground)
- A power supply capable of supplying 3.3 V or 5 V (if a TIOL11xx or TIOS10xx device without an internal LDO is used)
- An oscilloscope and probes capable of tolerating voltage as large as the L+ supply voltage
- The logic interface pins (TX, EN, RX, NFAULT, and WAKE) can interface to a microcontroller, pattern generator, or logic analyzer using 3.3-V or 5-V logic levels (to match the VCC_IN or VCC_OUT voltage).
- If connecting to an IO-Link master node, an appropriate cable with either 3 or 4 wires for the L+, CQ, GND, and optional DO signal can be connected to the 4-pin M12 connector, the wire terminal (J1), or test points.
- External loading components such as resistors, inductors, capacitors, and so on. Can be connected to the wire terminal (J1).

2.2 Power Overview

L+ is the primary supply voltage for the board and should be between 7-V and 36-V if the TIOL11xx device is evaluated, but can be between 5-V and 36-V if only the TIOS10xx device is evaluated. The power supply should be connected to pins 1 (L+) and 3 (GND) of the M12 connector (J2), pins 3 (L+) and 2 (GND) of the wire terminal (J1), or test points TP11 (L+) and TP12 (GND).

The 3.3-V or 5-V digital logic voltage and board configuration may differ depending on which TIOL11xx and TIOS10xx devices are installed. The EVM will support all versions of the TIOL11xx and TIOS10xx devices, both with and without an LDO of either 3.3 V or 5 V. By default, a TIOL1123 and TIOS1023 will be installed and allow each device to operate independently and supply its own logic level voltage derived from the single L+ power supply. These devices are also compatible with the standard 3.3-V logic level of most TI microcontrollers that may be used with this EVM.

If the board is configured with a version of the TIOL11xx and TIOS10XX that does not have an internal LDO, such as the TIOL112 and TIOS102, then an external power supply will be needed for the logic level 3.3-V or 5-V. An external power supply can be connected to pins 1 (VCC_EXT) and 2 (GND) of header J7 or to test points TP20 (VCC_EXT) and TP10 (GND).

If a 3.3-V or 5-V voltage is supplied through pin 1 (3.3 V), pin 21 (5 V), and pin 22 (GND) of header J10, the appropriate voltage can be used to supply the digital logic voltage to the board. Place a shunt on jumper J5 between pins 1 and 2 for the 3.3-V level, or pins 2 and 3 for the 5-V level. This will connect the voltage to pin 6 (VCC_LP) of the voltage connection header J9 and allow it to be used as the external supply voltage of the board. It also allows connection to the power planes of the board supplying the device VCC_IN pins through a shunt on pins 5 and 6 of header J9.

The VCC_IN and VCC_OUT pins of the TIOL11xx and TIOS10xx are connected to separate internal planes on the board to allow any combination of devices to be configured and powered properly. The power plane net for the TIOL11xx device (U1) is called VCC, and the power plane net for the TIOS10xx device (U2) is called DO_VCC. Placing the shunt on pins 1 and 2 of header J9 will connect VCC, and a shunt placed on pins 3 and 4 will connect DO_VCC to the external supply voltage net. The LDO of either the TIOL11xx or TIOS10xx can be used to supply the voltage for the board and other devices as well. The shunt locations on the connection header J9 would remain the same, but the direction of current is different.

2.3 Current Limit Overview

The output current limit for the TIOL11xx and TIOS11xx devices can be configured through the ILIM_ADJ pins. There is an external resistor on the ILIM_ADJ pin with a maximum settable current limit of 350 mA.

Connecting the ILIM_ADJ pin to GND increases the current limit to 500 mA for both the TIOL112x and TIOS102x devices. This also allows the TIOL112x devices to enter a master mode, and allows it to source or sink a minimum of 500 mA to generate a wake-up request. Also, while in this mode, the device enables a small current sink of 5 mA (minimum) as required in the IO-Link standard specification, which calls for a minimum limit of 500

mA, it disables the current fault indication, as well as the Output Disable and Auto Recovery features of the device.

Leaving the ILIM_ADJ pin floating sets the output current limit for the TIOL112x and TIOS102x devices to 300 mA, but disables the Output Disable and Auto Recovery if an over-current condition longer than the current fault blanking time (t_{sc}) occurs. The NFAULT pin will still report this over-current fault condition, but the output will not be disabled and is useful when driving certain capacitive loads that may require a charging time greater than t_{sc}.

The EVM allows both the TIOL112x and TIOS102x ILIM_ADJ pins to be fully and independently configured through headers J4 (TIOL112x) and J8 (TIOS102x). Placing a shunt on pins 3 and 4 of these headers connects the device's ILIM_ADJ pin with a fixed resistor, that is by default 25.5 kΩ. Placing a shunt between pins 5 and 6 connects a variable resistance through the 100 kΩ potentiometers that can be adjusted to the desired current limit for each device. Place a shunt between pins 1 and 2 to short the ILIM_ADJ pins to GND. Remove the shunt from the headers completely to allow the ILIM_ADJ pins to float.

2.4 Fault Reporting (NFAULT)

The TIOL112x and TIOS102x can both monitor for three types of fault conditions and have a single fault reporting pin (NFAULT) that is used to indicate that one or more of these faults are currently present in the device. The NFAULT pin is driven low if either a current fault condition is detected, the die temperature has exceeded the thermal warning threshold T_{WRN}, or supply has dropped below the under voltage lock out (UVLO) threshold. NFAULT returns to a high-impedance state as soon as all three fault conditions clear.

The NFAULT signal for the TIOL112x (NFAULT) can be monitored through pin 19 of header J11, test point TP13, and LED D1. Likewise, the NFAULT signal for the TIOS1012x (DO_NFAULT) can be monitored through pin 18 of header J11, test point TP14, and LED D2.

2.5 Transient Protection and Custom Loads

The TIOx1x2x family of devices include on-chip ESD (IEC 61000-4-2) and surge (IEC 6100-4-5) protection, which eliminates or reduces the size of any TVS diodes. Pads for external diodes (D3 – D7) are included on the board, allowing the EVM to be modified to support the user's requirements. These pads can also be used for other types of complex loads such as resistors, capacitors, and inductors that may be required during the evaluation.

2.6 IO-Link Communication (TIOL112x)

The communication and control signals of the TIOL112x (TX, RX, EN, WAKE, and NFAULT) can be connected to a microcontroller that is implementing an IO-Link protocol stack through pins 3 (RX), 4 (TX), 5 (EN), 8 (WAKE) of header J10 as well as pin 19 (NFAULT) of header J11. Test points for each of these signals are also provided next to the header pins, allowing the signals to be monitored or connected to additional test equipment, such as oscilloscope probes and logic analyzers.

2.7 Digital Sensor Output Driver Control (TIOS102x and TIOS112x)

Both the TIOS102x and TIOL112x devices can be used in a push-pull, high-side, or low-side configuration to drive resistive, large capacitive or large inductive loads.

The TIOS102x control signals can be connected to a microcontroller or test equipment through pins 11 (DO_IN), 17 (DO_EN), and 18 (DO_nFAULT) of header J11. Test points for each of these signals are also provided next to the header pins, allowing the signals to be monitored or connected to additional test equipment, such as oscilloscope probes and logic analyzers. The external load to be driven by the switch can be connected to the wire terminal connector J1, M12 connector J2, or test points TP16 (DO), TP11 (L+_24V), and TP12 (GND).

The TIOL112x can operate as a digital sensor output driver similar to the TIOS102x. The control signals are the same as the TIOS102x with the exception to the pin names where the TX pin is the Input, and the CQ is the Output. These signals can be connected to a microcontroller or test equipment through pins 4 (TX) and 5 (EN) of header J10 as well as pin 19 (NFAULT) of header J11. Test points for each of these signals are also provided next to the header pins, allowing the signals to be monitored or connected to additional test equipment, such as oscilloscope probes and logic analyzers. The external load to be driven by the switch can be connected to the wire terminal connector J1, M12 connector J2, or test points TP15 (CQ), TP11 (L+_24V), and TP12 (GND).

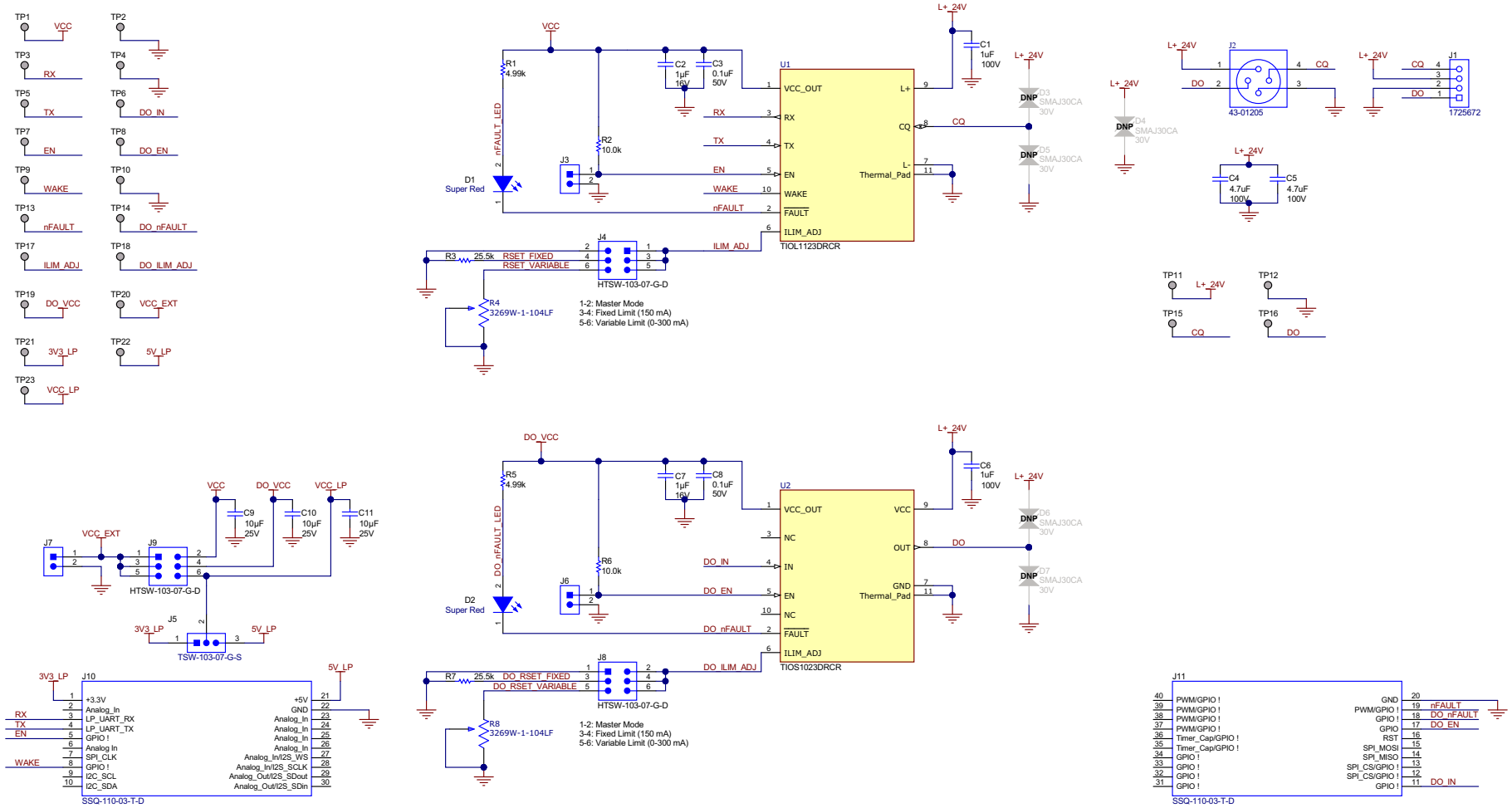
2.8 EVM Jumper Settings

Jumper	Description	Setting	Result
J1	IO-Link, Digital Output Port Wire Terminal Connector	DO	Digital Output Port (TIOS102x)
		GND	Ground
		L+_24V	Supply Voltage (24 V typical)
		CQ	IO-Link Output Port (TIOL112x)
J2	IO-Link, Digital Output Port Class A M12-4 connector	DO	Digital Output Port (TIOS102x)
		GND	Ground
		L+_24V	Supply Voltage (24 V typical)
		CQ	IO-Link Output Port (TIOL112x)
J3	TIOL112x	EN-GND	Shunt disables the transmitter or output driver
		EN-OPEN (no shunt)	Enables the transmitter or output driver
J4	TIOL112x Current Limit Adjustment	GND	TIOL112x configured in master mode. Current limit is at least 500 mA, Output Disable and Auto Recovery disabled, NFAULT indication during fault disabled
		FIXED	Current limit fixed by 25.5-kΩ resistor (approximately 180 mA)
		VARIABLE	Current limit variable up to 350 mA by adjusting the potentiometer
		OPEN (no shunt)	Current limit set to 300 mA, Output Disable and Auto Recovery disabled, NFAULT indication during fault enabled
J5	Microcontroller supplied voltage selection	3V3_LP	Shunt on pins 1 and 2 will connect 3V3_LP (J10 pin 1) to the board's VCC_LP rail
		5V_LP	Shunt on pins 2 and 3 will connect 5V_LP (J10 pin 21) to the board's VCC_LP rail
J6	TIOS102x Enable	DO_EN-GND	Shunt disables the output driver
		EN-OPEN (no shunt)	Enables the output driver
J7	External Low-Voltage Supply Connection	VCC_EXT (no shunt)	Connect an external 3.3-V or 5-V power supply if using a non-LDO version of the TIOL112 or TIOS102
J8	TIOS102x Current Limit Adjustment	GND	Current limit is at least 500 mA
		FIXED	Current limit fixed by 25.5-kΩ resistor (approximately 180 mA)
		VARIABLE	Current limit variable up to 350 mA by adjusting the potentiometer
		OPEN (no shunt)	Current limit set to 300 mA, Output Disable and Auto Recovery disabled, NFAULT indication during fault enabled
J9	Low-Voltage Supply selection	VCC	Shunt on pins 1 and 2 will connect the VCC_EXT rail to the TIOL112x rail
		DO_VCC	Shunt on pins 3 and 4 will connect the VCC_EXT rail to the TIOS102x rail
		VCC_LP	Shunt on pins 5 and 6 will connect the VCC_EXT rail to the VCC_LP rail
J10	Microcontroller and GPIO Connection	OPEN (no shunt)	Can be used to connect the following nets to a microcontroller or test equipment (3V3_LP, 5V_LP, GND, RX, TX, EN, and WAKE)
J11	Microcontroller and GPIO Connection	OPEN (no shunt)	Can be used to connect the following nets to a microcontroller or test equipment (nFAULT, DO_nFAULT, DO_EN, and DO_IN)

3 Schematic and Bill of Materials

The EVM schematic and bill of materials can be referenced for circuit design or component questions.

3.1 Schematic



3.2 Bill of Materials

Table 3-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C6	2	1uF	CAP, CERM, 1 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805	0805	CGA4J3X7S2A105K125AB	TDK
C2, C7	2	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	885012206052	Wurth Elektronik
C3, C8	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX
C4, C5	2	4.7uF	CAP, CERM, 4.7 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 1210	1210	CGA6M3X7S2A475K200AB	TDK
C9, C10, C11	3	10uF	CAP, CERM, 10 µF, 25 V,+/- 10%, X7R, 1206	1206	C3216X7R1E106K160AB	TDK
D1, D2	2	Super Red	LED, Super Red, SMD	LED_0603	150060SS75000	Wurth Elektronik
J1	1		Terminal Block, 4x1, 2.54 mm, Green, TH	Terminal Block, 4x1, 2.54 mm, TH	1725672	Phoenix Contact
J2	1		M12 Socket, Backmounting, 4Pos, Gold, R/A, TH	M12 Socket, Backmounting, 4Pos, R/A, TH	43-01205	Conec
J3, J6, J7	3		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J4, J8, J9	3		Header, 2.54mm, 3x2, Gold, TH	Header, 2.54mm, 3x2, Gold, TH	HTSW-103-07-G-D	Samtec
J5	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J10, J11	2		Receptacle, 2.54mm, 10x2, Tin, TH	10x2 Receptacle	SSQ-110-03-T-D	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R5	2	4.99k	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF4991X	Panasonic
R2, R6	2	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America
R3, R7	2	25.5k	RES, 25.5 k, 1%, 0.1 W, 0603	0603	RC0603FR-0725K5L	Yageo
R4, R8	2		100 kOhms 0.25W, 1/4W Gull Wing Surface Mount Trimmer Potentiometer Cermet 12 Turn Top Adjustment	SMD	3269W-1-104LF	Bourns
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	6		Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik

Table 3-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23	23		Test Point, SMT	Test Point, SMT	S2751-46R	Harwin
U1	1		IO-Link Device Transceiver with Low Residual Voltage and Integrated Surge Protection, VSON10	VSON10	TIOL1123DRCR	Texas Instruments
U2	1		Digital Sensor Output Driver with Integrated Surge Protection, VSON10	VSON10	TIOS1023DRCR	Texas Instruments
D3, D4, D5, D6, D7	0	30V	Diode, TVS, Bi, 30 V, 48.4 Vc, 400 W, 8.3 A, SMA (non-polarized)	SMA (non-polarized)	SMAJ30CA	Littelfuse

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2022	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265