Freescale Semiconductor, Inc.
Datasheet: Technical Data

Document Number: MC13201
Rev. 2, 04/2015

MC13201 Datasheet with Addendum

Rev. 2 of the MC13201 datasheet has two parts:

- The addendum to revision 1.3 of the datasheet immediately following this cover page.
- Revision 1.3 of the datasheet, following the addendum. The changes described in the addendum have not been implemented in the specified pages.

Freescale Semiconductor, Inc.
Datasheet Addendum

Document Number: MC13201AD
Rev. 0, 04/2015

Addendum to Rev. 1.3 of the MC13201 Datasheet

This addendum identifies changes to Rev. 1.3 of the MC13201 datasheet. The changes described in this addendum have not been implemented in the specified pages.

1 Case outline drawing change for new QFN-32 package migration

Location:	Section 9, Page 27

The case outline was changed because of migration from gold wireto copper wire for QFN-32 packages.

The case outline details in Section 9 Packaging Information, should be replaced with package document #98ASA00473D case outline details.

To view the new case outline details, go to freescale.com and perform a keyword search for the drawing's document number.

If you want the drawing for this package	Then use this document number
QFN-32	98ASA00473D

NOTE

For more information about QFN package use, see EB806 Electrical Connection Recommendations for Exposed Pad on QFN and DFN Packages.

2 References to case 1311-03

Location:	Section 1, Page 1 Section 9, Page 27

Remove the references to case 1311-03.

Freescale Semiconductor
Technical Data

Document Number: MC13201
Rev. 1.3, 04/2008

MC13201

Package Information
Plastic Package
Case 1311-03
QFN -32

Ordering Information

Device	Device Marking	Package
MC13201FC	13201	QFN-32
MC13201FCR2 (Tape and Reel)	13201	QFN-32

MC13201

2.4 GHz Low Power Transceiver for the IEEE® 802.15.4 Standard

1 Introduction

The MC13201 is a short range, low power, 2.4 GHz Industrial, Scientific, and Medical (ISM) band transceivers. The MC13201 contains a complete packet data modem which is compliant with the IEEE® 802.15.4 Standard PHY (Physical) layer. This allows the development of proprietary point-to-point and star networks based on the 802.15.4 packet structure and modulation format. For full 802.15.4 Standard compliance, the MC13202 and Freescale's 802.15.4 MAC software are required.

When combined with an appropriate microcontroller (MCU), the MC13201 provides a cost-effective solution for short-range data links and networks. Interface with the MCU is accomplished using a four wire serial peripheral interface (SPI) connection and an interrupt request output which allows for the use of a variety of processors. The software and processor can be scaled to fit applications ranging from simple point-to-point systems to star networks.

Contents

For more detailed information about MC13201 operation, refer to the *MC13201 Reference Manual*, (MC13201RM).

Applications include, but are not limited to, the following:

- Residential and commercial automation
  - Lighting control
  - Security
  - Access control
  - Heating, ventilation, air-conditioning (HVAC)
  - Automated meter reading (AMR)
- Industrial Control
  - Asset tracking and monitoring
  - Homeland security
  - Process management
  - Environmental monitoring and control
  - HVAC
  - Automated meter reading
- Health Care
  - Patient monitoring
  - Fitness monitoring
- Consumer
  - Human interface devices (keyboard, mice, etc.)
  - Remote control
  - Wireless toys

The transceiver includes a low noise amplifier, 1.0 mW power amplifiers (PA), onboard RF transmit/receive (T/R) switch for single port use, PLL with internal voltage controlled oscillator (VCO), on-board power supply regulation, and full spread-spectrum encoding and decoding. The device supports 250 kbps Offset-Quadrature Phase Shift Keying (O-QPSK) data in 2.0 MHz channels with 5.0 MHz channel spacing per the 802.15.4 Standard. The SPI port and interrupt request output are used for receive (RX) and transmit (TX) data transfer and control.

2 Features

- Recommended power supply range: 2.0 to 3.4 V
- Fully compliant 802.15.4 Standard transceiver supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode
- Operates on one of 16 selectable channels in the 2.4 GHz band
- -1 to 0 dBm nominal output power, programmable from -27 dBm to +3 dBm typical
- Receive sensitivity of <-91 dBm (typical) at 1% PER, 20-byte packet, much better than the 802.15.4 Standard of -85 dBm

- Integrated transmit/receive switch
- Dual PA output pairs which can be programmed for full differential single port or dual port operation that supports an external LNA and/or PA
- Three power down modes for increased battery life
  - < 1 µA Off current
  - 1.0 µA Typical Hibernate current
  - 35 µA Typical Doze current (no CLKO)
- Programmable frequency clock output (CLKO) for use by MCU
- Onboard trim capability for 16 MHz crystal reference oscillator eliminates need for external variable capacitors and allows for automated production frequency calibration
- Four internal timer comparators available to supplement MCU timer resources
- Buffered transmit and receive data packets for simplified use with low cost MCUs
- Seven GPIO to supplement MCU GPIO
- Operating temperature range: -40 °C to 85 °C
- Small form factor QFN-32 Package
  - Meets moisture sensitivity level (MSL) 3
  - 260 °C peak reflow temperature
  - Meets lead-free requirements

2.1 Software Support

Freescale provides a software suite to complement the MC13201 hardware which is called the Freescale Simple MAC (SMAC):

- Simple proprietary wireless connectivity.
- Small memory footprint (about 3 Kbytes typical)
- Supports point-to-point and star network configurations
- Proprietary networks
- Source code and application examples provided

3 Block Diagrams

Figure 1 shows a simplified block diagram of the MC13201 which is an 802.15.4 Standard compatible transceiver that provides the functions required in the physical layer (PHY) specification.

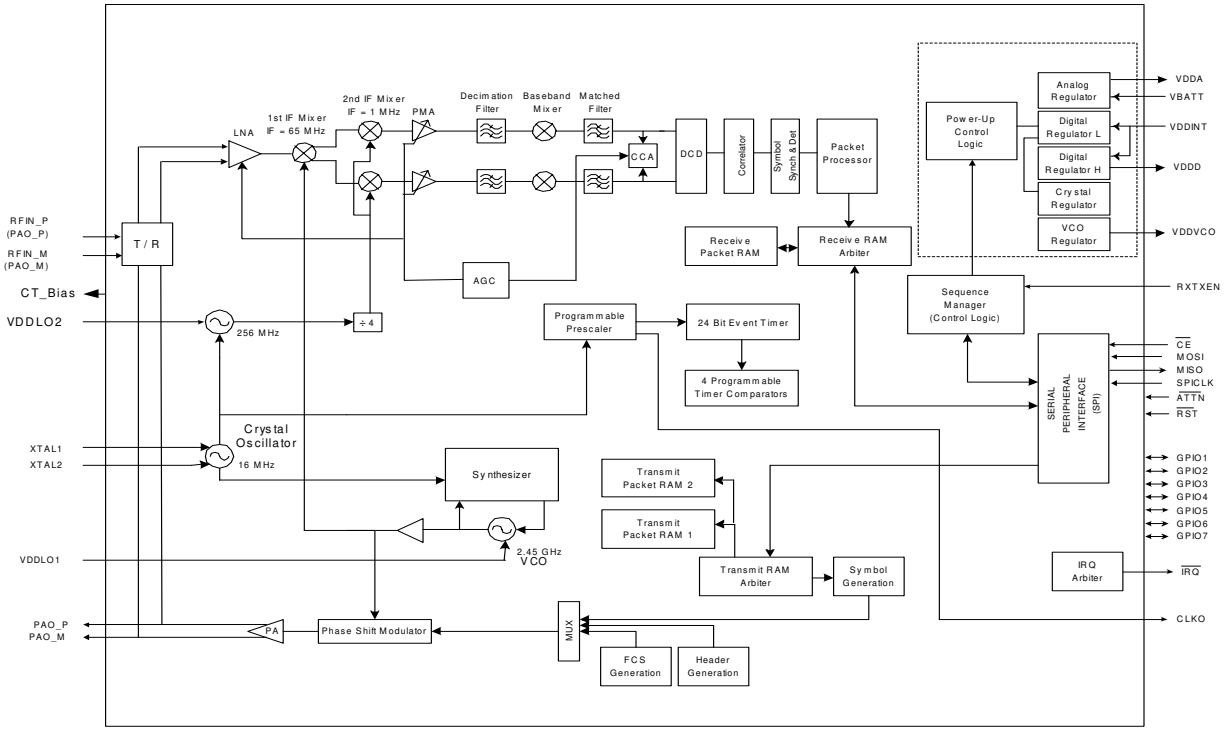


Figure 1. 802.15.4 modem Simplified Block Diagram

Figure 2 shows the basic system block diagram for the MC13201 in an application. Interface with the transceiver is accomplished through a 4-wire SPI port and interrupt request line. The media access control (MAC), drivers, and network and application software (as required) reside on the host processor. The host can vary from a simple 8-bit device up to a sophisticated 32-bit processor depending on application requirements.

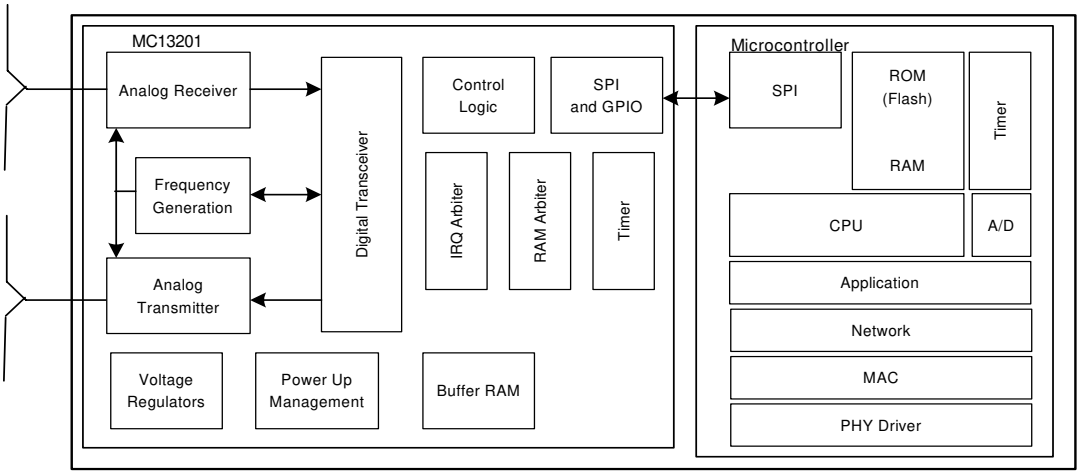


Figure 2. System Level Block Diagram

4 Data Transfer Mode

The MC13201 has a data transfer mode called Packet Mode where data is buffered in on-chip Packet RAMs. There is a TX Packet RAM and an RX Packet RAM, each of which are 64 locations by 16 bits wide.

4.1 Packet Structure

Figure 3 shows the packet structure of the MC13201 which is consistent with the 802.15.4 Standard. Payloads of up to 125 bytes are supported. The MC13201 adds a four-byte preamble, a one-byte Start of Frame Delimiter (SFD), and a one-byte Frame Length Indicator (FLI) before the data. A Frame Check Sequence (FCS) is calculated and appended to the end of the data.

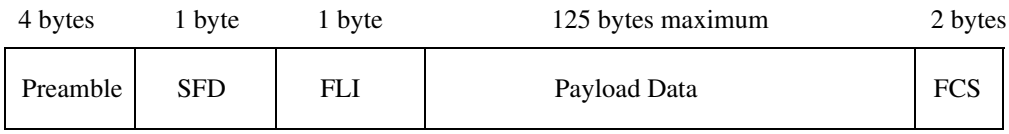


Figure 3. MC13201 Packet Structure

4.2 Receive Path Description

In the receive signal path, the RF input is converted to low IF In-phase and Quadrature (I & Q) signals through two down-conversion stages. A Clear Channel Assessment (CCA) can be performed based upon the baseband energy integrated over a specific time interval. The digital backend performs Differential Chip Detection (DCD), the correlator “de-spreads” the Direct Sequence Spread Spectrum (DSSS) Offset QPSK (O-QPSK) signal, determines the symbols and packets, and detects the data.

The preamble, SFD, and FLI are parsed and used to detect the payload data and FCS which are stored in RAM. A two-byte FCS is calculated on the received data and compared to the FCS value appended to the transmitted data, which generates a Cyclical Redundancy Check (CRC) result. Link Quality is measured over a 64 µs period after the packet preamble and stored in RAM.

The MC13201 uses a packet mode where the data is processed as an entire packet and stored in Rx Packet RAM. The MCU is notified that an entire packet has been received via an interrupt.

Figure 4 shows CCA reported power level versus input power. Note that CCA reported power saturates at about -57 dBm input power which is well above 802.15.4 Standard requirements. Figure 5 shows energy detection/LQI reported level versus input power.

NOTE

For both graphs, the required 802.15.4 Standard accuracy and range limits are shown. A 3.5 dBm offset has been programmed into the CCA reporting level to center the level over temperature in the graphs.

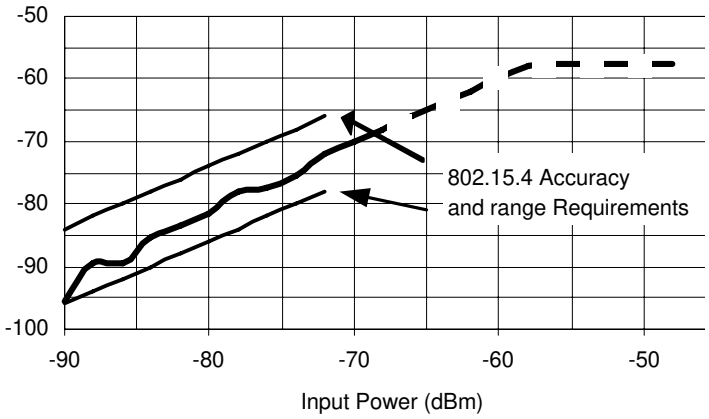


Figure 4. Reported Power Level versus Input Power in CCA Mode

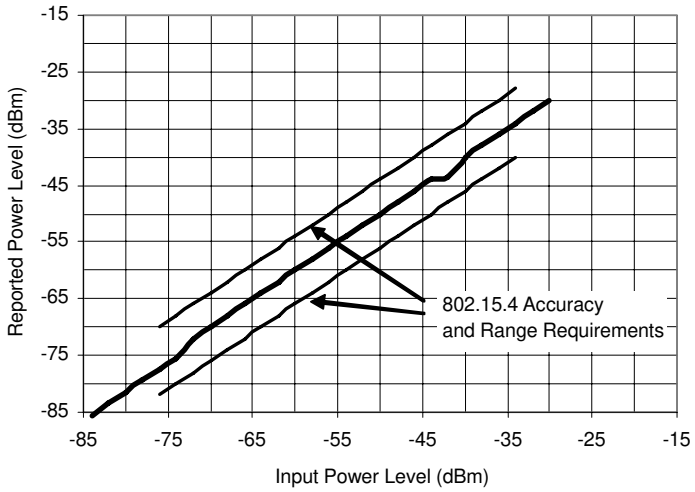


Figure 5. Reported Power Level Versus Input Power for Energy Detect or Link Quality Indicator

4.3 Transmit Path Description

For the transmit path, the TX data that was previously stored in TX Packet RAM is retrieved, formed into packets per the 802.15.4 PHY, spread, and then up-converted to the transmit frequency.

Because the MC13201 is used in packet mode, data is processed as an entire packet. The data is first loaded into the TX buffer. The MCU then requests that the MC13201 transmit the data. The MCU is notified via an interrupt when the whole packet has successfully been transmitted.

5 Electrical Characteristics

5.1 Maximum Ratings

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{BATT}, V_{DDINT}	-0.3 to 3.6	Vdc
Digital Input Voltage	Vin	-0.3 to (V_{DDINT} + 0.3)	
RF Input Power	P_{max}	10	dBm
Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	-55 to 125	°C

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

Note: Meets Human Body Model (HBM) = 2 kV. RF input/output pins have no ESD protection.

5.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BATT} = V_{DDINT})[1]	V_{BATT}, V_{DDINT}	2.0	2.7	3.4	Vdc
Input Frequency	f_{in}	2.405	-	2.480	GHz
Ambient Temperature Range	T_A	-40	25	85	°C
Logic Input Voltage Low	V_{IL}	0	-	30% V_{DDINT}	V
Logic Input Voltage High	V_{IH}	70% V_{DDINT}	-	V_{DDINT}	V
SPI Clock Rate	f_{SPI}	-	-	8.0	MHz
RF Input Power	P_{max}	-	-	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	f_{ref}	16 MHz Only			

[1] If the supply voltage is produced by a switching DC-DC converter, ripple should be less than 100 mV peak-to-peak.

5.3 DC Electrical Characteristics

Table 3. DC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_{BATT} + V_{DDINT}) Off[1] Hibernate[1] Doze (No CLKO)[1] [2] Idle Transmit Mode (0 dBm nominal output power) Receive Mode	 $I_{leakage}$ I_{CCH} I_{CCD} I_{CCI} I_{CCT} I_{CCR}	 - - - - - -	 0.2 1.0 35 500 30 37	 2.5 22 154 1500 38 45	 µA µA µA µA mA mA
Input Current (V_{IN} = 0 V or V_{DDINT}) (All digital inputs)	I_{IN}	-	-	±1	µA
Input Low Voltage (All digital inputs)	V_{IL}	0	-	30% V_{DDINT}	V
Input High Voltage (all digital inputs)	V_{IH}	70% V_{DDINT}	-	V_{DDINT}	V
Output High Voltage (I_{OH} = -1 mA) (All digital outputs)	V_{OH}	80% V_{DDINT}	-	V_{DDINT}	V
Output Low Voltage (I_{OL} = 1 mA) (All digital outputs)	V_{OL}	0	-	20% V_{DDINT}	V

1 To attain specified low power current, all GPIO and other digital IO must be handled properly. See Section 8.3, “Low Power Considerations.

2 CLKO frequency at default value of 32.786 kHz.

5.4 AC Electrical Characteristics

Table 4. Receiver AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% Packet Error Rate (PER) (-40 to +85 °C)	$SENS_{per}$	-	-91	-	dBm
Sensitivity for 1% Packet Error Rate (PER) (+25 °C)		-	-91	-82	dBm
Saturation (maximum input level)	$SENS_{max}$	-	10	-	dBm
Channel Rejection for 1% PER (desired signal -82 dBm) +5 MHz (adjacent channel) -5 MHz (adjacent channel) +10 MHz (alternate channel) -10 MHz (alternate channel) >= 15 MHz		 - - - - -	 31 30 43 41 53	 - - - - -	 dB dB dB dB dB
Frequency Error Tolerance		-	-	200	kHz
Symbol Rate Error Tolerance		-	-	80	ppm

Table 5. Transmitter AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Spectral Density (-40 to +85 °C) Absolute limit		-	-47	-	dBm
Power Spectral Density (-40 to +85 °C) Relative limit		-	47	-	
Nominal Output Power[1]	P_{out}	-5	-1	-	dBm
Maximum Output Power[2]			4		dBm
Error Vector Magnitude	EVM	-	20	45	%
Output Power Control Range		-	30	-	dB
Over the Air Data Rate		-	250	-	kbps
2nd Harmonic		-	TBD	-	dBc
3rd Harmonic		-	TBD	-	dBc

1 SPI Register 12 programmed to 0x00BC which sets output power to nominal (-1 dBm typical).

2 SPI Register 12 programmed to 0x00FF which sets output power to maximum.

Table 6. Digital Timing Specifications

(VBATT, VDDINT = 2.7 V, TA = 25 °C, frequency = 16 MHz, unless otherwise noted.
SPI timing parameters are referenced to Figure 8.

Symbol	Parameter	Min	Typ	Max	Unit
T0	SPICLK period	125			nS
T1	Pulse width, SPICLK low	50			nS
T2	Pulse width, SPICLK high	50			nS
T3	Delay time, MISO data valid from falling SPICLK		15		nS
T4	Setup time, $\overline{CE}$ low to rising SPICLK		15		nS
T5	Delay time, MISO valid from $\overline{CE}$ low		15		nS
T6	Setup time, MOSI valid to rising SPICLK		15		nS
T7	Hold time, MOSI valid from rising SPICLK		15		nS
	$\overline{RST}$ minimum pulse width low (asserted)	250			nS

Figure 6 shows a typical AC parameter evaluation circuit.

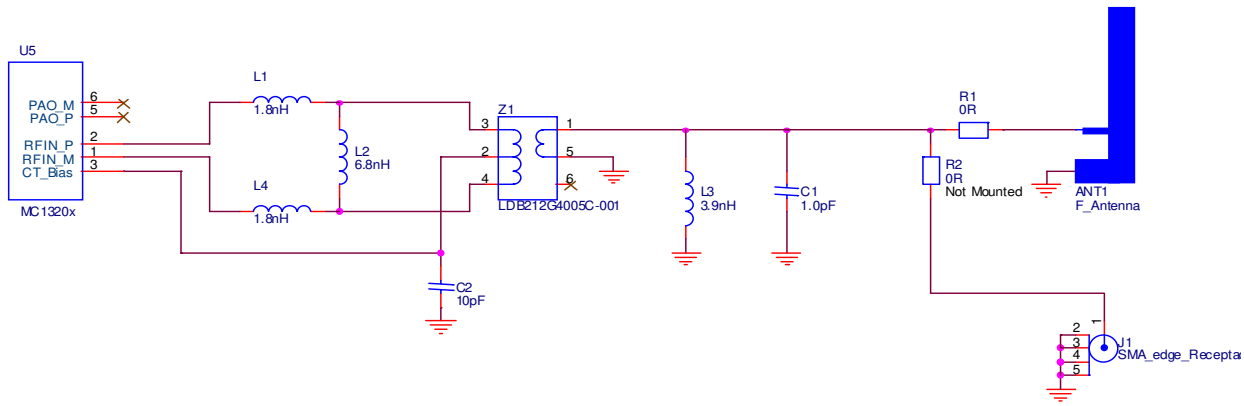


Figure 6. RF Parametric Evaluation Circuit

6 Functional Description

The following sections provide a detailed description of the MC13201 functionality, including operating modes, and the Serial Peripheral Interface (SPI).

6.1 MC13201 Operational Modes

The MC13201 has a number of operational modes that allow for low-current operation. Transition from the Off to Idle mode occurs when $\overline{RST}$ is negated. Once in Idle, the SPI is active and is used to control the IC. Transition to Hibernate and Doze modes is enabled via the SPI. These modes are summarized, along with the transition times, in Table 7. Current drain in the various modes is listed in Table 3, DC Electrical Characteristics.

Table 7. MC13201 Mode Definitions and Transition Times

Mode	Definition	Transition Time To or From Idle
Off	All IC functions Off, Leakage only. $\overline{RST}$ asserted. Digital outputs are tri-stated including $\overline{IRQ}$	10 - 25 ms to Idle
Hibernate	Crystal Reference Oscillator Off. (SPI not functional.) IC Responds to $\overline{ATTN}$. Data is retained.	7 - 20 ms to Idle
Doze	Crystal Reference Oscillator On but CLKO output available only if Register 7, Bit 9 = 1 for frequencies of 1 MHz or less. (SPI not functional.) Responds to $\overline{ATTN}$ and can be programmed to enter Idle Mode through an internal timer comparator.	(300 + 1/CLKO) µs to Idle
Idle	Crystal Reference Oscillator On with CLKO output available. SPI active.	
Receive	Crystal Reference Oscillator On. Receiver On.	144 µs from Idle
Transmit	Crystal Reference Oscillator On. Transmitter On.	144 µs from Idle

6.2 Serial Peripheral Interface (SPI)

The host microcontroller directs the MC13201, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the MC13201 occurs as multiple 8-bit bursts on the SPI. The SPI signals are:

1. Chip Enable ($\overline{CE}$) - A transaction on the SPI port is framed by the active low $\overline{CE}$ input signal. A transaction is a minimum of 3 SPI bursts and can extend to a greater number of bursts.
2. SPI Clock (SPICLK) - The host drives the SPICLK input to the MC13201. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

NOTE

For Freescale microcontrollers, the SPI clock format is the clock phase control bit CPHA = 0 and the clock polarity control bit CPOL = 0.

3. Master Out/Slave In (MOSI) - Incoming data from the host is presented on the MOSI input.
4. Master In/Slave Out (MISO) - The MC13201 presents data to the master on the MISO output.

A typical interconnection to a microcontroller is shown in Figure 7.

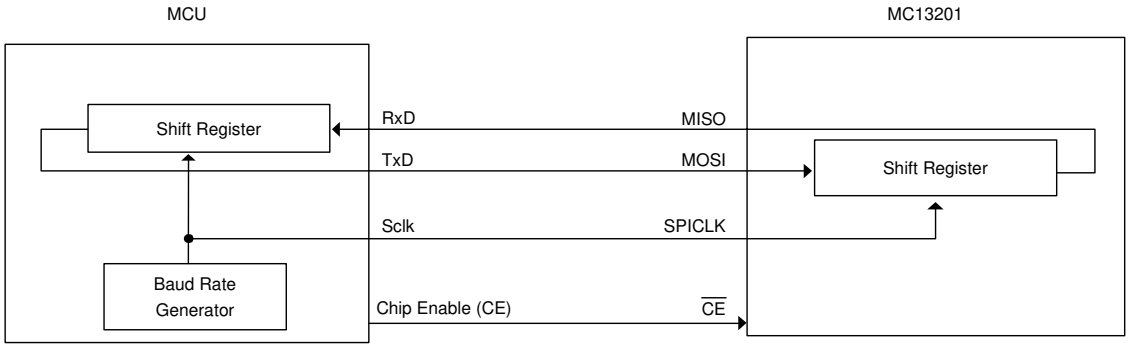


Figure 7. SPI Interface

Although the SPI port is fully static, internal memory, timer and interrupt arbiters require an internal clock (CLK_{core}), derived from the crystal reference oscillator, to communicate from the SPI registers to internal registers and memory.

6.2.1 SPI Burst Operation

The SPI port of an MCU transfers data in bursts of 8 bits with most significant bit (MSB) first. The master (MCU) can send a byte to the slave (transceiver) on the MOSI line and the slave can send a byte to the master on the MISO line. Although an MC13201 transaction is three or more SPI bursts long, the timing of a single SPI burst is shown in Figure 8.

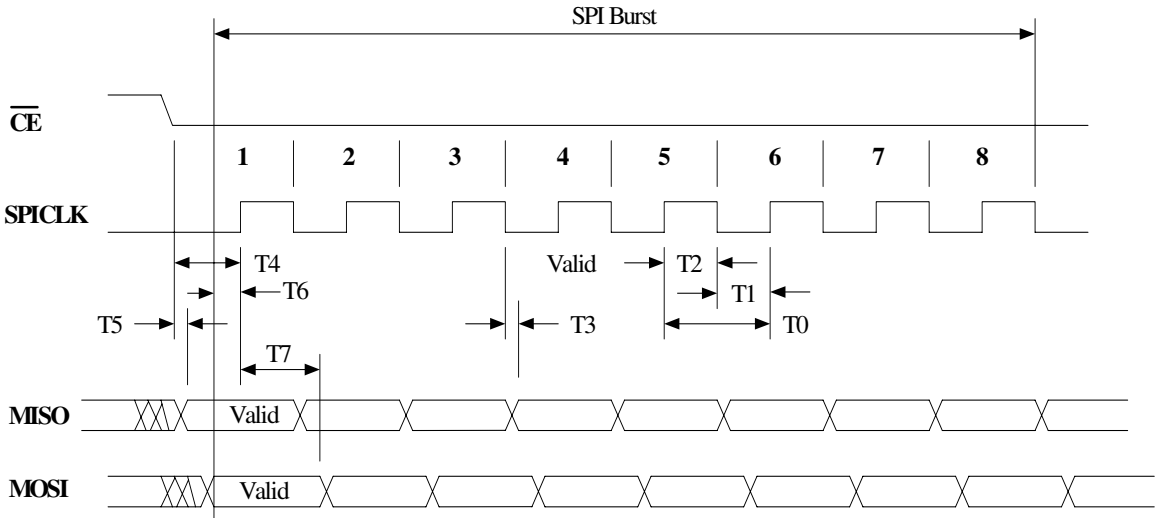


Figure 8. SPI Single Burst Timing Diagram

SPI digital timing specifications are shown in Table 6.

6.2.2 SPI Transaction Operation

Although the SPI port of an MCU transfers data in bursts of 8 bits, the MC13201 requires that a complete SPI transaction be framed by $\overline{CE}$, and there will be three (3) or more bursts per transaction. The assertion of $\overline{CE}$ to low signals the start of a transaction. The first SPI burst is a write of an 8-bit header to the transceiver (MOSI is valid) that defines a 6-bit address of the internal resource being accessed and identifies the access as being a read or write operation. In this context, a write is data written to the MC13201 and a read is data written to the SPI master. The following SPI bursts will be either the write data (MOSI is valid) to the transceiver or read data from the transceiver (MISO is valid).

Although the SPI bus is capable of sending data simultaneously between master and slave, the MC13201 never uses this mode. The number of data bytes (payload) will be a minimum of 2 bytes and can extend to a larger number depending on the type of access. The number of payload bytes sent will always be an even integer. After the final SPI burst, $\overline{CE}$ is negated to high to signal the end of the transaction. Refer to the *MC13201 Reference Manual*, (MC13201RM) for more details on SPI registers and transaction types.

An example SPI read transaction with a 2-byte payload is shown in Figure 9.

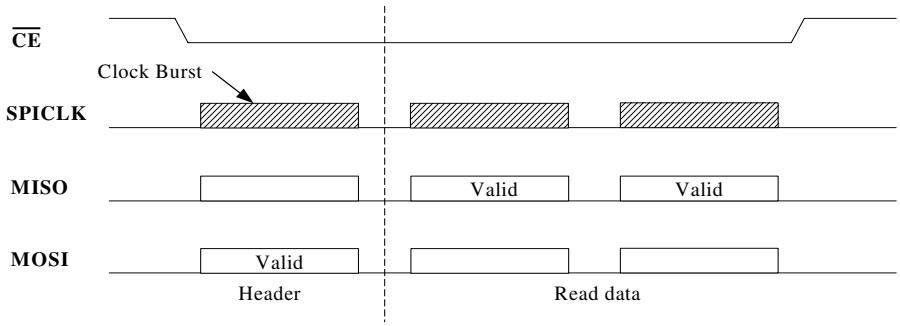


Figure 9. SPI Read Transaction Diagram

7 Pin Connections

Table 8. Pin Function Description

Pin #	Pin Name	Type	Description	Functionality
1	RFIN_M	RF Input	RF input/output negative.	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA
2	RFIN_P	RF Input	RF input/output positive.	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA
3	CT_Bias	Control voltage	Bias voltage/control signal for external RF components	When used with internal T/R switch, provides RX ground reference and TX VDDA reference for use with external balun. Can also be used as a control signal for external LNA, PA, or T/R switch.
4	NC		Tie to Ground.	
5	PAO_P	RF Output /DC Input	RF Power Amplifier Output Positive.	Open drain. Connect to VDDA through a bias network when used with an external balun. Not used when internal T/R switch is used.
6	PAO_M	RF Output/DC Input	RF Power Amplifier Output Negative.	Open drain. Connect to VDDA through a bias network when used with an external balun. Not used when internal T/R switch is used.
7	SM	Input	Test mode pin.	Must be grounded for normal operation.
8	GPIO4[1]	Digital Input/ Output	General Purpose Input/Output 4.	See Footnote 1.
9	GPIO3[1]	Digital Input/ Output	General Purpose Input/Output 3.	See Footnote 1.
10	GPIO2[1]	Digital Input/ Output	General Purpose Input/Output 2. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO2 functions as a “CRC Valid” indicator.	See Footnote 1.
11	GPIO1[1]	Digital Input/ Output	General Purpose Input/Output 1. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO1 functions as an “Out of Idle” indicator.	See Footnote 1.
12	$\overline{\text{RST}}$	Digital Input	Active Low Reset. While held low, the IC is in Off Mode and all internal information is lost from RAM and SPI registers. When high, IC goes to IDLE Mode, with SPI in default state.	

Table 8. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
13	RXTXEN[2]	Digital Input	Active High. Low to high transition initiates RX or TX sequence depending on SPI setting. Should be taken high after SPI programming to start RX or TX sequence and should be held high through the sequence. After sequence is complete, return RXTXEN to low. When held low, forces Idle Mode.	See Footnote 2
14	$\overline{\text{ATTN}}$[2]	Digital Input	Active Low Attention. Transitions IC from either Hibernate or Doze Modes to Idle.	See Footnote 2
15	CLKO	Digital Output	Clock output to host MCU. Programmable frequencies of: 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 62.5 kHz, 32.786+ kHz (default), and 16.393+ kHz.	
16	SPICLK[2]	Digital Clock Input	External clock input for the SPI interface.	See Footnote 2
17	MOSI[2]	Digital Input	Master Out/Slave In. Dedicated SPI data input.	See Footnote 2
18	MISO[3]	Digital Output	Master In/Slave Out. Dedicated SPI data output.	See Footnote 3
19	$\overline{\text{CE}}$[2]	Digital Input	Active Low Chip Enable. Enables SPI transfers.	See Footnote 2
20	$\overline{\text{IRQ}}$	Digital Output	Active Low Interrupt Request.	Open drain device. Programmable 40 kΩ internal pull-up. Interrupt can be serviced every 6 µs with <20 pF load. Optional external pull-up must be >4 kΩ.
21	VDDD	Power Output	Digital regulated supply bypass.	Decouple to ground.
22	VDDINT	Power Input	Digital interface supply & digital regulator input. Connect to Battery.	2.0 to 3.4 V. Decouple to ground.
23	GPIO5[1]	Digital Input/Output	General Purpose Input/Output 5.	See Footnote 1
24	GPIO6[1]	Digital Input/Output	General Purpose Input/Output 6.	See Footnote 1
25	GPIO7[1]	Digital Input/Output	General Purpose Input/Output 7.	See Footnote 1
26	XTAL1	Input	Crystal Reference oscillator input.	Connect to 16 MHz crystal and load capacitor.

Table 8. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
27	XTAL2	Input/Output	Crystal Reference oscillator output **Note:** Do not load this pin by using it as a 16 MHz source. Measure 16 MHz output at Pin 15, CLKO, programmed for 16 MHz. See the *MC13201 Reference Manual* for details.	Connect to 16 MHz crystal and load capacitor.
28	VDDLO2	Power Input	LO2 VDD supply. Connect to VDDA externally.	
29	VDDLO1	Power Input	LO1 VDD supply. Connect to VDDA externally.	
30	VDDVCO	Power Output	VCO regulated supply bypass.	Decouple to ground.
31	VBATT	Power Input	Analog voltage regulators Input. Connect to Battery.	Decouple to ground.
32	VDDA	Power Output	Analog regulated supply Output. Connect to directly VDDLO1 and VDDLO2 externally and to PAO± through a bias network. **Note**: Do not use this pin to supply circuitry external to the chip.	Decouple to ground.
EP	Ground		External paddle / flag ground.	Connect to ground.

1 The transceiver GPIO pins default to inputs at reset. There are no programmable pullups on these pins. Unused GPIO pins should be tied to ground if left as inputs, or if left unconnected, they should be programmed as outputs set to the low state.

2 During low power modes, input must remain driven by MCU.

3 By default MISO is tri-stated when $\overline{CE}$ is negated. For low power operation, miso_hiz_en (Bit 11, Register 07) should be set to zero so that MISO is driven low when $\overline{CE}$ is negated.

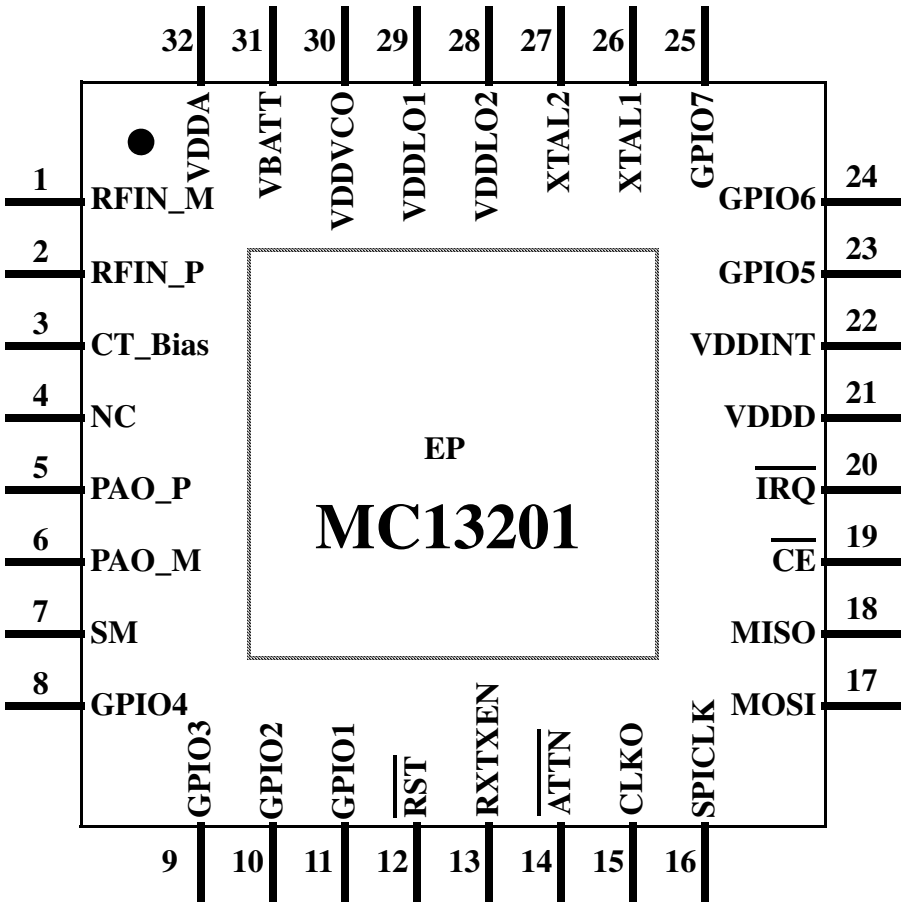


Figure 10. Pin Connections (Top View)

8 Crystal Oscillator Reference Frequency

This section provides application specific information regarding crystal oscillator reference design and recommended crystal usage.

8.1 Crystal Oscillator Design Considerations

The 802.15.4 Standard requires that several frequency tolerances be kept within ± 40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The MC13201 transceiver provides onboard crystal trim capacitors to assist in meeting this performance.

The primary determining factor in meeting this specification is the tolerance of the crystal oscillator reference frequency. A number of factors can contribute to this tolerance and a crystal specification will quantify each of them:

1. The initial (or make) tolerance of the crystal resonant frequency itself.
2. The variation of the crystal resonant frequency with temperature.
3. The variation of the crystal resonant frequency with time, also commonly known as aging.
4. The variation of the crystal resonant frequency with load capacitance, also commonly known as pulling. This is affected by:
   a) The external load capacitor values - initial tolerance and variation with temperature.
   b) The internal trim capacitor values - initial tolerance and variation with temperature.
   c) Stray capacitance on the crystal pin nodes - including stray on-chip capacitance, stray package capacitance and stray board capacitance; and its initial tolerance and variation with temperature.
5. Whether or not a frequency trim step will be performed in production

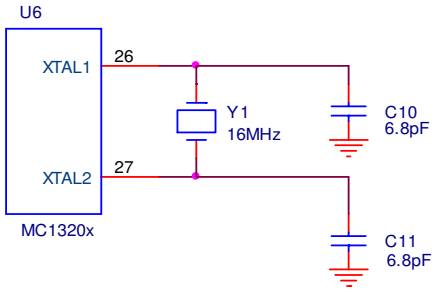
Freescale requires the use of a 16 MHz crystal with a <9 pF load capacitance. The MC13201 does not contain a reference divider, so 16 MHz is the only frequency that can be used. A crystal requiring higher load capacitance is prohibited because a higher load on the amplifier circuit may compromise its performance. The crystal manufacturer defines the load capacitance as that total external capacitance seen across the two terminals of the crystal. The oscillator amplifier configuration used in the MC13201 requires two balanced load capacitors from each terminal of the crystal to ground. As such, the capacitors are seen to be in series by the crystal, so each must be <18 pF for proper loading.

In the Figure 11 crystal reference schematic, the external load capacitors are shown as 6.8 pF each, used in conjunction with a crystal that requires an 8 pF load capacitance. The default internal trim capacitor value (2.4 pF) and stray capacitance total value (6.8 pF) sum up to 9.2 pF giving a total of 16 pF. The value for the stray capacitance was determined empirically assuming the default internal trim capacitor value and for a specific board layout. A different board layout may require a different external load capacitor value. The on-chip trim capability may be used to determine the closest standard value by adjusting the trim value via the SPI and observing the frequency at CLKO. Each internal trim load capacitor has a trim range of approximately 5 pF in 20 fF steps.

Initial tolerance for the internal trim capacitance is approximately ±15%.

Since the MC13201 contains an on-chip reference frequency trim capability, it is possible to trim out virtually all of the initial tolerance factors and put the frequency within 0.12 ppm on a board-by-board basis. Individual trimming of each board in a production environment allows use of the lowest cost crystal, but requires that each board go through a trimming procedure. This step can be avoided by using/specifying a crystal with a tighter stability tolerance, but the crystal will be slightly higher in cost.

A tolerance analysis budget may be created using all the previously stated factors. It is an engineering judgment whether the worst case tolerance will assume that all factors will vary in the same direction or if the various factors can be statistically rationalized using RSS (Root-Sum-Square) analysis. The aging factor is usually specified in ppm/year and the product designer can determine how many years are to be assumed for the product lifetime. Taking all of the factors into account, the product designer can determine the needed specifications for the crystal and external load capacitors to meet the 802.15.4 Standard.



Y1 = Daishinku KDS - DSX321G ZD00882

Figure 11. MC13201 Modem Crystal Circuit

8.2 Crystal Requirements

The suggested crystal specification for the MC13201 is shown in Table 10. A number of the stated parameters are related to desired package, desired temperature range and use of crystal capacitive load trimming. For more design details and suggested crystals, see application note *AN3251, Reference Oscillator Crystal Requirements for MC1319x, MC1320x, and MC1321x.*

Table 9. MC13201 Crystal Specifications[1]

Parameter	Value	Unit	Condition
Frequency	16.000000	MHz	
Frequency tolerance (cut tolerance)[2]	± 10	ppm	at 25 °C
Frequency stability (temperature drift)[3]	± 15	ppm	Over desired temperature range
Aging[4]	± 2	ppm	max
Equivalent series resistance[5]	43	Ω	max
Load capacitance[6]	5 - 9	pF	
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

1 User must be sure manufacturer specifications apply to the desired package.

2 A wider frequency tolerance may acceptable if application uses trimming at production final test.

[3] A wider frequency stability may be acceptable if application uses trimming at production final test.
[4] A wider aging tolerance may be acceptable if application uses trimming at production final test.
[5] Higher ESR may be acceptable with lower load capacitance.
[6] Lower load capacitance can allow higher ESR and is better for low temperature operation in Doze mode.

8.3 Low Power Considerations

- Program and use the modem IO pins properly for low power operation
  - — All unused modem GPIOx signals must be used one of 2 ways:
    - – If the Off mode is to be used as a long term low power mode, unused GPIO should be tied to ground. The default GPIO mode is an input and there will be no conflict.
    - – If only Hibernate and/or Doze modes are used as long term low power modes, the GPIO should programmed as outputs in the low state.
  - — When modem GPIO are used as outputs:
    - – Pullup resistors should be provided (can be provided by the MCU IO pin if tied to the MCU) if the modem Off condition is to be used as a long term low power mode.
    - – During Hibernate and/or Doze modes, the GPIO will retain its programmed output state.
  - — If the modem GPIO is used as an input, the GPIO should be driven by its source during all low power modes or a pullup resistor should be provided.
  - — Digital outputs $\overline{\text{IRQ}}$, MISO, and CLKO:
    - – MISO - is always an output. During Hibernate, Doze, and active modes, the default condition is for the MISO output to go to tristate when $\overline{\text{CE}}$ is de-asserted, and this can cause a problem with the MCU because one of its inputs can float. Program Control_B Register 07, Bit 11, miso_hiz_en = 0 so that MISO is driven low when $\overline{\text{CE}}$ is de-asserted. As a result, MISO will not float when Doze or Hibernate Mode is enabled.
    - – $\overline{\text{IRQ}}$ - is an open drain output (OD) and should always have a pullup resistor (typically provided by the MCU IO). $\overline{\text{IRQ}}$ acts as the interrupt request output.

NOTE

It is good practice to have the $\overline{\text{IRQ}}$ interrupt input to the MCU disabled during the hardware reset to the modem. After releasing the modem hardware reset, the interrupt request input to the MCU can then be enabled to await the $\overline{\text{IRQ}}$ that signifies the modem is ready and in Idle mode; this can prevent a possible extraneous false interrupt request.

    - – CLKO - is always an output. During Hibernate CLKO retains its output state, but does not toggle. During Doze, CLKO may toggle depending on whether it is being used.
- If the MCU is also going to be used in low power modes, be sure that all unused IO are programmed properly for low power operation (typically best case is as outputs in the low state). The MC13201 is commonly used with the Freescale MC9S08GT/GB 8-bit devices. For these MCUs:
  - — Use only STOP2 and STOP3 modes (not STOP1) with these devices where the GPIO states are retained. The MCU must retain control of the MC13201 IO during low power operation.
  - — As stated above all unused GPIO should be programmed as outputs low for lowest power and no floating inputs.

— MC9S08GT devices have IO signals that are not pinned-out on the package. These signals must also be initialized (even though they cannot be used) to prevent floating inputs.

8.4 Transceiver RF Configurations and External Connections

The MC13201 radio has features that allow for a flexible as well as low cost RF interface:

- Programmable output power — 0 dBm nominal output power, programmable from -27 dBm to +4 dBm typical
- <-91 dBm (typical) receive sensitivity — At 1% PER, 20-byte packet (well above 802.15.4 Standard of -85 dBm)
- Optional integrated transmit/receive (T/R) switch for low cost operation — With internal PAs and LNA, the internal T/R switch allows a minimal part count radio interface using only a single balun to interface to a single-ended antenna
- Maximum flexibility — There are full differential RF I/O pins for use with the internal T/R switch. Optionally, these pins become the RF_IN signals and a separate set of full differential PA outputs are also provided. Separate inputs and outputs allow for a variety of RF configurations including external LNA and PA for increased range
- CT_Bias Output — The CT_Bias signal provides a switched bias reference for use with the internal T/R switch, and alternatively can be programmed as an antenna switch signal for use with an external antenna switch
- Onboard trim capability for 16 MHz crystal reference oscillator — The 802.15.4 Standard puts a +/- 40 ppm requirement on the carrier frequency. The onboard trim capability of the modem crystal oscillator eliminates need for external variable capacitors and allows for automated production frequency calibration. Also tighter tolerance can produce greater receive sensitivity

8.5 RF Interface Pins

Figure 12 shows the RF interface pins and the associated analog blocks. Notice that separate PA blocks are associated with RFIN_x and PAO_x signal pairs. The RF interface allows both single port differential operation and dual port differential operation.

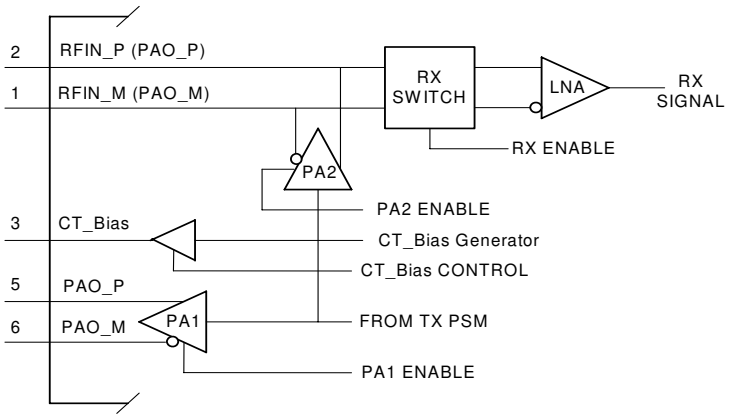


Figure 12. RF Interface Pins

8.5.1 Single Port Operation

The integrated RF switch allows users to operate in a single port configuration. In Single Port Mode, an internal RX switch and separate PA are used and pins RFIN_P (PAO_P) and RFIN_M (PAO_M) become bidirectional and connect both for TX and RX. When receiving, the RX switch is enabled to the internal LNA and the TX PA is disabled. When transmitting, the RX switch is disabled (isolating the LNA) and a TX PA is enabled. The optional CT_Bias pin provides a reference or bias voltage which is at VDDA for transmit and is at ground for receive. This signal can be used to provide the proper bias voltage to a balun that converts a single-ended antenna to the differential interface required by the transceiver.

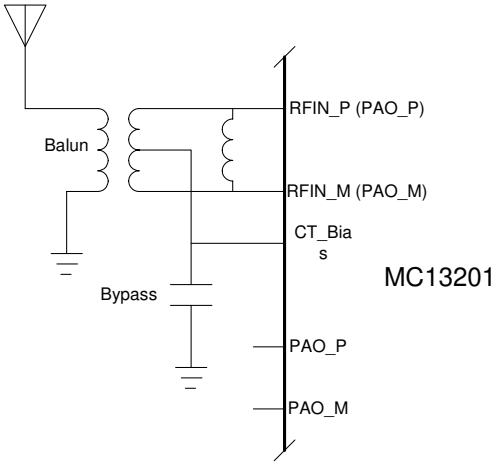


Figure 13. Single Port RF Operation with a Balun

Figure 13 shows a single port example with a balun. The CT_Bias is connected to the balun center-tap providing the proper DC bias voltage to the balun depending on RX or TX.

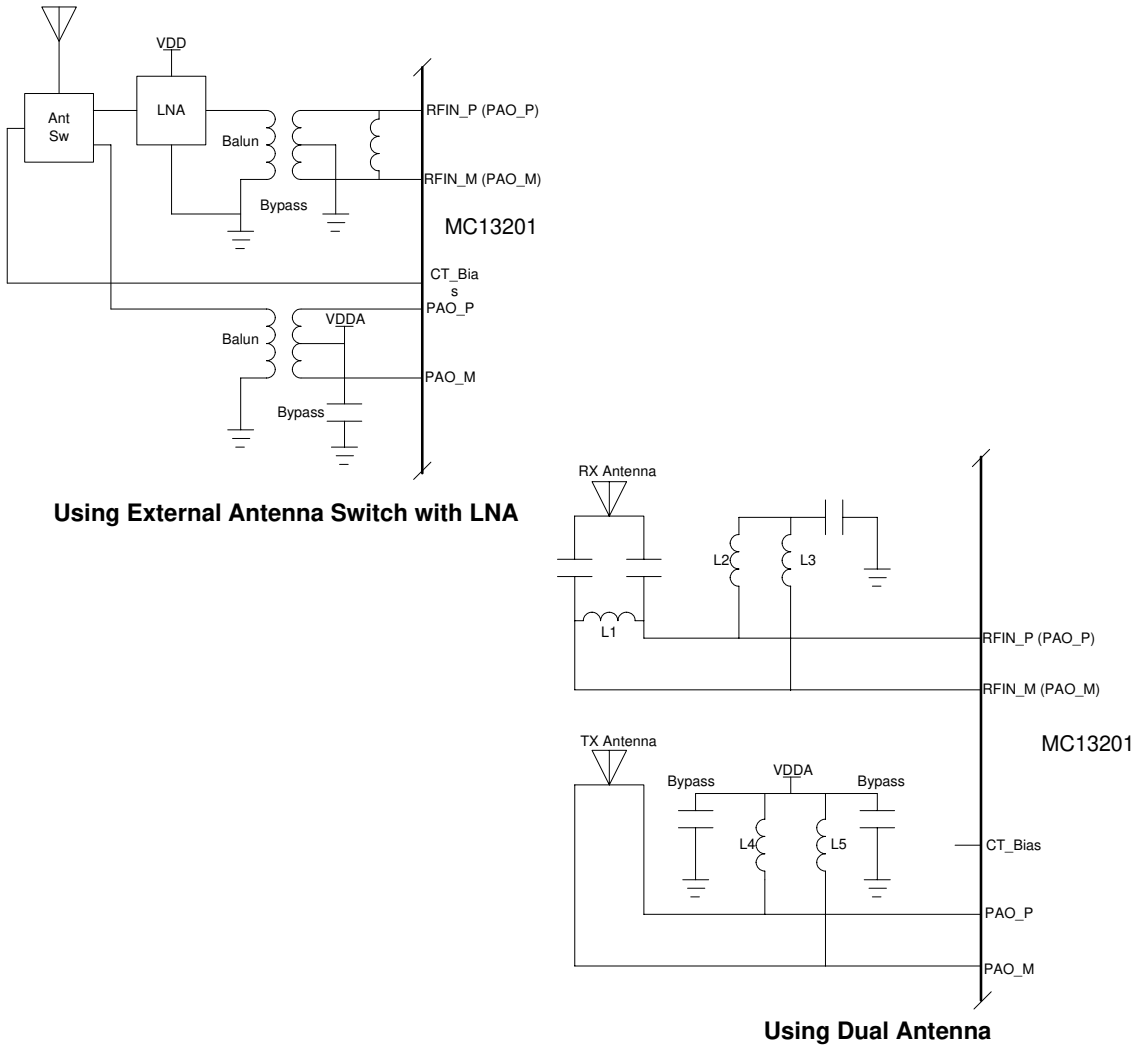
8.5.2 Dual Port Operation

A second set of pins designated PAO_P and PAO_N allow operation in a dual port configuration. There are separate paths for transmit and receive with the optional CT_Bias pin providing a signal that indicates if the radio is in TX or RX Mode which then can be used to drive an external low noise amplifier, power amplifier, or antenna switch.

In dual port operation, the RFIN_P and RFIN_N are inputs only, the internal RX switch to the LNA is enabled to receive, and the associated TX PA stays disabled. Pins PAO_P and PAO_N become the differential output pins and the associated TX PA is enabled for transmit.

Figure 14 shows two dual port configurations. First is a single antenna configuration with an external low noise amplifier (LNA) for greater range. An external antenna switch is used to multiplex the antenna between receive and transmit. An LNA is in the receive path to add gain for greater receive sensitivity. Two external baluns are required to convert the single-ended antenna switch signals to the differential signals required by the radio. Separate RFIN and PAO signals are provided for connection with the baluns, and the CT_bias signal is programmed to provide the external switch control. The polarity of the external switch control is selectable.

Figure 14 also shows a dual antenna configuration where there is a RX antenna and a TX antenna. For the receive side, the RX antenna is ac-coupled to the differential RFIN inputs and these capacitors along with inductor L1 form a matching network. Inductors L2 and L3 are ac-coupled to ground to form a frequency trap. For the transmit side, the TX antenna is connected to the differential PAO outputs, and inductors L4 and L5 provide DC-biasing to VDDA but are ac-isolated. CT_Bias is not required or used.



Using External Antenna Switch with LNA

Using Dual Antenna

Figure 14. Dual Port RF Configuration Examples

8.6 Controlling RF Modes of Operation

Use of the RF interface pins and RF modes of operation are controlled through several bits of modem Control_B Register 07. Figure 15 shows the model for Register 07 with the RF interface control bits highlighted.

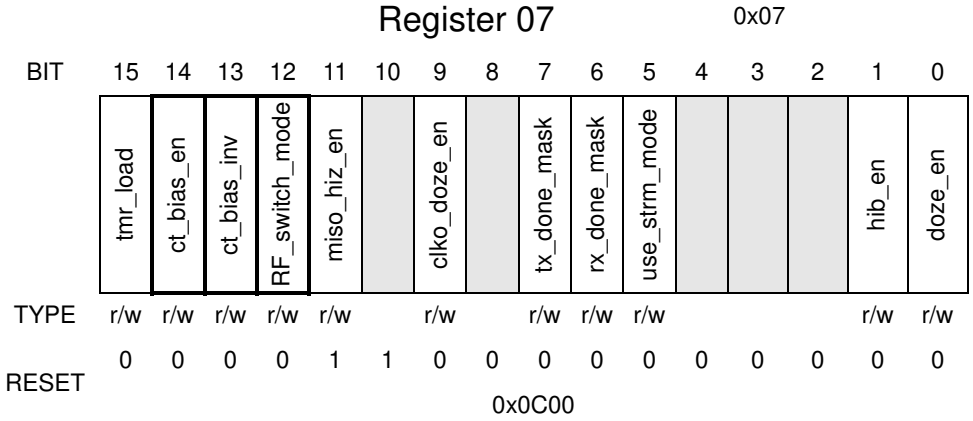


Figure 15. Control_B Register 07 Model

The RF interface control bits include:

- RF_switch_mode (Bit 12) - This bit selects Dual Port Mode versus Single Port Mode:
  - The default condition (Bit 12 = 0) is Dual Port Mode where the RF inputs are RFIN_M and RFIN_P and the RF outputs are PAO_M and PAO_P, and operation is as described in Section 8.5.2, “Dual Port Operation. The use of CT_Bias pin in Dual Port Mode is controlled by Bit 13 and Bit 12.
  - When Bit = 1, the Single Port Mode is selected where RFIN_M (PAO_M) and RFIN_P (PAO_P) become bidirectional pins and operation is as described in Section 8.5.1, “Single Port Operation. The use of CT_Bias pin in Dual Port Mode in controlled by Bit 13 and Bit 12.
- Ct_bias_en (Bit 14) - This bit is the enable for the CT_Bias output. When Bit 14 = 0 (default), the CT_Bias is disabled and stays in a Hi-Z or tri-stated condition. When Bit 14 = 1, the CT_Bias output is active and its state is controlled by the selected mode (Bit 12), ct_bias_inv, and operation of the radio.
- Ct_bias_inv (Bit 13) - This bit only affects the state of CT_Bias when Dual Port Mode is selected and CT_bias is active. The CT_Bias changes state in Dual Port Mode based on the TX or RX state of the radio. The ct_bias_inv bit causes the sense of the active state to change or invert based on Bit 13’s setting. In this manner, the user can select the CT_Bias as a control signal for external components and make the control signal active high or active low.

Table 10 summarizes the operation of the RF interface control bits.

Table 10. RF Interface Control Bits

Bit	Designation	Default	Operation
14	ct_bias_en	0	1 = CT_Bias enabled. Output state is defined by Table 11. 0 = CT_Bias disabled. Output state is tri-stated.
13	ct_bias_inv	0	The output state of CT_Bias under varying conditions is defined in Table 11. This bit only has effect for dual port operation. 1 = CT_Bias inverted. 0 = CT_Bias not inverted
12	RF_switch_mode	0	1= Single Port Mode selected where RF switch is active and RFIN_M and RFIN_P and bidirectional signals. 0 = Dual Port Mode selected where RFIN_M and RFIN_P are inputs only and PAO_P and PAO_N are separate outputs. (This is default operation).

8.7 RF Control Output CT_Bias

CT_Bias is a useful signal for interface with external RF components. It must be enabled via the ct_bias_en control bit, and then its state is determined first by the selected RF mode and then by the active state of the radio, i.e., whether a TX or RX operation is active:

- Single Port Operation - In this mode, the CT_Bias can be used to establish the proper DC bias voltage to a balun depending on the RX state versus TX state as described in Section 8.5.1, “Single Port Operation. Note that in single port operation, the ct_bias_inv has no effect and CT_Bias is at VDDA for TX and is at ground for RX.
- Dual Port Operation - In this mode, the CT_Bias can be used as a control signal to enable a LNA or PA or to determine the direction of an antenna switch as described in Section 8.5.2, “Dual Port Operation. In dual port operation, ct-bias_inv is used to control the sense of the output control, i.e., CT_Bias can be active high or active low for TX and vice-versa for RX.

Table 11 defines the CT_Bias output state depending on control bits and operation mode of the modem. Note that the output state is also defined in Idle, Hibernate, and Doze state as well as RX and TX operation.

Table 11. CT_Bias Output vs. Register Settings

Mode	CT_Bias_en	RF_switch_mode	CT_Bias_inv	CT_Bias
RX	1	1	0	0
RX	1	1	1	0
RX	1	0	0	0
RX	0	X	X	Hi-Z
RX	1	1	0	1
TX	1	1	0	1
TX	1	1	1	1
TX	1	0	0	1

Table 11. CT_Bias Output vs. Register Settings (continued)

Mode	CT_Bias_en	RF_switch_mode	CT_Bias_inv	CT_Bias
TX	1	0	1	0
TX	0	X	X	Hi-Z
Idle	1	X	X	0
Idle	0	X	X	Hi-Z
Doze	1	X	X	0
Doze	0	X	X	Hi-Z
Hibernate	1	X	X	0 (Low-Z)
Hibernate	0	X	X	Hi-Z
Off	X	X	X	Unknown

8.8 RF Single Port Application with an F Antenna

Figure 16 shows a typical single port RF application in which part count is minimized and a printed copper F antenna is used for low cost. Only the RFIN port of the MC13201 is required because the differential port is bi-directional and uses the on-chip T/R switch. Matching to near 50 Ohms is accomplished with L1, L2, L3, and the traces on the PCB. A balun transforms the differential signal to single-ended to interface with the F antenna.

The proper DC bias to the RFIN_x (PAO_x) pins is provided through the balun. The CT_Bias pin provides the proper bias voltage point to the balun depending on operation, that is, CT_Bias is at VDDA voltage for transmit and is at ground for receive. CT_Bias is switched between these two voltages based on the operation. Capacitor C2 provides some high frequency bypass to the DC bias point. The L3/C1 network provides a simple bandpass filter to limit out-of-band harmonics from the transmitter.

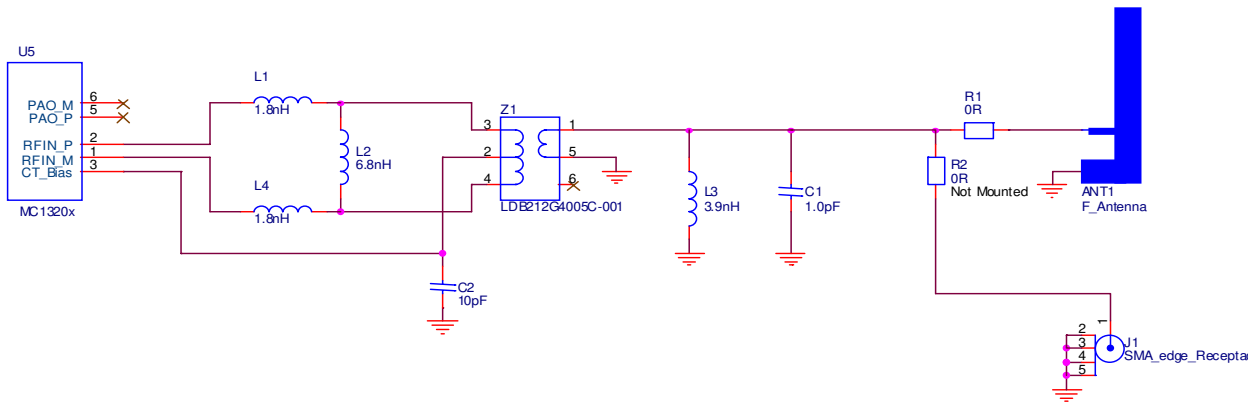


Figure 16. RF Single Port Application with an F-Antenna

9 Packaging Information

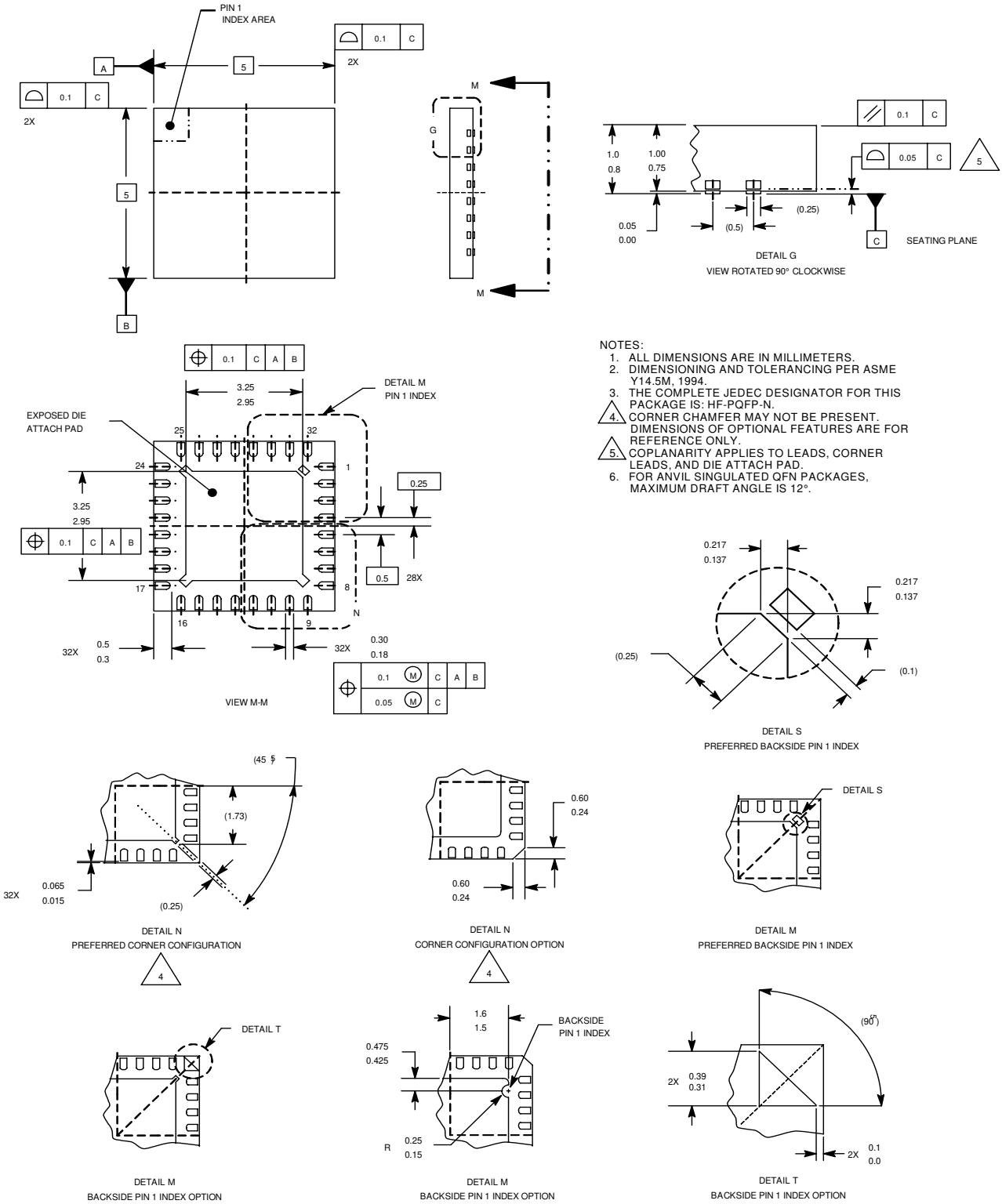


Figure 17. Outline Dimensions for QFN-32, 5x5 mm (Case 1311-03, Issue E)

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Document Number: MC13201
Rev. 1.3,
04/2008