Graphic Display Module

Part Number

G12832A-UW-DW63

Overview

Custom UWVD LCD with FPC: 128x32 (30x11.5), Transmissive (negative), Bottom Viewing Angle (6:00), 1/33 Duty, 1/7 Bias, 3.3V LCD, 3.0V White LED Backlight, Operating Temp: -20C to +70C, Storage Temp: -30C to +80C, 105mm FPC, COG Controller: ST7539I
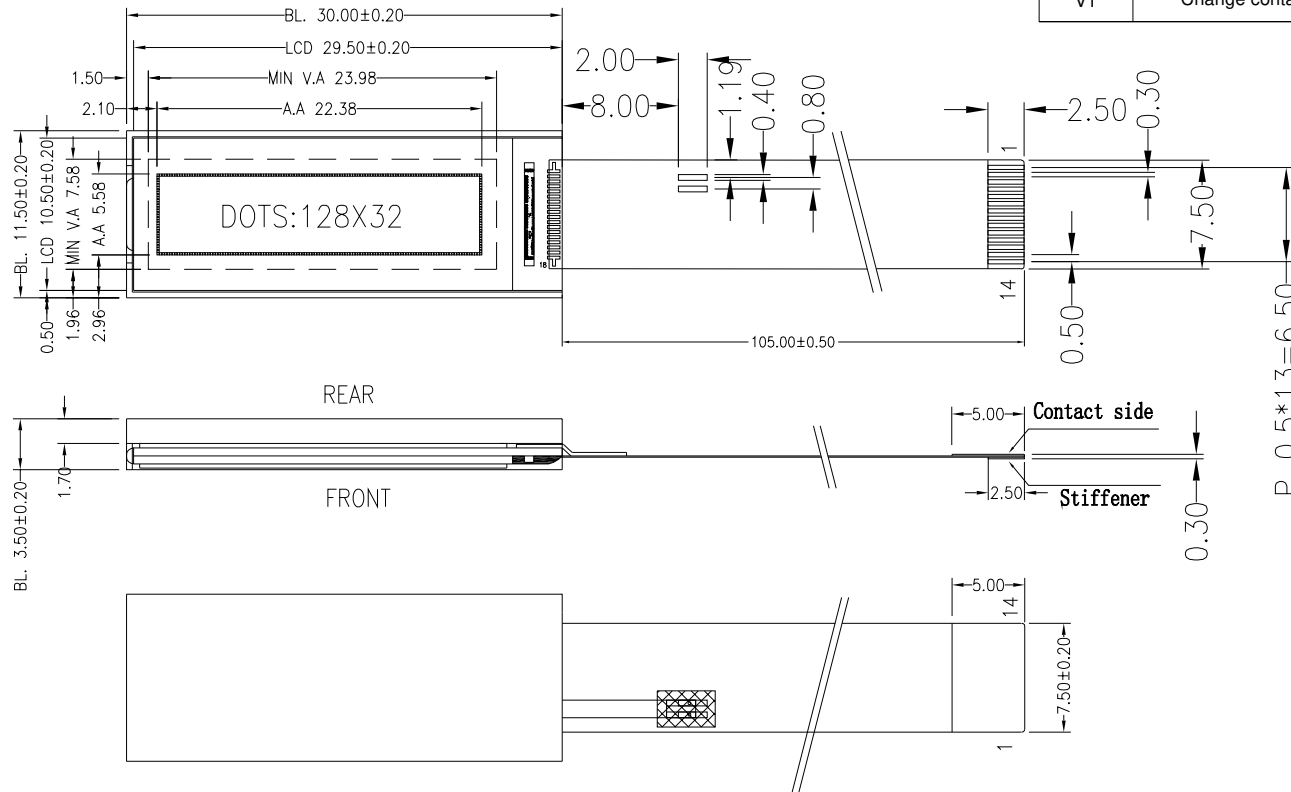
1. Features

Item	Contents	Unit
LCD type	VATN, Negative, Transmissive	---
LCD duty	1/33	---
LCD bias	1/7	---
VDD	3.3	V
Vop	9.0	V
Viewing direction	6:00	o'clock
Module size (W×H×T)	30.0×11.5×3.5	mm
Viewing area	23.98x7.58	mm
Active area	22.38x5.58	mm
Number of dots(W×H)	128x32	dots
LCD type	COG	
IC	ST7539I	
Backlight type	LED/White/3.0V/15mA	

REV.	DESCRIPTION	REVISER	DATE
V0	First issue	YD	2019.10.22
V1	Change contact type of the FPC	YD	2019.11.04

DOTS:128X32

REAR

FRONT

Contact side

Stiffener

DISPLAY TYPE: **UWVD**, NEGATIVE
POLARIZER: TRANSMISSIVE
VIEWING DIRECTION: 6 O'CLOCK
DRIVE METHOD: 1/33DUTY,1/7BIAS
LCM OPERATING VOLTAGE: 3.3V
OPERATING TEMP: -20 TO 70 Deg.C
STORAGE TEMP: -30 TO 80 Deg.C
CONNECTOR: COG ST7539I
UNSIGNED TOLERANCE: ±0.20
RoHS

BLA

BLK

WHITE color   3.0V/15mA

PIN	SYMBOL
1	VG
2	XV0
3	V0
4	VSS
5	VDD
6	BM2
7	BM0
8	SDA
9	SCL
10	A0
11	RST
12	CS0
13	A
14	K
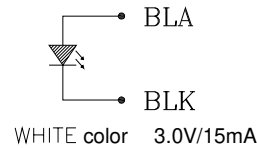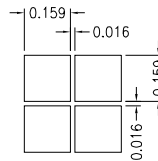
FOCUS LCDs
LCDs MADE SIMPLE®

	NAME:	DATE:	MODEL NUMBER :		SHEET:	1 OF 1
DESIGN BY:		2019.11.4	G12832A-UW-DW63			
CHECKED BY:		2019.11.4			NAME:	LCM
APPROVED BY:			DEFAULT UNITS: mm	PROJECTION		

3. Electrical characteristics

Item	Symbol	Min.	Type	Max.	Unit	Humidity
Operating Voltage	V_{DD}	-0.3		3.6	Volt	
Supply Voltage	VEE	-0.3		13.5	Volt	
Power Supply for LCD	VLCD	-0.3		13.5	Volt	
Input Voltage	Vin	V_{SS}-0.3		V_{DD}+0.3	Volt	
Operating Temperature	Top	-20		+70	℃	
Storage Temperature	Tst	-30		+80	℃	

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}			3.3		Volt
Input Voltage	V_{IH}	H level	$0.8V_{DD}$		V_{DD}	Volt
	V_{IL}	L level	V_{SS}		$0.2V_{DD}$	Volt
LCD Module Driving Voltage	VLCD	Ta=25℃	8.8	9.0	9.2	Volt
Power Supply Current for LCM	I_{DD}	V_{DD}=3.0V		TBD	TBD	mA

4. LED backlight

WHITE color   3.0V,15mA
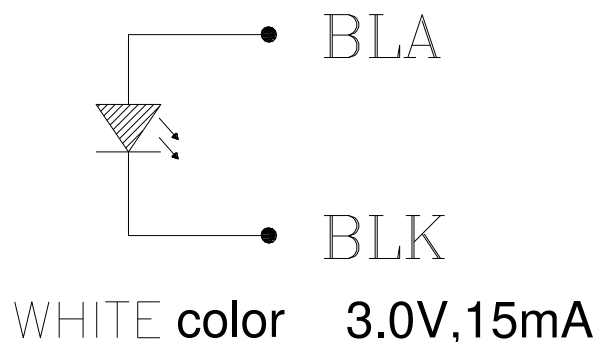
5. Timing characteristics

4-Line Serial interface

ST7539 is active when CS0 is "L" and CS1 is "H", serial data (SDA) and serial clock (SCL) inputs are enabled. When CS0 and CS1 are "H", ST7539 is not active, and the internal 8-bit shift register and 3-bit counter are reset. Some specified information (status byte) can be read out in this mode. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCL). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.
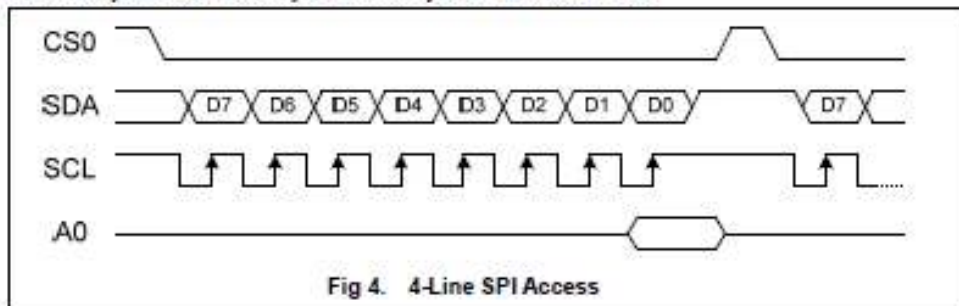
Fig 4.   4-Line SPI Access

I²C Interface

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.
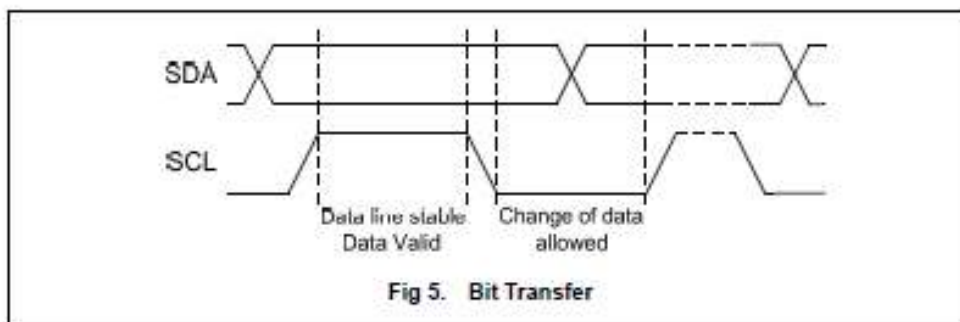
Fig 5.   Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.

Fig 6. Definition of STRAT and STOP Condition
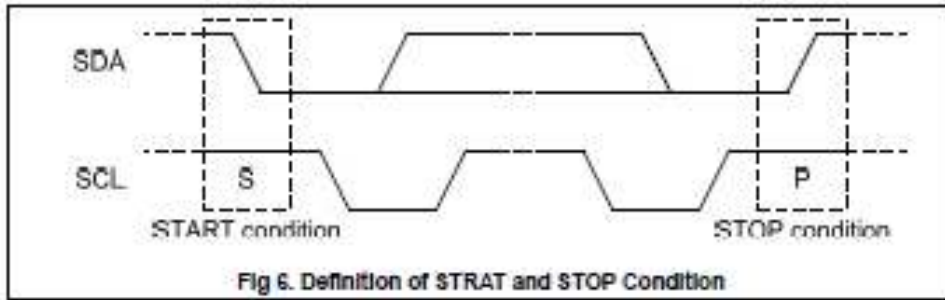
SYSTEM CONFIGURATION

The system configuration is illustrated in Fig 7. and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.

- Receiver: the device which receives the data from the bus.

- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.

- Slave: the device which is addressed by a master.

- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

- Synchronization: procedure to synchronize the clock signals of two or more devices.

Fig 7. System Configuration
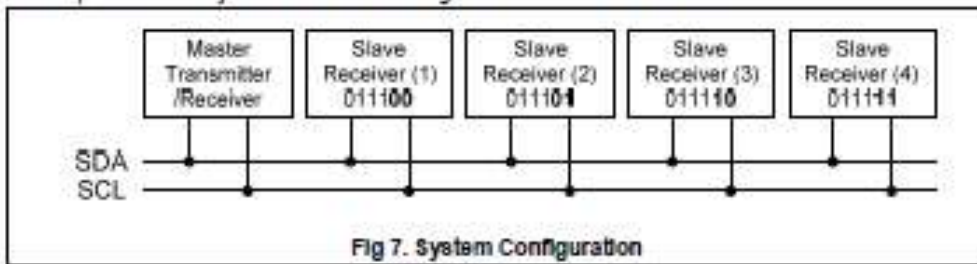
ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated in Fig 8.

Fig 8. Acknowledgement of I²C Interface
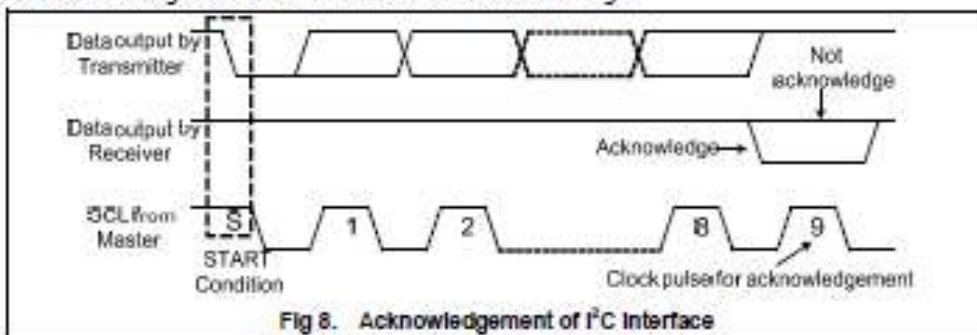
I²C INTERFACE PROTOCOL

ST7539 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 6-bit slave addresses (011100, 011101, 011110 and 011111) and A0 (0111000 or 0111001) are reserved for ST7539. The bit 2 and bit 1 are slave address that set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1). The I²C Interface protocol is illustrated in Fig 9.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address and A0. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

The slave address and control byte is tagged with a cleared most significant bit. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7539 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7539 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.
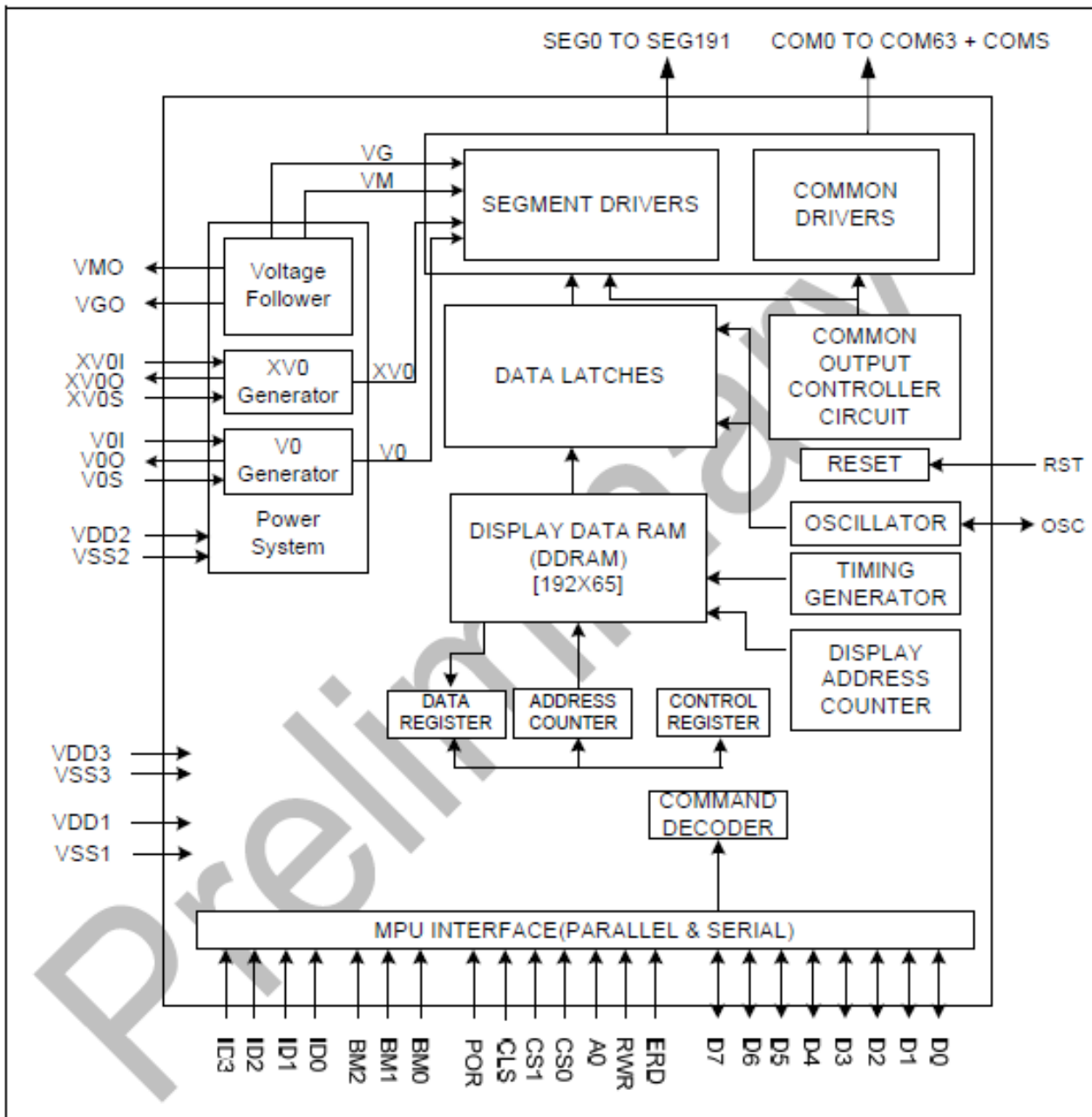

Fig 9.   I²C Interface Protocol
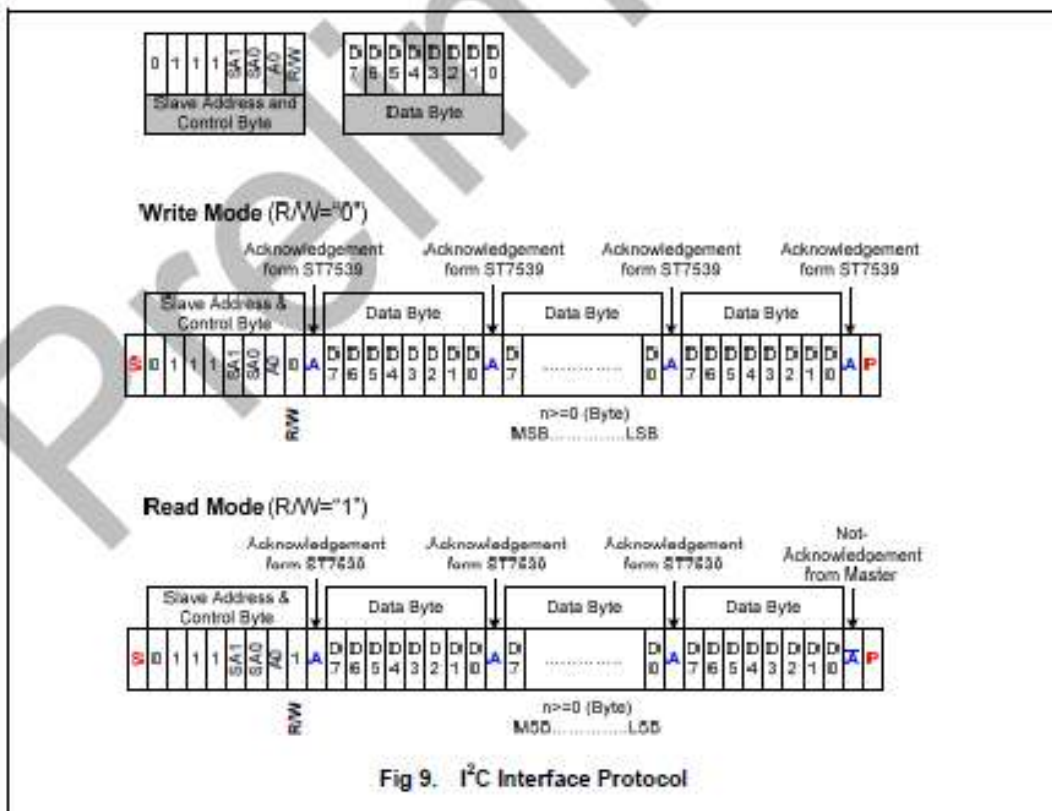
6. Pin define

PIN	SYMBOL	FUNCTIONS
1	VG	LCD driving voltage for segments
2	XV0	LCD driving voltage for commons at positive frame
3	V0	LCD driving voltage for commons at negative frame
4	VSS	Ground
5	VDD	Power supply
6	BM2	BM2,BM0 IS "L", 4-line serial interface
7	BM0	BM2,BM0 IS "H", I2C serial interface
8	SDA	Serial data input
9	SCL	Serial clock input
10	A0	Select for command or data
11	RST	Reset input pin
12	CS0	Chip select pin and slave address pin(i2c)
13	BLA	Backlight power
14	BLK	Backlight ground

7. Block diagram

8. Instructions

INSTRUCTION	A0	R/W (RWR)	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to DDRAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM Only for parallel interface and I^2C
Read Status Byte (parallel interface)	0	1	ID0	MX	MY	WA	DE	0	0	0	Read status byte Only for parallel interface
			0	POR	0	0	0	ID3	ID2	ID1	
Read Status Byte (4-SPI)	0	0	1	1	1	1	1	1	1	0	Read status byte Only for 4 line SPI
	0	1	ID0	MX	MY	WA	DE	0	0	0	
			0	POR	0	0	0	ID3	ID2	ID1	
Set Column Address LSB	0	0	0	0	0	0	CA3	CA2	CA1	CA0	Set column address of RAM
Set Column Address MSB	0	0	0	0	0	1	CA7	CA6	CA5	CA4	
Set Scroll Line	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Specify line address for the 1st display line of DDRAM (vertical scrolling)
Set Page Address	0	0	1	0	1	1	PA3	PA2	PA1	PA0	Set page address of RAM
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Set Vop voltage
			EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
Set Partial Screen Mode	0	0	1	0	0	0	0	1	0	PS	PS=1: Enable partial mode
Set RAM Address Control	0	0	1	0	0	0	1	AC2	AC1	AC0	Set column and page address behavior
Set Frame Rate	0	0	1	0	1	0	0	0	FR1	FR0	Set frame frequency
Set All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all display segments on
Set Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display
Set Display Enable	0	0	1	0	1	0	1	1	1	PD	PD=0: Chip is in power down mode
Scan Direction	0	0	1	1	0	0	0	MY	MX	0	Set COM and SEG scan direction
Software Reset	0	0	1	1	1	0	0	0	1	0	Set software reset
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set Bias	0	0	1	1	1	0	1	0	BR1	BR0	Set internal bias circuit
Set COM End	0	0	1	1	1	1	0	0	0	1	2-byte instruction. Set display duty
			--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	
Partial Start Address	0	0	1	1	1	1	0	0	1	0	Set partial start for partial display screen
			--	--	DST5	DST 4	DST 3	DST 2	DST 1	DST 0	
Partial End Address	0	0	1	1	1	1	0	0	1	1	Set partial end for partial display screen
			--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0	
Test Control	0	0	1	1	1	1	1	1	1	1	Set test command table
			--	--	--	--	--	--	H1	H0	

Note: 1. Do not use instructions not listed in these tables (Command Table).

2. "--" = Disabled bit. It can be either logic 0 or 1.

9. Booster application
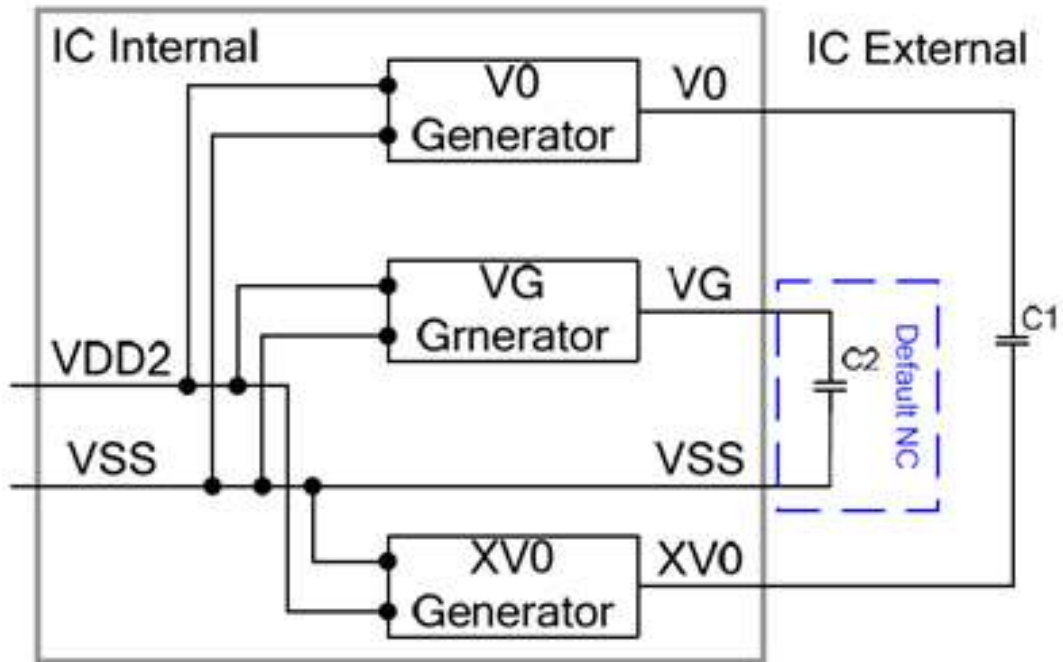
The referential external component values are listed below.

    1. C1=0.1uF~2.2uF (Non-Polar/25V, default 1uF)

    2. C2=0.1uF~2.2uF (Non-Polar/6.3V, default N.C.)

10. Environmental absolute Maximum ratings

ITEM	SYMBOL	CONDITIONS	CRITERION
OPERATING TEMPERATURE	TOPR	-20℃ ~ +70℃	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
STORAGE TEMPERATURE	TSTG	-30℃ ~ +80℃	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION

11. Reliability

ITEM	CONDITIONS	CRITERION
OPERATING TEMPERATURE	HIGH TEMPERTURE +70℃ 96HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -20℃ 96HRS	
STORAGE TEMPERATURE	HIGH TEMPERTURE +80℃ 96HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE - 30℃ 96HRS	
HUMIDITY	40℃ 90%RH 96HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
VIBRATION	· Operating Time: thirty minutes exposure for each direction (X,Y,Z) · Sweep Frequency: 10 ~ 55Hz (1 min) · Amplitude: 1.5mm	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
THERMAL SHOCK	-20℃(30mins) ←→+70℃(30mins) 10 cycles	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION

*NOTE: TEST CONDITION
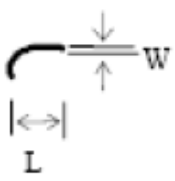
(1)TEMPERATURE AND HUMIDITY: IF NO SPECIFICATION, TEMP. SET AT 25±2℃, HUMIDITY SET AT 60±5%RH
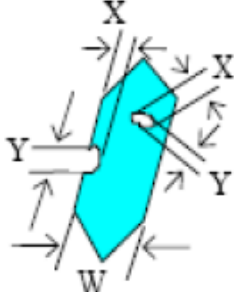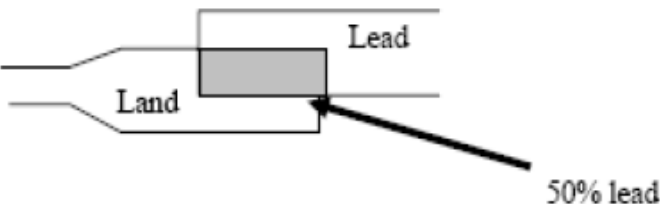
(2) OPERATING STATE: SAMPLES SUBJECT TO THE TESTS SHALL BE IN " OPERATING" CONDITION

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12. Inspection standard of LCM

Classify		Item	Note	AQL
Major	Display state	Short or open circuit	1	0.65
		Contrast defect (dim, ghost)		
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction	2	
		Wrong Back-light	7	
	Non-display	Flat cable or pin reverse	9	
		Wrong or missing component	10	
Minor	Display state	Background color deviation	2	1.5
		Black spot and dust	3	
		Line defect	4	
		Scratch		
		Rainbow	5	
		Pin hole	6	
	Polarizer	Bubble and foreign material	3	
		Scratch	4	
	PCB	Scratch	4	
	Soldering	Poor connection	8	
	Wire	Poor connection	9	

No.	Item	Criterion
1	Short or open circuit	Not allow
	LC leakage	
	Flickering	
	No display	
	Wrong viewing direction	
	Wrong Back-light	
2	Contrast defect	Refer to approval sample
	Background color deviation	

No.	Item	Criterion
3	Point defect, Black spot, dust (incl. Polarizer) $\phi = (X+Y)/2$	(see diagram)

Point Size	Acceptable Qty.
$\phi \leq 0.10$	Disregard
$0.10 < \phi \leq 0.20$	3
$0.20 < \phi \leq 0.25$	2
$0.25 < \phi \leq 0.30$	1
$\phi > 0.30$	0

Unit: mm

No.	Item	Criterion
4	Line defect	(see diagram)

Line		Acceptable Qty.
L	W	
---	$0.015 \geq W$	Disregard
$3.0 \geq L$	$0.03 \geq W$	2
$2.0 \geq L$	$0.05 \geq W$	
$1.0 \geq L$	$0.1 > W$	1
---	$0.05 < W$	Applied as point defect

Unit: mm

No.	Item	Criterion
5	Rainbow	Not more than two color changes across the viewing area.

| No.	Item	Criterion
6	Segment pattern W = Segment width $\phi = (X+Y)/2$	(1) Pin hole $\phi < 0.10mm$ is acceptable. | Point Size	Acceptable Qty
---	---
$\phi \leq 1/4W$	Disregard
$1/4W < \phi \leq 1/2W$	1
$\phi > 1/2W$	0	 Unit: mm
7	Back-light	(1) The color of backlight should correspond its specification. (2) Not allow flickering
8	Soldering	(1) Not allow heavy dirty and solder ball on PCB. (The size of dirty refer to point and dust defect) (2) Over 50% of lead should be soldered on Land. Lead Land 50% lead
9	Wire	(1) Copper wire should not be rusted (2) Not allow crack on copper wire connection. (3) Not allow reversing the position of the flat cable. (4) Not allow exposed copper wire inside the flat cable.
10	PCB	(1) Not allow screw rust or damage. (2) Not allow missing or wrong putting of component.

| 11 | LCD | 2.1.1 chip on the surface |
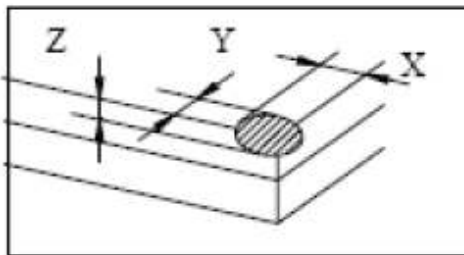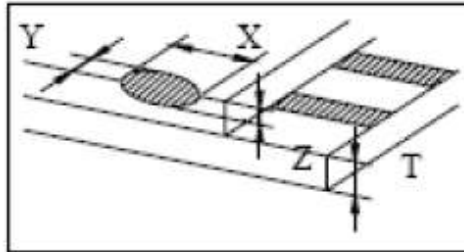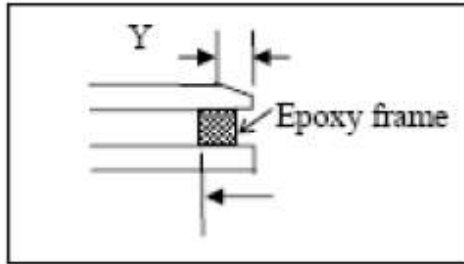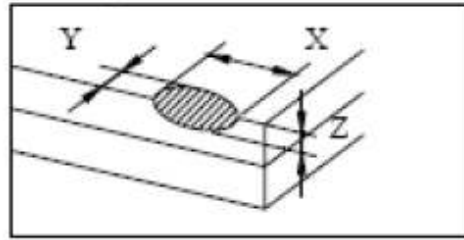
X	Y	Z
>1/8A	≤0.3mm	≤1/2T
≤1/8A	Not enter into epoxy frame	≤T
	Not enter into the inner edge of epoxy	≤1/2T

		2.1.2 chip on the terminal
11	LCD	
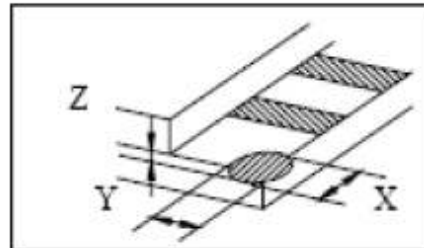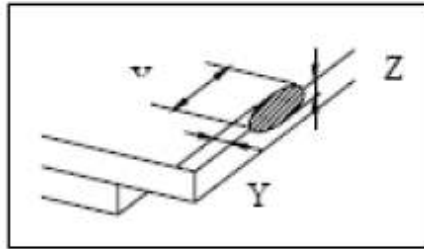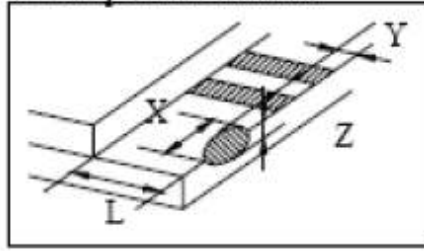
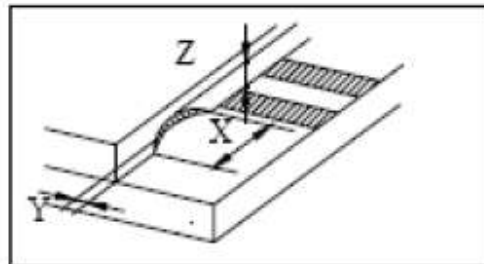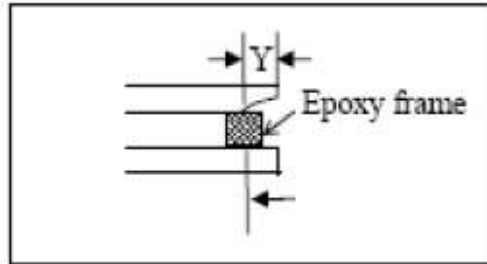| X	Y	Z
>1/8A	≤0.3mm	≤1/2T
≤1/8A	≤1/2L	≤T
≤1/8A 且≤1mm	≤L	≤T
≤1/8A 且≤2mm	≤L	≤1/2T

Note: the distance between crack and contact pad must be greater than the width of 1st contact pad

2.1.3chip out on between side
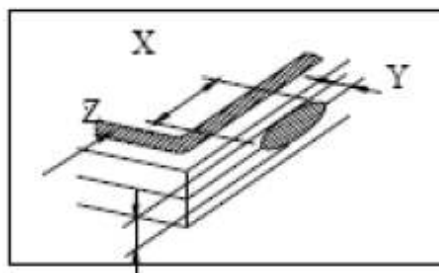
11	LCD	

Epoxy frame

X	Y	Z
≤ 1/8A	Not enter into epoxy frame	Z≤2T
	Not enter into 1/2 epoxy frame	Z≤1/2T

2.1.4 including corner chip and side chip
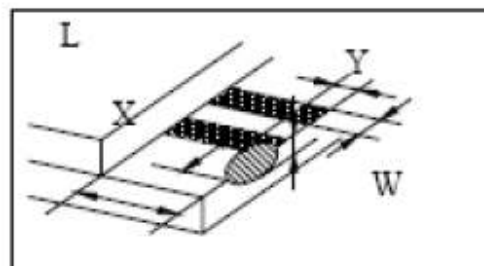
X	Y	Z
>1/8A	≤1/6L	
≤1/8A	≤1/3L	≤1/2T
≤1/4W	≤2/3L	
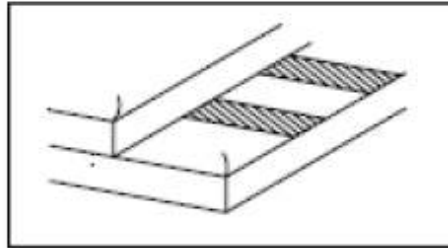
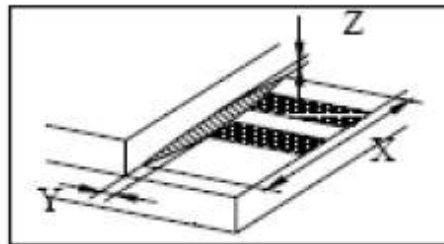|		
11	LCD	**2.2 Chip out** 1) Chip out is that crackles extend to inner edge . 2) Crackles round epoxy frame will be rejected. 3) Chip out on the terminal will be rejected: Z=T length >1mm or Z<T length >2mm 4) The chip out at ITO will be rejected.

2.3 Poor cutting

X	Y	Z
>1/8A	≤0.3	≤1/2T
≤ 1/8A	According to drawing	1/2T≤Z≤T

Any one out of the specification will be rejected.

13. Using LCD modules

(1) Mounting Method

The panel of the LCD Module consists of two thin glass plates with polarizer' which easily get damaged since the Module is fixed by utilizing fitting holes in the printed circuit board. Extreme care should be taken when handling the LCD Modules.

(2) Caution of LCD handling & cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- Isopropyl alcohol

- Ethyl alcohol

- Tricolor trifler thane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water

- Kenton

- Aromatics

(3) Caution against static charge

The LCD Module use C-MOS LSI drivers, so we recommend that you connect any unused input terminal to VDD or VSS, do not input any signals before power is turned on. And ground your body, Work/assembly table. And assembly equipment to protect against static electricity.

(4) Packaging

- Modules use LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

- To prevent modules from degradation. Do not operate or store them exposed directly to sunshine or high temperature/humidity.

(5) Caution for operation

- It is indispensable to drive LCD's within the specified voltage limit since the higher voltage than the limits shorten LCD life. An electrochemical reaction due to direct current causes LCD deterioration, Avoid the use of direct current drive.

- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them. However those phenomena do not mean malfunction or out of order with LCD's，Which will come back in the specified operating temperature range.

- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.

- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the relative condition of 40　C, 50%RH or less is required.

(6) Storage

In the case of storing for a long period of time (for instance.) For years) for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with sealed so as not to enter fresh air outside in it, And with no desiccant.

- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping temperature in the specified storage temperature range.

- Storing with no touch on polarizer surface by the anything else. (It is recommended to store them as they have been contained in the inner container at the time of delivery)

  (7) Safety

- It is recommendable to crash damaged or unnecessary LCD into pieces and wash off liquid crystal by using solvents such as acetone and ethanol.

Which should be burned up later.

-When any liquid crystal leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.