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TI Precision Designs: Verified Design
±10V 4-Quadrant Multiplying DAC

TEXAS INSTRUMENTS

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Circuit Description

This four-quadrant multiplying DAC (MDAC) circuit conditions the current output of an MDAC into a symmetrical bipolar voltage. The design uses an op amp in a transimpedance configuration to convert the MDAC current into a voltage. This stage is followed by an additional amplifier in a summing configuration to apply an offset voltage. The fundamentals of this design can be extended to realize any symmetric or non-symmetric output voltage.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
DAC8811	Product Folder
OPA2277	Product Folder

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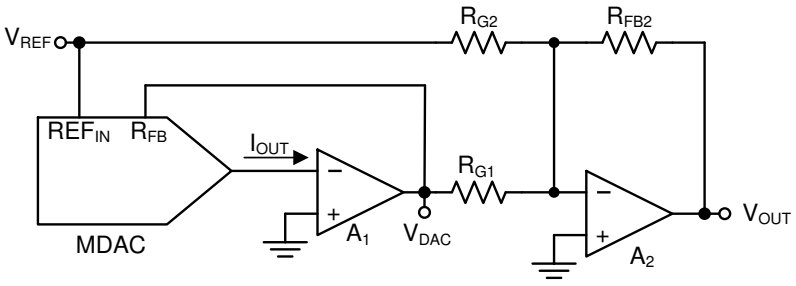
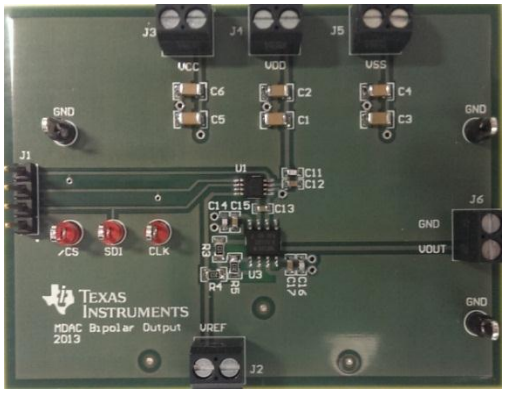




1 Design Summary

The design requirements are as follows:

- DAC Supply Voltage: +5V dc
- Amplifier Supply Voltage: ±15V dc
- Input: 3-wire, 16-bit SPI
- Output: ±10V dc

The design goals and performance are summarized in Table 1. TUE is defined as the total unadjusted error of the system, including errors from each component in the system. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
System Total Unadjusted Error (%FSR)	0.1%	0.087135	0.053985

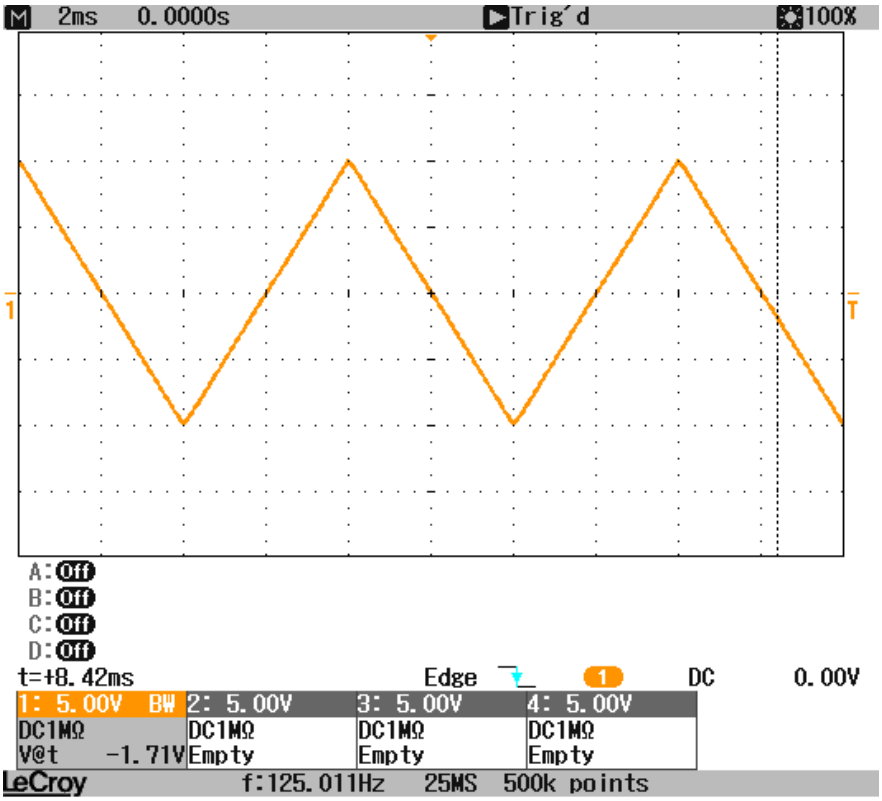


Figure 1: Full-Scale Ramp of Output

2 Theory of Operation

The first stage of the design converts the current output of the MDAC (I_{out}) to a voltage (V_{out}) using an amplifier in a transimpedance configuration. A typical MDAC features an on-chip feedback resistor sized appropriately to match the ratio of the resistor values used in the DAC R-2R ladder. This resistor is available using the input shown in Figure 2 called R_{FB} on the MDAC. The MDAC reference and the output of the transimpedance stage are then connected to the inverting input of the amplifier in the summing stage to produce the output that is defined by Equation 1.

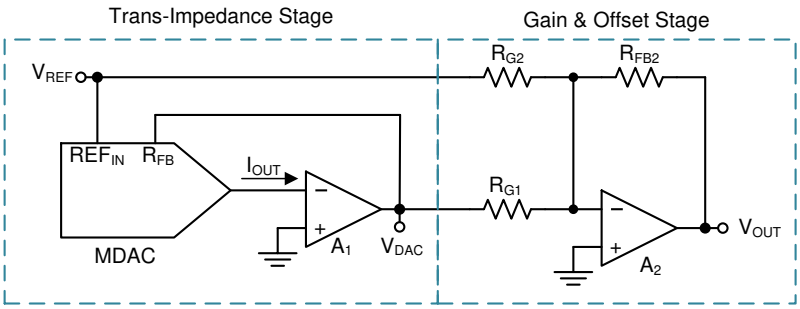
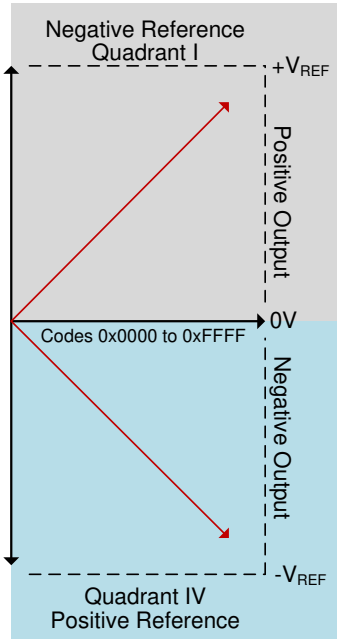


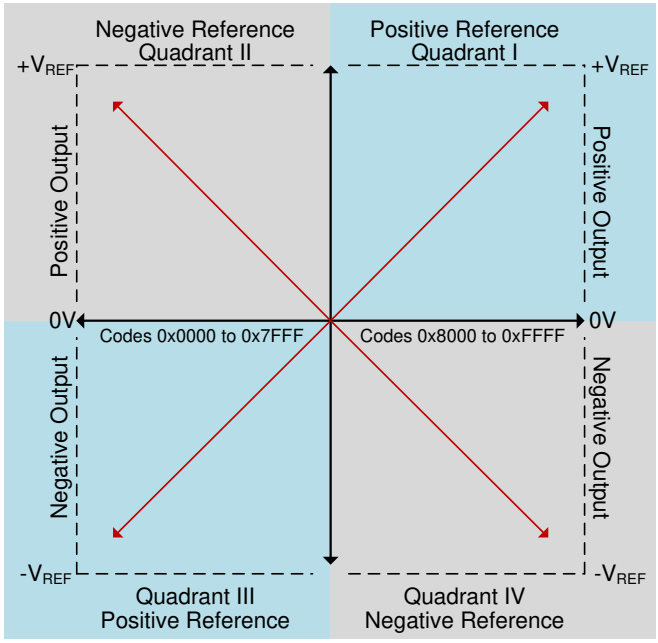
Figure 2: System Diagram

$$V_{OUT}(Code) = \left(\frac{R_{FB2}}{R_{G1}} * \frac{V_{REF} * Code}{2^{bits}}\right) - \left(\frac{R_{FB2}}{R_{G2}} * V_{REF}\right) \quad (1)$$

The resulting system is commonly referred to as a four-quadrant MDAC configuration. A system only including the MDAC and transimpedance stage, highlighted in Figure 2, would be referred to as a two-quadrant configuration because the output is only able to swing positive or negative by changing the reference voltage polarity, illustrated in Figure 3(a). The four-quadrant system is capable of positive or negative output voltages by changing either the reference voltage or by changing DAC codes as illustrated in Figure 3(b).



(a) Two-Quadrant



(b) Four-Quadrant

Figure 3: Two-Quadrant vs. Four-Quadrant Output

2.1 Transimpedance Amplifier Stage

The transimpedance amplifier converts the current output of the MDAC to voltage. This voltage, V_{DAC}, is opposite in polarity to V_{REF}, making the output range of V_{DAC} between 0 and -V_{REF}. Amplifier selection for this stage is one of the most critical decisions for this design. This design is focused on delivering a highly accurate, un-calibrated, dc signal. Input offset voltage and input bias current are the two most critical op amp specifications to achieve accuracy. Ideally the amplifier selected will contribute negligible error to the system.

2.1.1 Input Bias Current

The output of the MDAC is a current, so any amplifier input bias current, I_B, directly adds or subtracts from the MDAC output. This results in an offset error at the voltage output of the amplifier. The equation for this offset is shown below:

$$V_{DAC\_OFFSET} = i_B * R_{FB} \quad (2)$$

The value of R_{FB} is not always explicitly listed in the MDAC's datasheet but it is typically equal to the input impedance of the reference pin, which is listed in the theory of operation section or in the electrical characteristics table. Input bias current for CMOS amplifiers tends to be very small, usually on the order of picoamperes, so finding one with small input bias current can be an easy task with most modern amplifier portfolios. Because the offset contribution of input bias current is constant, its effects will be more significant with small reference values or with high-resolution devices because of the reduced LSB size.

2.1.2 Input Offset Voltage

The effect of input offset voltage is a linearity error at the output of the transimpedance stage, V_{DAC}. Input offset voltage introduces non-linearity because the output impedance of the IOUT pin of the MDAC creates a code-dependent gain on the amplifier input offset voltage. In the circuit shown in Figure 4, the input offset voltage of the amplifier is subject to non-inverting amplification with a gain of ($1+R_{FB}/R_{OF}$), where R_{OF} changes based on the DAC code. R_{OF} represents the output impedance of the I_{OUT} pin.

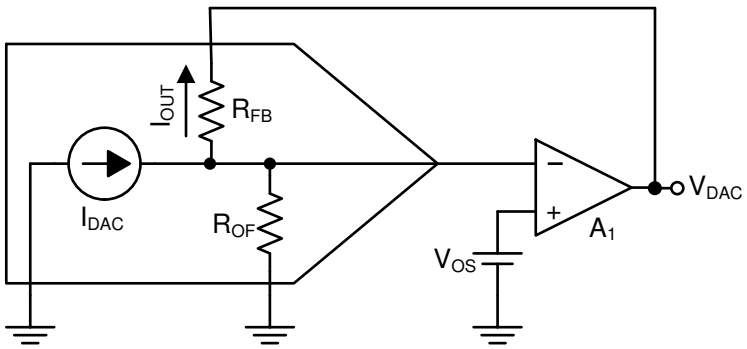


Figure 4: DAC + Transimpedance Stage Model

In order to calculate the impedance seen at IOUT at each code, the following generic procedure can be used:

1. Analyze the R-2R ladder architecture of the DAC
2. Write nodal equations for each rung of the ladder
3. Write equations to define I_{OUT} impedance versus code
4. Iterate through all the codes

To be practical, this process requires the use of software to iterate through all of the codes available for a modern DAC which typically has 8-bits or more of resolution. The design archive for this document includes MATLAB files that were used for this analysis. A simplified example using a 5-bit DAC with 2 MSBs segmented will be used to step through the above procedure. In section 2.1.2.5 results will be shown from the MATLAB simulations used to model the DAC8811.

2.1.2.1 Internal Architecture

The specific topology implemented in the R-2R ladder of the MDAC will impact the impedance seen at Iout for each code. Segmentation is frequently implemented for R-2R ladder designs to improve linearity and the segmentation scheme and is a key concern in studying the MDACs topology. Although some devices may implement complex trimming schemes to deliver highly matched resistors, a practical approximation can be made by using just the number of segmented and non-segmented bits along with the ratio of resistor values for each leg.

Non-segmented bits are normal R-2R ladder legs where there is a resistor of value 2R that connects between V_{REF} and either I_{OUT} or GND. In between each 2R leg of the non-segmented ladder is a resistor of value R. The R resistor causes a binary weighted current divider effect on each of the 2R legs.

Segmented bits are similar to regular R-2R legs, except there is no R resistor between each leg, causing each segmented leg to be equally weighted current dividers. An example is shown in Figure 5 for a 5-bit MDAC with 2 bits of segmentation. Each bit of the 5-bit DAC in Figure 5 is labeled as B_n, where B_1 controls the first two segmented switches.

The segmentation scheme and the values of the resistor may vary slightly from device to device. The theory of operation section of the chosen MDAC datasheet will describe the architecture of the R-2R ladder.

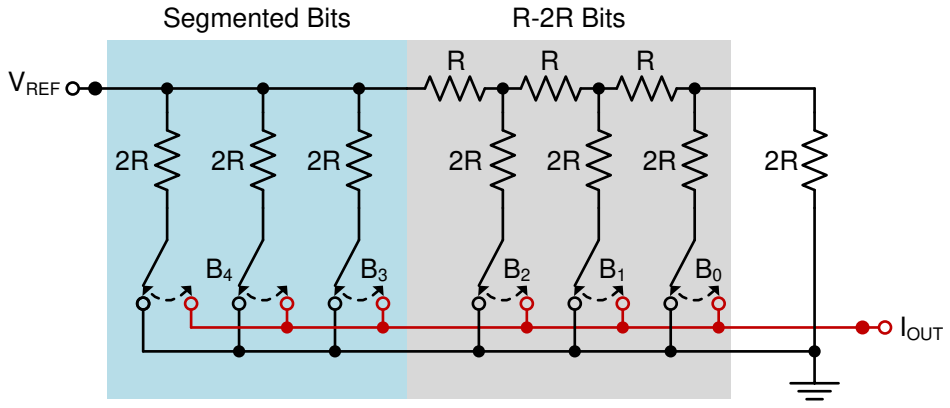


Figure 5: 5-Bit R-2R Ladder, 2 segmented bits

2.1.2.2 Nodal Equations

In order to iterate through all the bit combinations it is necessary to write the nodal equations for this ladder network. Equations for each node in the ladder that is not a switch and is not part of the segmentation scheme will be written. The segmented node equations are straightforward.

In this case the resistors connected to switches controlled by bits B_3, B_4 and B_5 will receive nodal equations. Since the goal is to calculate the equivalent dc resistance seen from I_{OUT}, V_{REF} can be effectively grounded, as shown in Figure 6.

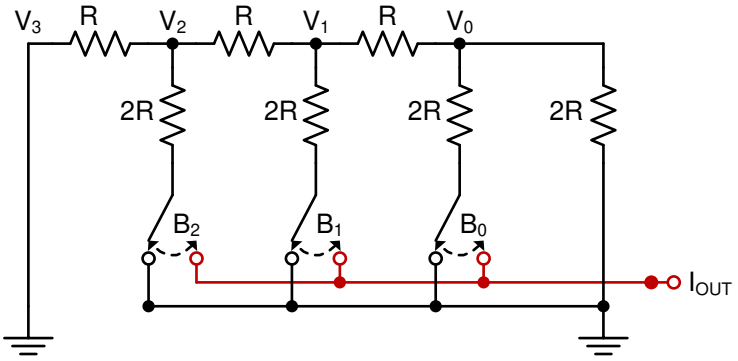


Figure 6: Simplified Equivalent model for 5-Bit, 2 Bit Segmented Ladder

The equations for this example are shown below. Although V_2 is equal to zero it remains in Equation 3 to highlight the pattern that occurs in all the nodes except for the LSB node. In these equations the B_n coefficients represent the binary value (0 or 1) of the respective bits of the DAC data register. V_{IOUT} is the voltage at the I_{OUT} terminal.

$$V_2 = \frac{B_2 * V_{IOUT}}{5} + \frac{2}{5} * (V_3 + V_1) \tag{3}$$

$$V_1 = \frac{B_1 * V_{IOUT}}{5} + \frac{2}{5} * (V_2 + V_0) \tag{4}$$

$$V_0 = \frac{B_0 * V_{IOUT}}{4} + \frac{V_1}{2} \tag{5}$$

This method can be extended for any MDAC with an R-2R ladder as follows:

n: number of non-segmented bits *i: bit number*

$$0 < i < n \rightarrow V_i = \frac{B_i * V_{IOUT}}{5} + \frac{2}{5} * (V_{i+1} + V_{i-1}) \tag{6}$$

$$i = 0 \rightarrow V_i = \frac{B_i * V_{IOUT}}{4} + \frac{V_{i+1}}{2} \tag{7}$$

2.1.2.3 Input Impedance of I_{OUT}

First Equations 3, 4, and 5 simplified to be defined in terms of bits.

$$V_2 = V_{IOUT}\left(\frac{B_2}{4} + \frac{B_1}{8} + \frac{B_0}{16}\right) \tag{8}$$

$$V_1 = V_{IOUT}\left(\frac{B_2}{8} + \frac{5*B_1}{16} + \frac{5*B_0}{32}\right) \tag{9}$$

$$V_0 = V_{IOUT}\left(\frac{B_2}{16} + \frac{5*B_1}{32} + \frac{21*B_0}{64}\right) \tag{10}$$

Using the voltage equations for each node of the R-2R ladder, equations can be written that define the current going through each leg of the ladder and finally an equation can be written defining the sum of all ladder currents seen at IOUT. Iterating through all possible bit combinations will show the changing input impedance of the IOUT pin versus code. Note that leading B coefficients are added to these equations when necessary to ensure that the bits that are LOW will not be summed to the current going into IOUT.

$$i_4 = B_4\frac{V_{IOUT}}{R}, i_3 = B_3\frac{V_{IOUT}}{2R}, i_2 = B_2\frac{V_{IOUT} - V_2}{2R}, i_1 = B_1\frac{V_{IOUT} - V_1}{2R}, i_0 = B_0\frac{V_{IOUT} - V_0}{2R} \tag{11-16}$$

$$i_{OUT} = i_0 + i_1 + i_2 + i_3 + i_4 \tag{17}$$

$$R_{OS} = \frac{V_{IOUT}}{i_{OUT}} \tag{18}$$

R_{OS} is recorded for each code in order to analyze the results. Matrix math in MATLAB is used to iterate through all possible combinations to generate the curves in Figures 7-10.

2.1.2.4 Iterations & Results

The plots below approximate what R_{OS} looks like, normalized to one unit of resistance R as defined by the R-2R ladder of the DAC, across all codes for both the 5-Bit, 2 MSB segmented example and the 16-Bit, 3 MSB segmented DAC8811.

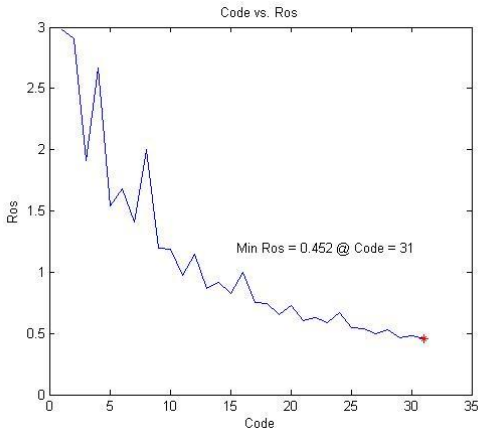


Figure 7: 5-Bit DAC, Code vs. R_{OS}

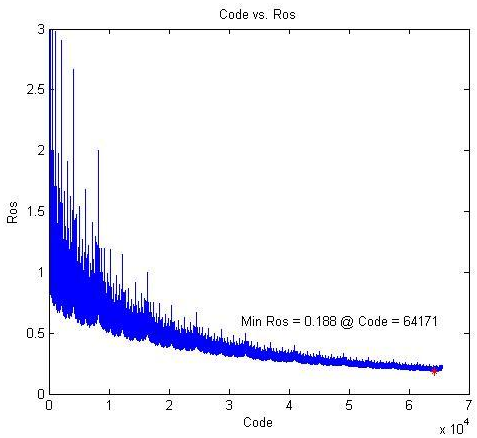


Figure 8: 16-Bit DAC, Code vs. R_{OS}

The gain applied to the input offset voltage for each code can then be calculated based on the value of R_{OS} and R_{FB}. The value of R_{FB} must be equal to the parallel and series combination of all of the resistors in the R-2R ladder design. For the 5-Bit, 2 MSB segmented example, R_{FB}=R/2. For a 16-Bit, 3 MSB segmented DAC, R_{FB}=R/4.

$$Gain_{Vos} = 1 + \frac{R_{FB}}{R_{OS}} \tag{19}$$

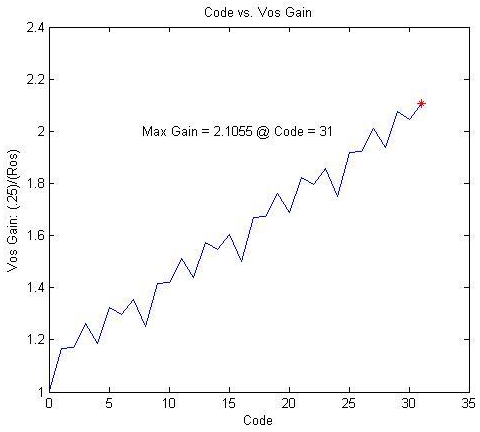


Figure 9: 5-Bit DAC, Code vs. V_{OS} Gain

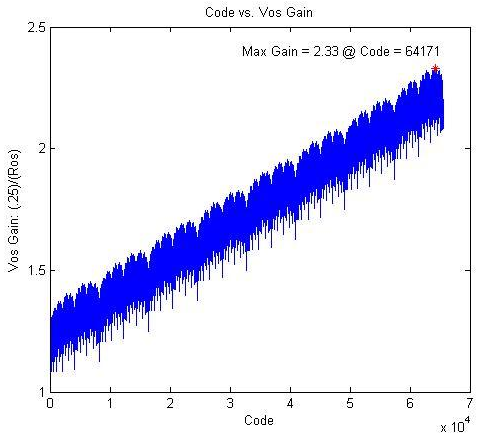


Figure 10: 16-Bit DAC, Code vs. V_{OS} Gain

This variable gain on the offset voltage will cause a linearity error at the output of the transimpedance stage. There is a linear component to this gain error and the values calculated in this analysis could be used to calibrate the linear component of this error. The MATLAB code to generate the curves shown in Figure 9 and Figure 10 are included in this documents design archive.

In this case, the non-linear gain error is simply treated as an INL error and only the maximum error is recorded for the circuit to calculate the worst case INL contributions due to VOS. The worst case INL error occurs when VOS experiences the highest gain, shown in Figure 10. For the DAC8811, this occurs at approximately code 64171.

2.2 Summing Amplifier Stage

The summing amplifier outputs the difference between the two inputs with individual gain applied to each of them based on their respective input impedances. The reference input (V_{REF}) acts as a DC offset multiplied by a gain of $-R_{FB2}/R_{G2}$. The output of the transimpedance stage (V_{DAC}) receives a gain equal to $-R_{FB2}/R_{G1}$.

V_{DAC} has an output of 0 to $-V_{REF}$ and the system has an output of $\pm V_{REF}$. The resistor ratios are then determined using two end point equations derived from Equation 1.

Case 1: Code = 0, $V_{OUT} = -V_{REF}$

$$-V_{REF} = -\left(\frac{R_{FB2}}{R_{G2}} * V_{REF}\right)$$

$$R_{G2} = R_{FB2} \tag{20}$$

Case 2: Code = 2^{bits} , $V_{OUT} = V_{REF}$

$$V_{REF} = \left(\frac{R_{FB2}}{R_{G1}} * V_{REF}\right) - V_{REF}$$

$$R_{G1} = \frac{R_{FB2}}{2} \tag{21}$$

2.3 Passive Component Values

Large resistors will introduce noise and therefore decrease system accuracy. Small resistors will draw more current, and subsequently increase power, which may affect load regulation of the reference. The base values for the resistors used in this design are based on the resistor ratios discussed in Section 2.2 while limiting the current drawn from the reference to 500µA. The maximum current that the amplifier in the transimpedance stage will sink is 1mA. The precision required is determined from the simulation results shown in Section 4.2.

- R_{G1} = 10kΩ ±0.1%
- R_{G2} = 20kΩ ±0.1%
- R_{FB2} = 20kΩ ±0.1%

There is a small 12 pF capacitor between the IOUT pin and the R_{FB} pin that is not installed by default. This is a compensation capacitor that may be needed if gain peaking is observed due to parasitics. Since the exact value is not critical for this component, 10% tolerance is acceptable.

3 Component Selection

The goal of this design is to achieve 0.1% TUE (%FSR). The error contributions of each component can be subtracted from the overall error budget to ensure that the design goal is met. Each component subtracts from the error budget for the rest of the components.

3.1 DAC Selection

Generally, MDACs are used in high performance applications that take full advantage of their strong dc specifications. Since the typical MDAC does not feature an on-board output amplifier, they do not exhibit an offset error. Instead MDACs are only specified with INL, DNL, and gain errors and usually they show very strong linearity specifications. Other differences are application related, such as resolution, number or channels, control interface, or other auxiliary features. The DAC is chosen first in this system and sets the error baseline. All the other components will be chosen using the remaining head-room for the system.

For this design the DAC8811 is chosen. DAC8811 delivers excellent linearity and low gain error to leave much of the error budget to the rest of the discrete components. DAC8811 also features a serial interface, which is often preferred over a parallel bus since it uses fewer pins.

3.2 Amplifier Selection

Two amplifiers must be selected in this design: one for the transimpedance stage and one for the summing amplifier stage.

For the transimpedance stage, low input bias current and low input offset voltage are the most critical parameters to deliver accurate dc operation. Input bias current will create a dc offset across the transfer function. Input offset voltage will create an integral non-linearity error. Both of these error sources may be increased by gain in the summing amplifier stage. Full details on the implications of each of these specifications are explained in sections 2.1 and 2.2 of this document.

Similar concerns are applicable to the summing stage of this design. Input bias current is not as critical since the impedance in the summing stage is typically be small enough, making the impact of input bias current negligible compared to other error sources. Input offset voltage should still be considered since V_{OS} of the summing amplifier directly contributes to offset error of the system.

The OPA277 core was selected for both stages because it delivers very low input offset voltage and very low input bias current. The OPA2277 is the dual package offering of the OPA277 core with very similar specifications and can help reduce PCB area.

Other amplifier considerations such as bandwidth, temperature drift and slew rate may also be relevant depending on the application requirements.

3.3 Passive Component Selection

Resistor matching is very important on the amplifying stage since resistor mismatch can cause both offset and gain errors in the system. High tolerance components must be used to keep the error within the allowance. In this design $\pm 0.1\%$ tolerance resistors were suitable to meet the accuracy requirements, but this can be adjusted to enhance performance. The capacitor between the IOUT pin and the R_{FB} pin is a compensation capacitor that does not require high tolerance.

4 Simulation

Simulation is split into two sections, one for the DAC + transimpedance stage and one for the summing stage. The results from both simulations will be combined to calculate overall system performance.

4.1 DAC + Transimpedance Stage

The INL and offset error effects of the MDAC and transimpedance stage were simulated using a separate model that was developed in MATLAB, as described in Section 2.1.1 and 2.1.2. These results, along with the INL and gain error specifications from the MDAC datasheet, are used to model the MDAC + transimpedance stage in TINA-TI.

The DAC + Transimpedance stage model uses an ideal summing stage in order to obtain the error contribution of just the DAC and transimpedance amplifier at the output of the system.

The TINA-TI™ schematic shown in Figure 11 represents the DAC + transimpedance stage model. The results are shown in Table 2 and Figure 12. The results of this stage will be used with the results of the summing stage in order to determine the overall system offset error, gain error and total unadjusted error (TUE).

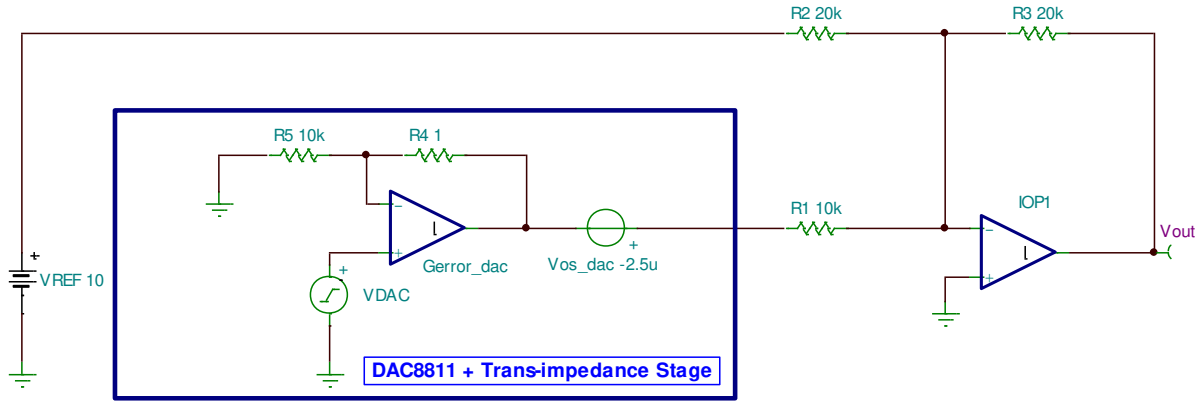


Figure 11: DAC + Transimpedance Stage Model

Table 2. Simulated DAC & Transimpedance Stage Performance

Parameter	Simulated Value
Negative Full-Scale Voltage (V)	-9.999995
Zero-Scale Voltage (mV)	1.005
Positive Full-Scale Voltage (V)	10.002008
Offset Error (%FSR)	0.000025
Gain Error (%FSR)	0.010000
INL Error (%FSR)	0.001530
Total Unadjusted Error (%FSR)	0.010116

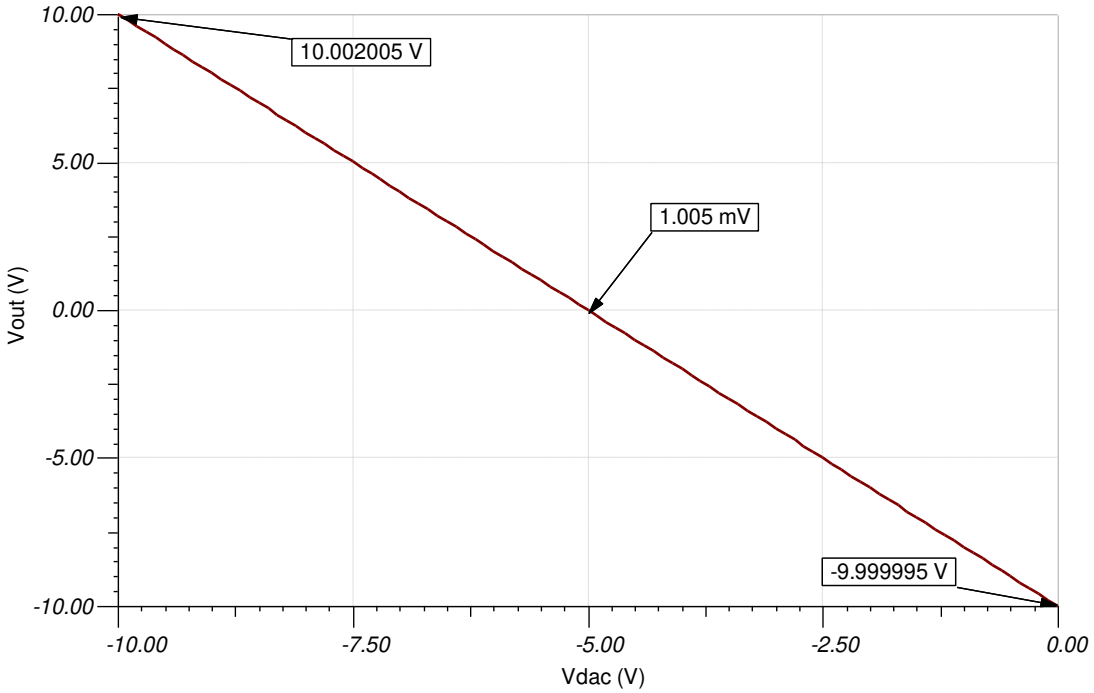


Figure 12: DAC + Transimpedance Stage, Output Transfer Function

The following equations are used to calculate the error parameters in Table 2 based on the information in Figure 12. The total unadjusted error equation uses a root sum squared (RSS) technique to sum uncorrelated error sources.

$$OffsetError_{(\%FSR)} = \frac{\left|V_{OUT_{SIM\,(MIN)}} - V_{OUT_{Ideal\,(MIN)}}\right|}{V_{OUT_{Ideal\,(MAX)}} - V_{OUT_{Ideal\,(MIN)}}} * 100 \tag{22}$$

$$GainError_{(\%FSR)} = \frac{\left|\left(V_{OUT_{SIM\,(MAX)}} - V_{OUT_{SIM\,(MIN)}}\right) - \left(V_{OUT_{SIM\,(MAX)}} - V_{OUT_{IDEAL\,(MIN)}}\right)\right|}{V_{OUT_{IDEAL\,(MAX)}} - V_{OUT_{IDEAL\,(MIN)}}} * 100 \tag{23}$$

$$INL\_Error_{(\%FSR)} = \frac{\left(INL\_Error_{DAC\_LSBs} * \frac{V_{REF}}{2^{bits}}\right) * \left(\frac{R_{FB2}}{R_{G1}}\right)}{V_{OUT_{IDEAL\,(MAX)}} - V_{OUT_{IDEAL\,(MIN)}}} * 100 \tag{24}$$

$$TUE_{(\%FSR)} = \sqrt{Offset_{ERROR(\%FSR)}^{2} + Gain_{ERROR(\%FSR)}^{2} + INL_{ERROR(\%FSR)}^{2}} \tag{25}$$

4.2 Summing Stage

The TINA-TI™ schematic shown in Figure 13 uses the OPA277 model and Monte-Carlo analysis for the resistor network to simulate the summing stage and to select appropriate resistor tolerances to meet the system accuracy goals. In this model the DAC and transimpedance stage are represented by an ideal voltage source sweeping from 0 to -10V.

Resistors of 0.1% tolerance were found suitable to meet 0.1% system TUE, but tighter tolerance resistors could be used to enhance results.

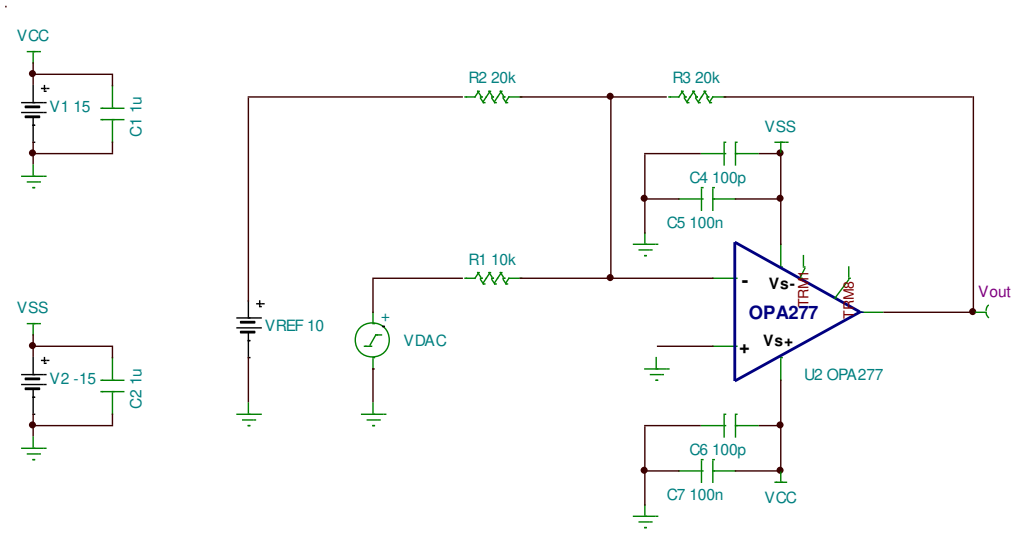


Figure 13: Summing Stage Model

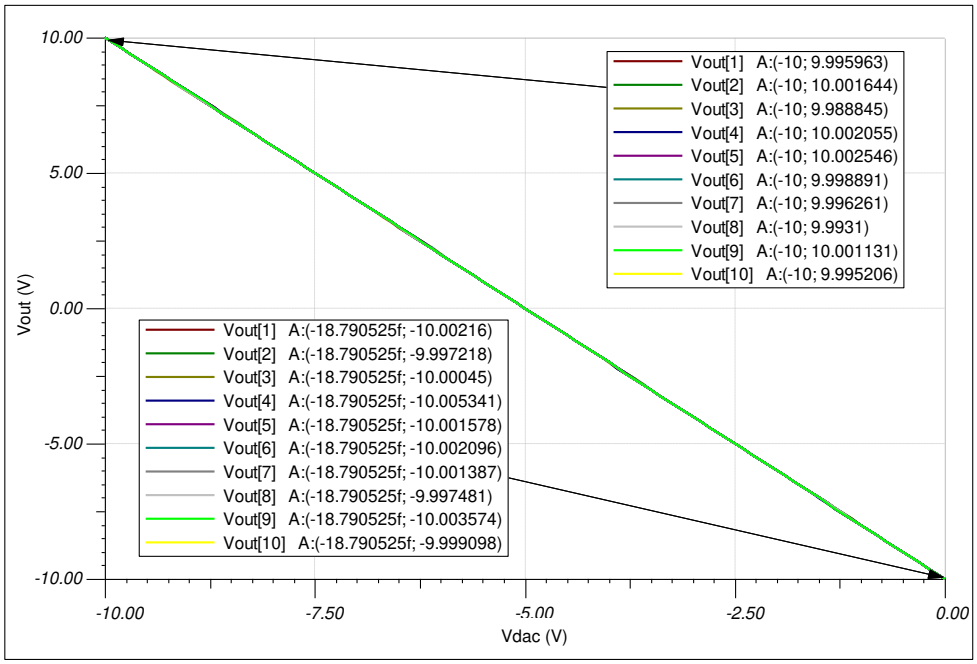


Figure 14: Monte Carlo Results

The results from 10 iterations of the Monte-Carlo simulation of the summing stage are shown in Tables 3 & 4. Figure 14 shows a subset of the Monte-Carlo dc transfer function simulations.

Table 3. Simulated Summing Stage Value

	Min	Max	Average	Std. Dev. (σ)
Offset error (mV)	0.4841	5.8023	0.8000	2.5298
Full-Scale Range (V)	19.9938	20.0062	19.9995	0.0153
|Full-Scale Error| (mV)	0.0730	6.2250	0.0041	2.9640

The standard deviation of the Monte-Carlo results can be used to generate a realistic error figure for the system by multiplying the standard deviation by 3, commonly referred to as a 3-σ system. This error should encompass 99.7% of systems, leaving out absolute worst-case resistor mismatches that are highly unlikely to occur. These errors are summarized in Table 4. The equations used to calculate the error values are shown below:

$$OffsetError_{(\%FSR)} = \frac{3 * \sigma_{OffsetError}}{V_{OUT_{IDEAL(MAX)}} - V_{OUT_{IDEAL(MIN)}}} * 100 \quad (26)$$

$$GainError_{(\%FSR)} = \frac{3 * \sigma_{GainError}}{V_{OUT_{IDEAL(MAX)}} - V_{OUT_{IDEAL(MIN)}}} * 100 \quad (27)$$

Table 4. Simulated Summing Stage Performance

Parameter	Simulated Value
Offset Error (%FSR)	0.0379
Gain Error (%FSR)	0.0763
INL Error (%FSR)	0.0000
Total Unadjusted Error (%FSR)	0.0852

4.3 System Simulation

The DAC+ transimpedance stage results are root sum squared with the summing stage simulation results in order to see the results of the combined stages. INL error is taken directly from the DAC + transimpedance simulation since the summing stage is completely linear.

Table 5. Simulated System Performance

Parameter	Simulated Value	Goal
Offset Error (%FSR)	0.037948	n/a
Gain Error (%FSR)	0.076931	n/a
INL Error (%FSR)	0.001530	n/a
Total Unadjusted Error (%FSR)	0.087135	0.1

$$OffsetError_{(System)} = \sqrt{OffsetError^2_{(DAC+Trans)} + OffsetError^2_{(Summing)}} \quad (28)$$

$$GainError_{(System)} = \sqrt{GainError^2_{(DAC+Trans)} + GainError^2_{(Summing)}} \quad (29)$$

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

General PCB layout best-practices should be followed for this design. The transimpedance stage summing node should be kept as small as possible and a pour cut-out should be placed underneath to reduce parasitics. Similar guidelines should be followed for the summing amplifier stage.

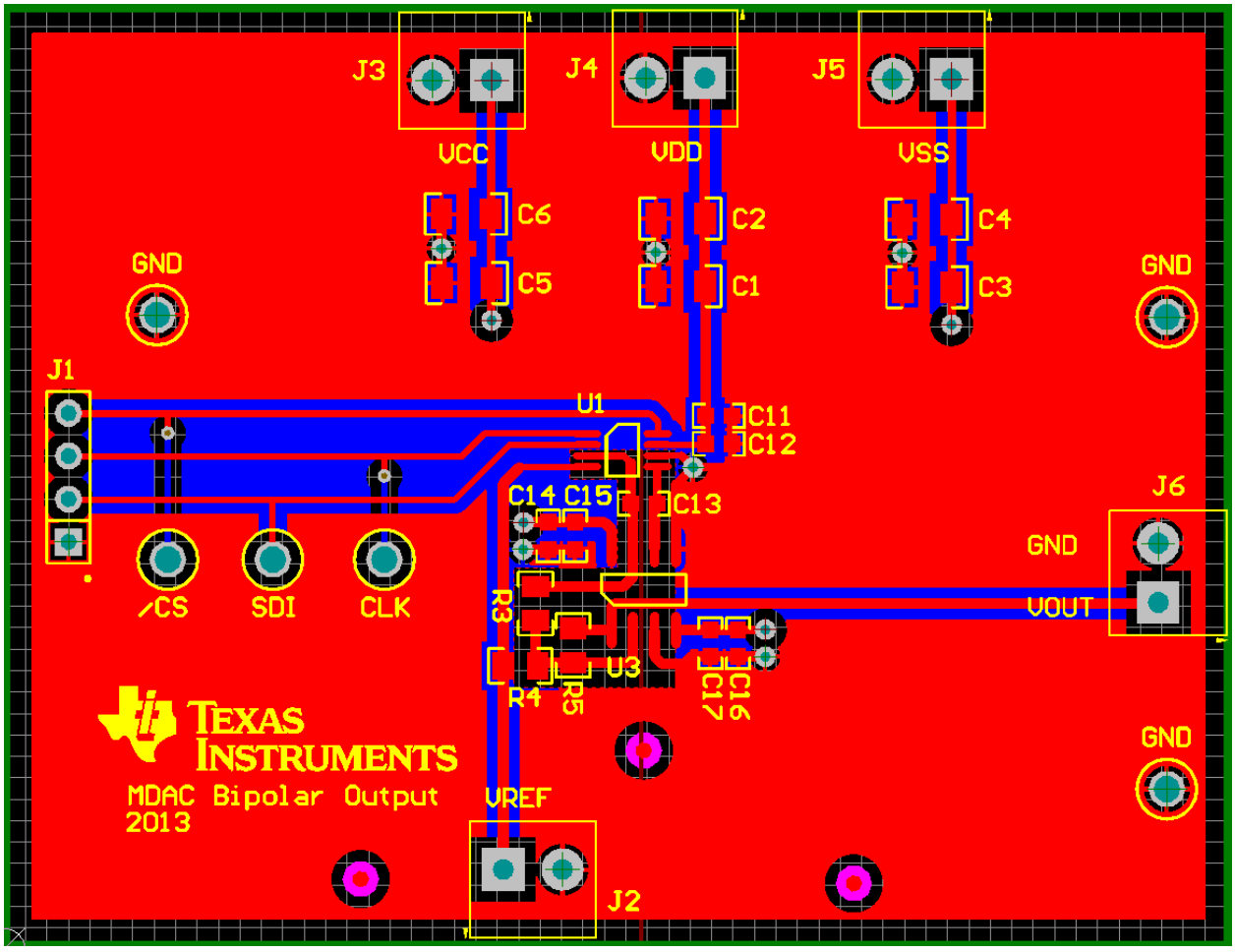


Figure 15: PCB Layout

6 Verification & Measured Performance

6.1 Transfer Function

The graph in Figure 16 was collected by applying input codes from 0 to 65535 to the DAC and measuring the output voltage on a single system.

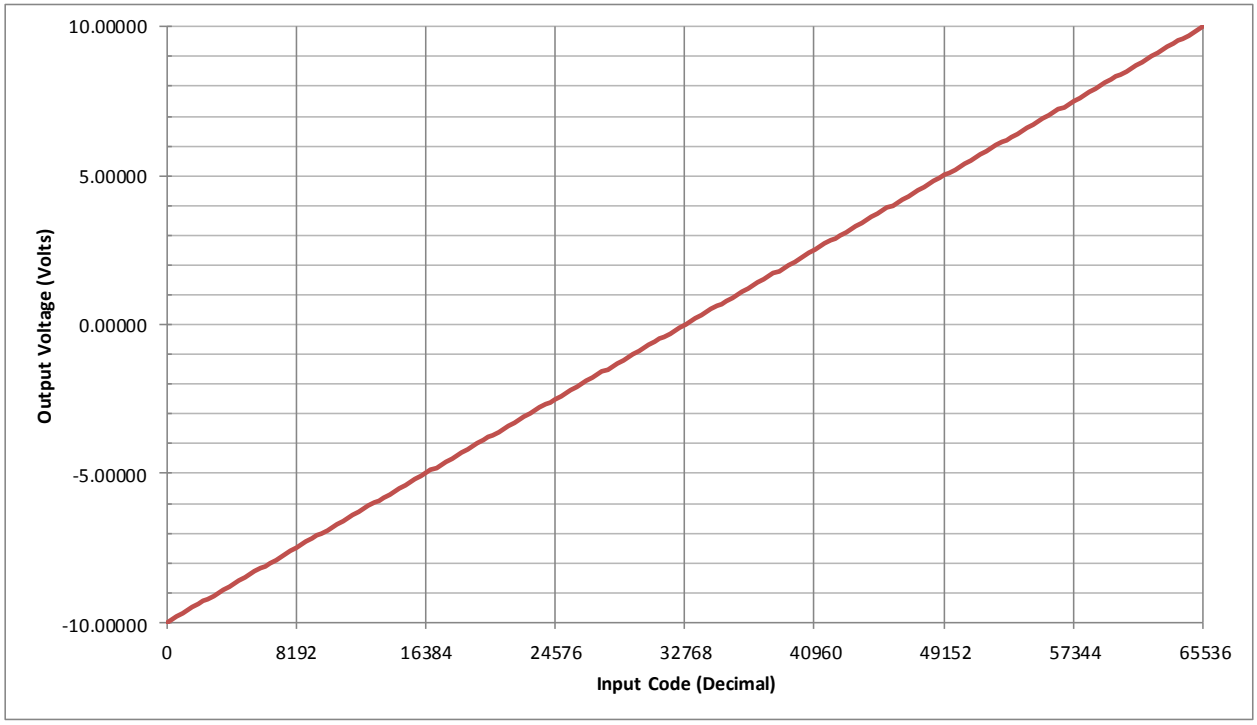


Figure 16: Measured Transfer Function

To easily visualize the error of the system, the difference between the ideal output voltage and measured output voltage of the circuit in %FSR is plotted in Figure 17.

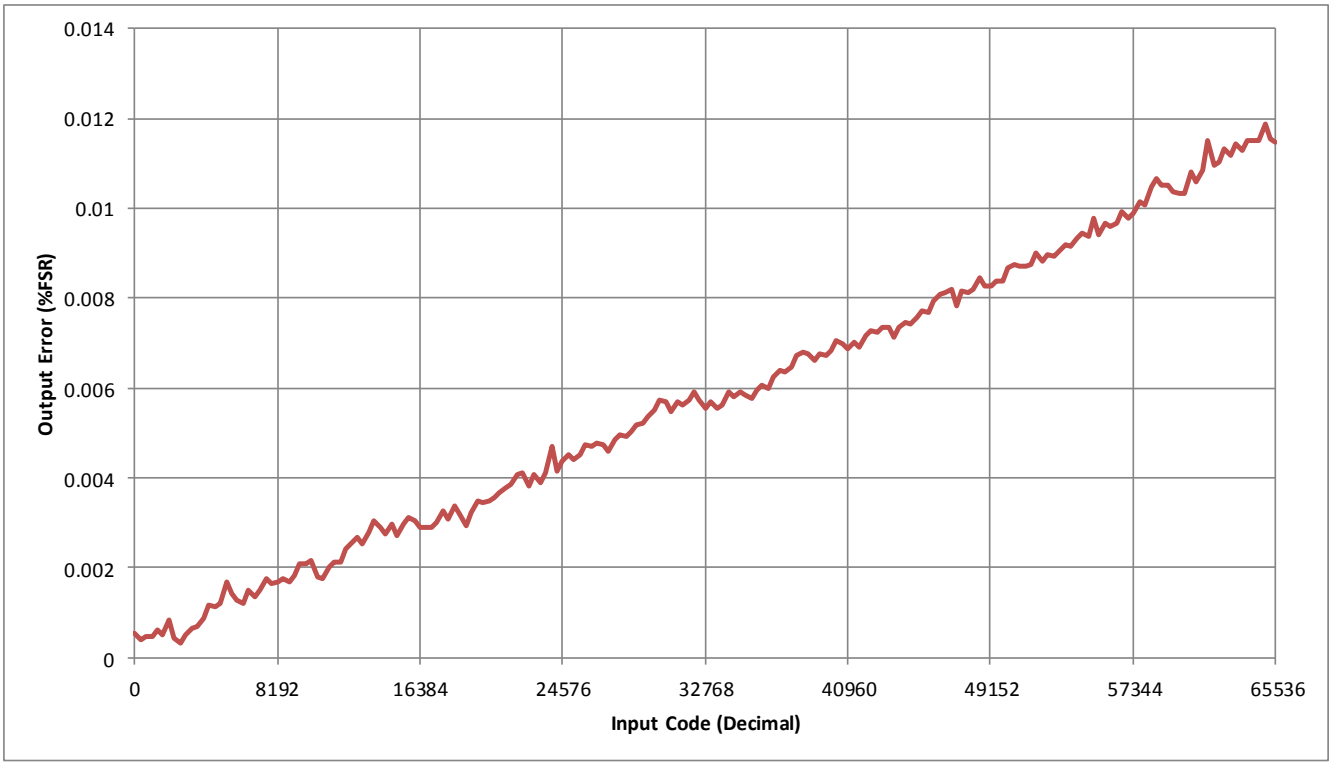


Figure 17: Output Voltage Error vs. Input Code

Table 6 summarizes the average results observed over 10 units. These results were measured using a two-point line of best fit measured at codes 485 and 64714. The equations used to calculate these values are shown in Equations X and Y

Table 6. Average Measured Circuit Performance

Parameter	Measured Value	Simulated	Goal
Offset Error (%FSR)	0.001374	0.037900	n/a
Gain Error (%FSR)	0.053619	0.076900	n/a
INL Error (%FSR)	0.001330	0.001530	n/a
Total Unadjusted Error (%FSR)	0.053985	0.087135	0.1

$$GainError_{(\%FSR)} = \frac{\left(V_{OUT_{REAL(64714)}} - V_{OUT_{REAL(485)}}\right) - \left(V_{OUT_{IDEAL(64714)}} - V_{OUT_{IDEAL(485)}}\right)}{V_{OUT_{IDEAL(64714)}} - V_{OUT_{IDEAL(485)}}} * 100 \quad (30)$$

$$OffsetError_{(\%FSR)} = \frac{V_{OUT_{REAL(485)}} - \left(\frac{V_{OUT_{REAL(64714)}} - V_{OUT_{REAL(485)}}}{64714 - 485} * 485\right) - V_{OUT_{IDEAL(MIN)}}}{V_{OUT_{IDEAL(MAX)}} - V_{OUT_{IDEAL(MIN)}}} * 100 \quad (31)$$

7 Modifications

The components in this design were selected based on the design goals outlined at the beginning of this document. The components may differ depending on the constraints of a different design. The resistor tolerance was selected to meet the 0.1%FSR goal. By improving the tolerance of the resistors a lower TUE can be achieved.

Most alternative MDACs will offer comparable linearity, gain error, and offset error but may show different interface options, channel count, resolution, and other auxiliary features. Table 7 offers options to expand the channel count of this design.

This design was not simulated or measured over temperature. The OPA277 features excellent input offset voltage drift specifications. This drift could be improved by selecting a zero-drift chopper amplifier, but additional noise may be introduced at the output of the system.

Table 7. Alternate DAC Options

DAC	Resolution	Channel Count	Interface	INL Error	Full Scale Error
DAC8811	16-Bit	1	SPI	±1 LSB	±1 mV
DAC8812	16-Bit	2	SPI	±1 LSB	±0.75 mV
DAC8814	16-Bit	4	SPI	±1 LSB	±0.75 mV
DAC8822	16-Bit	2	Parallel	±1 LSB	±1 mV

Table 8. Alternate Amplifier Options

Amplifier	Supply Voltage	Bandwidth	Offset Voltage (Typ)	Offset Drift (Typ)	Quiescent Current	Input Bias Current (Typ)	Input Voltage Noise (0.1Hz to 10Hz)
OPA2277	±18 V	1MHz	±10 µV	0.1 µV/°C	790 µA	±0.5 nA	220 nVpp
OPA211	±18 V	80 MHz	±30 µV	0.35 µV/°C	3.6 mA	±50 nA	80 nVpp
OPA188	±18 V	2 MHz	±6 µV	0.085 µV/°C	450 µA	±160 pA	250 nVpp
OPA170	±18 V	1.2 MHz	±250 µV	0.3 µV/°C	110 µA	±8 pA	2 µVpp

8 About the Authors

Eugenio Mejia is an applications engineer intern in the precision digital to analog converters group at Texas Instruments.

Kevin Duke is an applications engineer in the precision digital to analog converters group at Texas Instruments where he supports industrial and catalog products and applications. Kevin received his BSEE from Texas Tech University in 2010.

Navin Kommaraju is the systems and applications manager in the precision digital to analog converters group at Texas Instruments. Navin received his BTech in Electrical and Electronics Engineering from the Indian Institute of Technology, India, an MS in Computer Engineering from Iowa State University and an MBA from the University of Texas at Austin.

Appendix A.

A.1 Electrical Schematic

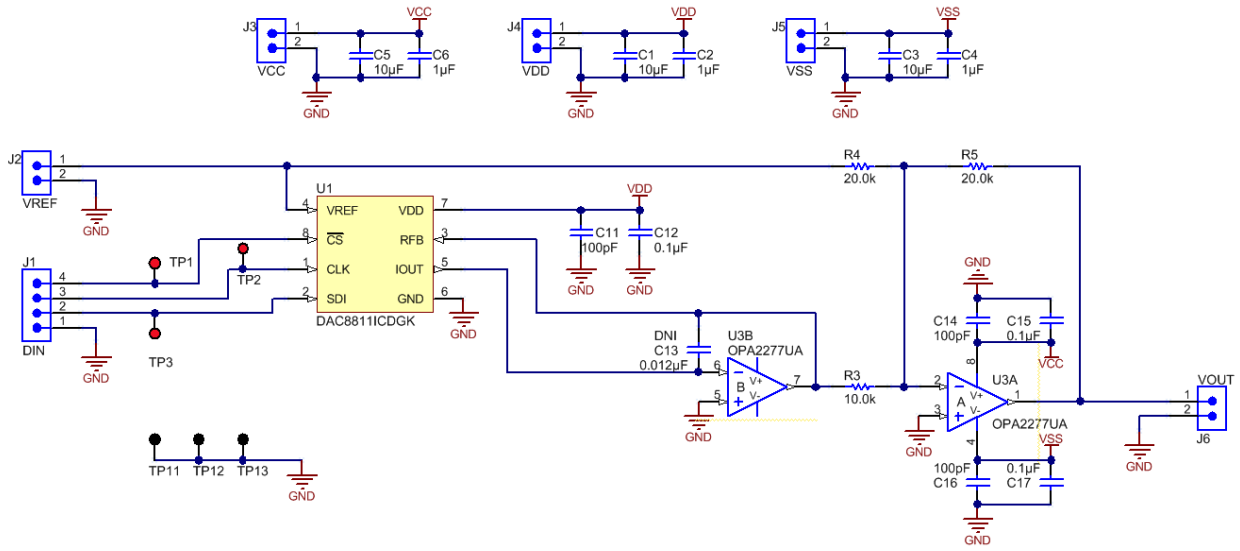


Figure A-1: Electrical Schematic

Passive Name in Text	Passive Name in Schematic
R_{G1}	R3
R_{G2}	R4
R_{FB2}	R5
C_{COMP}	C13

A.2 Bill of Materials

TEXAS INSTRUMENTS

Bill of Materials

TI DESIGNS

TIPD137: ±10V 4-Quadrant Multiplying DAC

Item #	Quantity	Designator	Value	Description	Manufacturer	PartNumber
1	3	C1, C3, C5	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1206	MuRata	GRM31CR61E106KA12L
2	3	C2, C4, C6	1uF	CAP, CERM, 1uF, 25V, +/-10%, X7R, 1206	AVX	12063C105KAT2A
3	3	C11, C14, C16	100pF	CAP, CERM, 100pF, 25V, +/-10%, X7R, 0603	AVX	06033C101KAT2A
4	3	C12, C15, C17	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	Kemet	C0603C104K3RACTU
5	1	C13	0.012uF	CAP, CERM, 0.012uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E123KA01D
7	1	J1		Header, TH, 100mil, 4x1, Gold plated, 230 mil above insulator	Samtec	TSW-104-07-G-S
8	5	J2, J3, J4, J5, J6		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology, Inc.	ED555/2DS
9	1	R3	10.0kΩ	RES 10K OHM 1/8W .1% 0805 SMD	Panasonic	ERA-6AEB103V
10	2	R4, R5	20.0kΩ	RES 20K OHM 1/8W .1% 0805 SMD	Panasonic	ERA-6AEB203V
11	3	TP1, TP2, TP3		Test Point, Multipurpose, Red, TH	Keystone	5010
12	3	TP11, TP12, TP13		Test Point, Multipurpose, Black, TH	Keystone	5011
13	1	U1		16-Bit, Serial Input Multiplying Digital-to-Analog Converter, DGK0008A	Texas Instruments	DAC8811ICDGK
14	1	U3		High Precision OPERATIONAL AMPLIFIER, D0008A	Texas Instruments	OPA2277UA

Figure A-2: Bill of Materials

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