300V, Dual P-Channel Enhancement-Mode Lateral MOSFET

Features

- 300V breakdown voltage
- Integrated gate-to-source resistor
- Integrated gate-to-source Zener diode
- Low input capacitance
- Fast switching speeds
- Free from secondary breakdown

Applications

- High voltage level translators
- Current sources
- High side switches
- Discrete Amplifier

General Description

The LP1030D is a dual high voltage P-channel enhancement-mode (normally-off) lateral MOSFET. Each MOSFET has integrated gate-to-source resistor and gate-to-source Zener diode. This allows the device to be easily driven with a capacitively coupled gate drive circuit.

The LP1030D utilizes an advanced lateral MOSFET structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices.

Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Ordering Information

Part Number	Package Option	Packing
LP1030DK1-G	5-Lead SOT-23	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Product Summary

BV_{DSS} (V)	$R_{DS(ON)}$ (typ Ω)	$V_{GS(th)}$ (max V)	$I_{D(ON)}$ (min mA)
-300	180	-2.4	-50

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-Source voltage	-16V to +1.0V
Operating temperature range	-25°C to 125°C

Absolute Maximum Ratings are those values beyond which damage to the device can occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration

5-Lead SOT-23
(*Top View*)

Typical Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	253°C/W

Note:
Thermal testboard per JEDEC JESD51-7

Package Marking

W = Code for Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or ⏚

5-Lead SOT-23

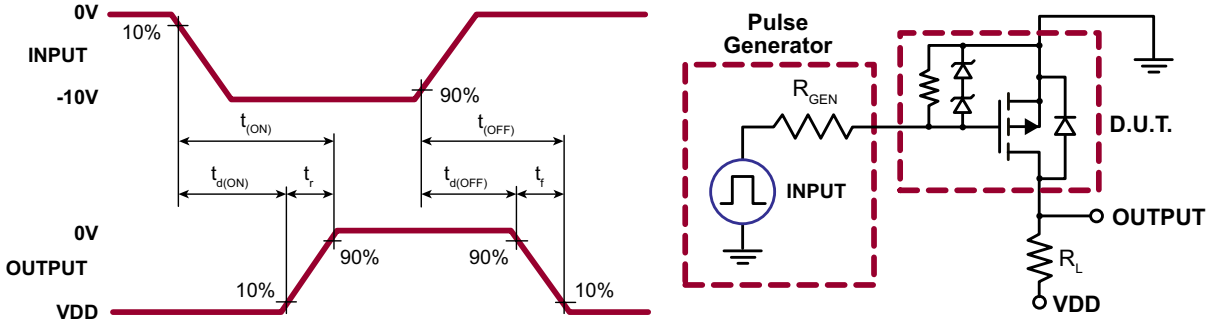
P-Channel Electrical Characteristics *(T_j = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-300	-	-	V	V_{GS} = 0V, I_D = -2.0mA
$V_{GS(th)}$	Gate threshold voltage	-1.4	-1.7	-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	5.0	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
R_{GS}	Gate-to-source shunt resistor	15	-	45	kΩ	I_{GS} = -100µA
V_Z	Gate-to-source Zener voltage	16	-	-	V	I_{GS} = -1.0mA
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{GS} = 0V, V_{DS} = Max rating
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-50	-	-	mA	V_{GS} = -7.0V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	180	-	Ω	V_{GS} = -7.0V, I_D = -20mA
C_{ISS}	Input capacitance	-	10.8	-	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	4.2	-		
C_{RSS}	Reverse transfer capacitance	-	3.1	-		
$t_{d(ON)}$	Turn-on delay time	-	1.0	-	ns	V_{DD} = -25V, I_D = -50mA, R_{GEN} = 25Ω
t_r	Rise time	-	11.5	-		
$t_{d(OFF)}$	Turn-off delay time	-	3.8	-		
t_f	Fall time	-	16	-		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	V_{GS} = 0V, I_{SD} = -25mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = -25mA

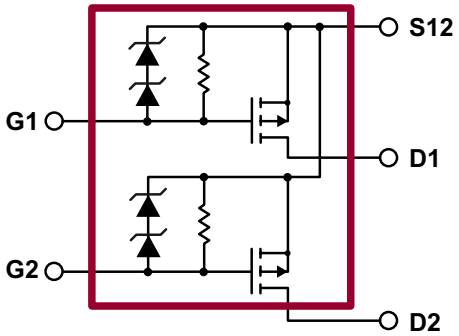
Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

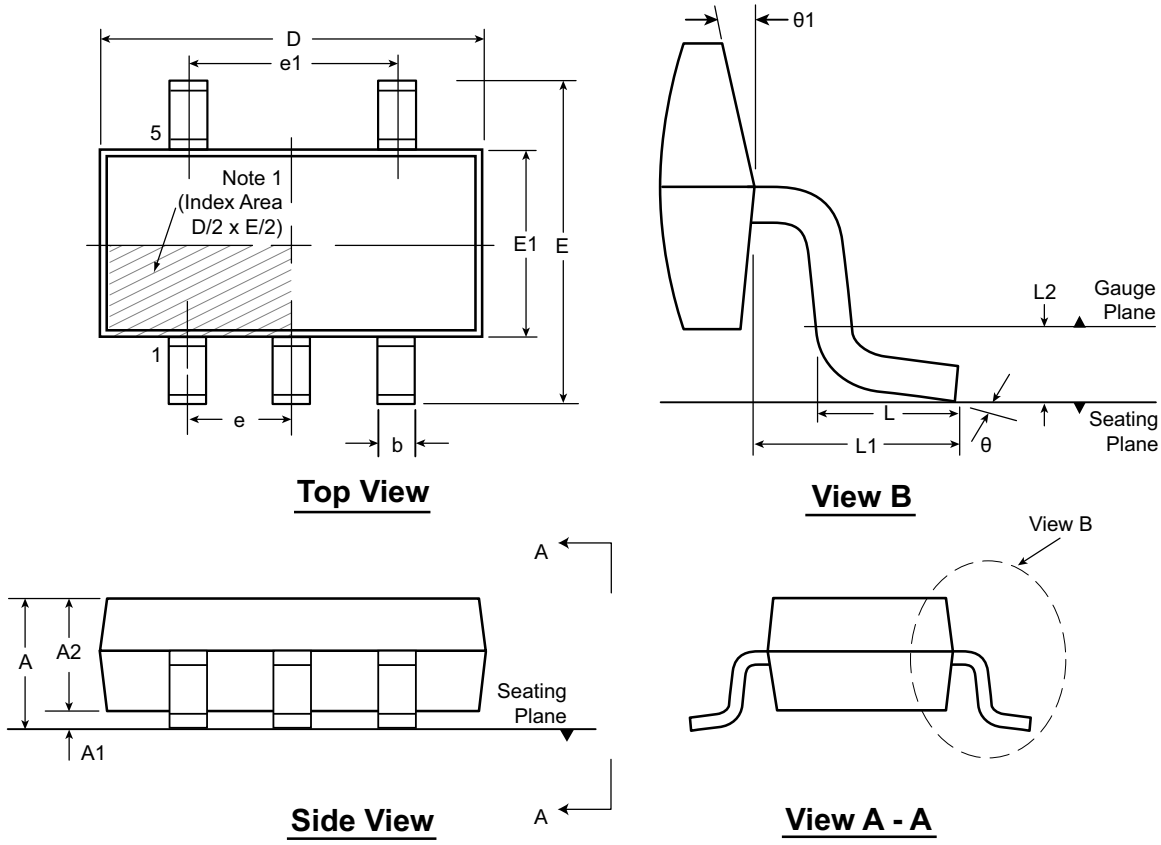


Block Diagram



5-Lead SOT-23 Package Outline (K1)

2.90x1.60mm body, 1.45mm height (max), 0.95mm pitch



Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.90*	0.00	0.90	0.30	2.75*	2.60*	1.45*	0.95 BSC	1.90 BSC	0.30	0.60 REF	0.25 BSC	0°	5°
	NOM	-	-	1.15	-	2.90	2.80	1.60			0.45			4°	10°
	MAX	1.45	0.15	1.30	0.50	3.05*	3.00*	1.75*			0.60			8°	15°

JEDEC Registration MO-178, Variation AA, Issue C, Feb. 2000.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-5SOT23K1, Version A041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com