NLAST4053

Analog Multiplexer/ Demultiplexer

TTL Compatible, Triple 2:1 Analog Switch–Multiplexer Improved Process, Sub–Micron Silicon Gate CMOS

The NLAST4053 is an improved version of the MC14053 and MC74HC4053 fabricated in sub–micron Silicon Gate CMOS technology for lower $R_{DS(on)}$ resistance and improved linearity with low current. This device may be operated either with a single supply or dual supply up to ±3 V to pass a 6 V_{PP} signal without coupling capacitors.

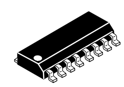
When operating in single supply mode, it is only necessary to tie V_{EE}, pin 7 to ground. For dual supply operation, V_{EE} is tied to a negative voltage, not to exceed maximum ratings. Translation is provided in the device, the Address and Inhibit pins are standard TTL level compatible. For CMOS compatibility see NLAS4053. Pin for pin compatible with all industry standard versions of ‘4053.’

- Improved $R_{DS(on)}$ Specifications
- Pin for Pin Replacement for MAX4053 and MAX4053A
  – One Half the Resistance Operating at 5.0 Volts
- Single or Dual Supply Operation
  – Single 3–5 Volt Operation, or Dual ±3 Volt Operation
  – With V_{CC} of 3.0 to 3.3 V, Device Can Interface with 1.8 V Logic, No Translators Needed
  – Address and Inhibit Pins are Over–Voltage Tolerant and May Be Driven Up +6 V Regardless of V_{CC}
- Address and Inhibit Pins are Standard TTL Compatible
  – Greatly Improved Noise Margin Over MAX4053 and MAX4053A
  – True TTL Compatibility V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Improved Linearity Over Standard HC4053 Devices
- Popular SOIC, and Space Saving TSSOP, and QSOP 16 Pin Packages

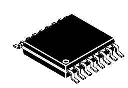
ON Semiconductor®

http://onsemi.com

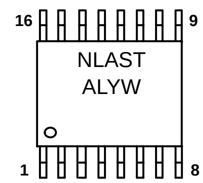
MARKING DIAGRAMS

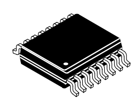


SO–16
D SUFFIX
CASE 751B

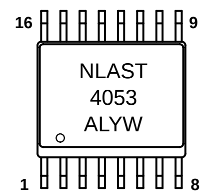


TSSOP–16
DT SUFFIX
CASE 948F





QSOP–16
QS SUFFIX
CASE 492



A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
NLAST4053D	SO–16	48 Units/Rail
NLAST4053DR2	SO–16	2500 Units/Reel
NLAST4053DT	TSSOP–16	96 Units/Rail
NLAST4053DTR2	TSSOP–16	2500 Units/Reel
NLAST4053QS	QSOP–16	98 Units/Rail
NLAST4053QSR	QSOP–16	2500 Units/Reel

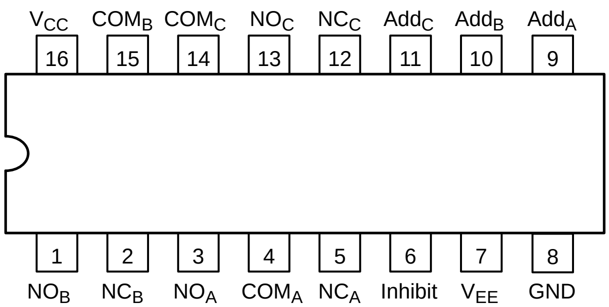


Figure 1. Pin Connection
(Top View)

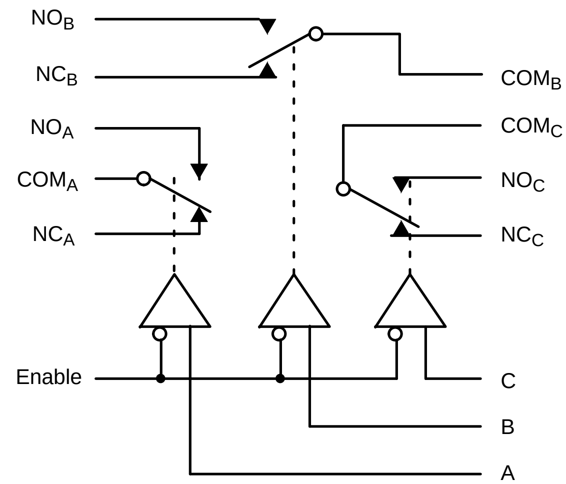


Figure 2. Logic Diagram

TRUTH TABLE

Inhibit	Address			ON SWITCHES*
	C	B	A	
1	X don’t care	X don’t care	X don’t care	All switches open
0	0	0	0	COM_A–NC_A, COM_B–NC_B, COM_C–NC_C
0	0	0	1	COM_A–NO_A, COM_B–NC_B, COM_C–NC_C
0	0	1	0	COM_A–NC_A, COM_B–NO_B, COM_C–NC_C
0	0	1	1	COM_A–NO_A, COM_B–NO_B, COM_C–NC_C
0	1	0	0	COM_A–NC_A, COM_B–NC_B, COM_C–NO_C
0	1	0	1	COM_A–NO_A, COM_B–NC_B, COM_C–NO_C
0	1	1	0	COM_A–NC_A, COM_B–NO_B, COM_C–NO_C
0	1	1	1	COM_A–NO_A, COM_B–NO_B, COM_C–NO_C

*NO, NC, and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{EE}	Negative DC Supply Voltage	(Referenced to GND)	–7.0 to +0.5	V
V_{CC}	Positive DC Supply Voltage (Note 2)	(Referenced to GND) (Referenced to V_{EE})	–0.5 to +7.0 –0.5 to +7.0	V
V_{IS}	Analog Input Voltage		V_{EE} –0.5 to V_{CC} +0.5	V
V_{IN}	Digital Input Voltage	(Referenced to GND)	–0.5 to 7.0	V
I	DC Current, Into or Out of Any Pin		±50	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOIC TSSOP QSOP	143 164 164	°C/W
P_D	Power Dissipation in Still Air,	SOIC TSSOP QSOP	500 450 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 >1000	V
$I_{LATCH–UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 6)	±300	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied.
2. The absolute value of $V_{CC} \pm |V_{EE}| \leq 7.0$.
3. Tested to EIA/JESD22–A114–A.
4. Tested to EIA/JESD22–A115–A.
5. Tested to JESD22–C101–A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{EE}	Negative DC Supply Voltage	(Referenced to GND)	–5.5	GND	V
V_{CC}	Positive DC Supply Voltage	(Referenced to GND) (Referenced to V_{EE})	2.5 2.5	5.5 6.6	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{IN}	Digital Input Voltage	(Note 7) (Referenced to GND)	0	5.5	V
T_A	Operating Temperature Range, All Package Types		–55	125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 3.0 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

7. Unused digital inputs may not be left open. All digital inputs must be tied to a high–logic voltage level or a low–logic input voltage level.

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Address and Inhibit Inputs		3.0 4.5 5.5	1.6 2.0 2.0	1.6 2.0 2.0	1.6 2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage, Address and Inhibit Inputs		3.0 4.5 5.5	0.5 0.8 0.8	0.5 0.8 0.8	0.5 0.8 0.8	V
I_{IN}	Maximum Input Leakage Current, Address and Inhibit Inputs	V_{IN} = 6.0 or GND	0 V to 6.0 V	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Address and Inhibit, and $V_{IS} = V_{CC}$ or GND	6.0	4.0	40	80	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					–55 to 25°C	≤85°C	≤125°C	
R_{ON}	Maximum "ON" Resistance	$V_{IN} = V_{IL}$ or $V_{IH,}$ $V_{IS} = V_{EE}$ to V_{CC} $\|I_S\|$ = 10 mA (Figures 4 thru 9)	3.0 4.5 3.0	0 0 –3.0	86 37 26	108 46 33	120 55 37	Ω
ΔR_{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{IN} = V_{IL}$ or $V_{IH,}$ V_{IS} = 2.0 V V_{IS} = 3.0 V $\|I_S\|$ = 10 mA, V_{IS} = 2.0 V	3.0 4.5 3.0	0 0 –3.0	15 2.0 10	20 2.0 15	20 2.0 15	Ω
$R_{flat(ON)}$	COM–NO On–Resistance Flatness	V_{com} = 1, 2, 3.5 V V_{com} = –2, 0, 2 V	4.5 3.0	0 –3.0	24 2.0	24 2.0	35 3.0	Ω
$I_{NC(OFF)}$ $I_{NO(OFF)}$	Maximum Off–Channel Leakage Current	Switch Off $V_{IN} = V_{IL}$ or V_{IH} $V_{IO} = V_{CC}$ –1.0 V or V_{EE} +1.0 V (Figure 17)	6.0 3.0	0 –3.0	0.1 0.1	5.0 5.0	100 100	nA
$I_{COM(ON)}$	Maximum On–Channel Leakage Current, Channel–to–Channel	Switch On $V_{IO} = V_{CC}$ –1.0 V or V_{EE} +1.0 V (Figure 17)	6.0 3.0	0 –3.0	0.1 0.1	5.0 5.0	100 100	nA

AC CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit –55 to 25°C Min	Guaranteed Limit –55 to 25°C Typ*	≤85°C	≤125°C	Unit
t_{BBM}	Minimum Break–Before–Make Time	$V_{IN} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ R_L = 300 Ω, C_L = 35 pF (Figure 19)	3.0 4.5 3.0	0.0 0.0 –3.0	1.0 1.0 1.0	6.5 5.0 3.5	– – –	– – –	ns

*Typical Characteristics are at 25°C.

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f = 3$ ns)

Symbol	Parameter	V_{CC} V	V_{EE} V	–55 to 25°C Min	–55 to 25°C Typ	–55 to 25°C Max	≤85°C Min	≤85°C Max	≤125°C Min	≤125°C Max	Unit
t_{TRANS}	Transition Time (Address Selection Time) (Figure 18)	2.5 3.0 4.5 3.0	0 0 0 –3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns
t_{ON}	Turn–on Time (Figures 14, 15, 20, and 21) Enable to N_O or N_C	2.5 3.0 4.5 3.0	0 0 0 –3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns
t_{OFF}	Turn–off Time (Figures 14, 15, 20, and 21) Enable to N_O or N_C	2.5 3.0 4.5 3.0	0 0 0 –3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{IN}	Maximum Input Capacitance,Select Inputs	8	pF
C_{NO} or C_{NC}	Analog I/O	10	
C_{COM}	Common I/O	10	
$C_{(ON)}$	Feedthrough	1.0	

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Typ 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response	V_{IS} = ½ (V_{CC} – V_{EE}) Source Amplitude = 0 dBm (Figures 10 and 22)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 –3.0	145 165 180 180	MHz
V_{ISO}	Off–Channel Feedthrough Isolation	f = 100 kHz; V_{IS} = ½ (V_{CC} – V_{EE}) Source = 0 dBm (Figures 12 and 22)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 –3.0	–93 –93 –93 –93	dB
V_{ONL}	Maximum Feedthrough On Loss	V_{IS} = ½ (V_{CC} – V_{EE}) Source = 0 dBm (Figures 10 and 22)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 –3.0	–2 –2 –2 –2	dB
Q	Charge Injection	V_{IN} = V_{CC} to $V_{EE,}$ f_{IS} = 1 kHz, t_r = t_f = 3 ns R_{IS} = 0 Ω, C_L= 1000 pF, Q = C_L * ΔV_{OUT} (Figures 16 and 23)	5.0 3.0	0.0 –3.0	9.0 12	pC
THD	Total Harmonic Distortion THD + Noise	f_{IS} = 1 MHz, R_L = 10 KΩ, C_L = 50 pF, V_{IS} = 5.0 V_{PP} sine wave V_{IS} = 6.0 V_{PP} sine wave (Figure 13)	 6.0 3.0	 0.0 –3.0	 0.10 0.05	%

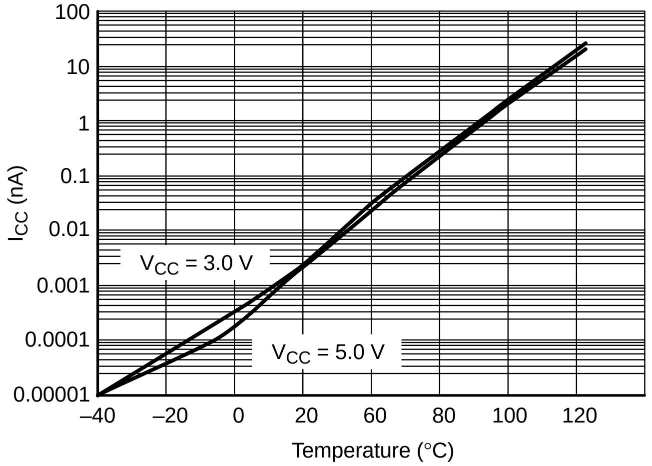


Figure 3. I_{CC} versus Temp, V_{CC} = 3 V and 5 V

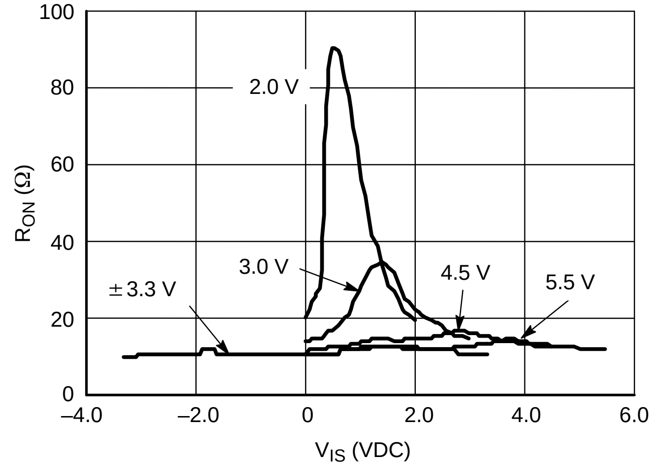


Figure 4. R_{ON} versus V_{CC}, Temp = 25°C

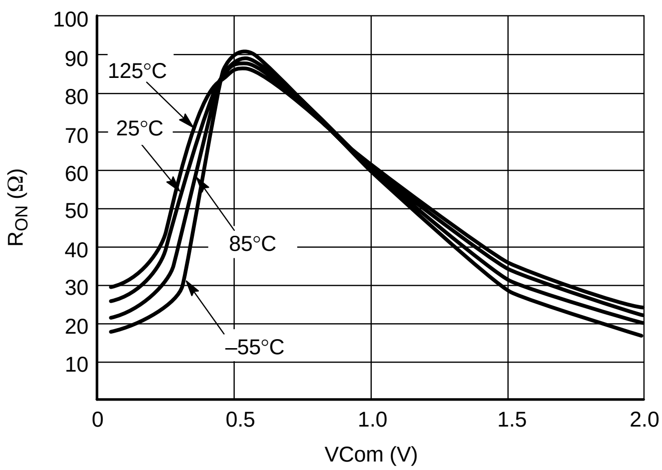


Figure 5. Typical On Resistance
V_{CC} = 2.0 V, V_{EE} = 0 V

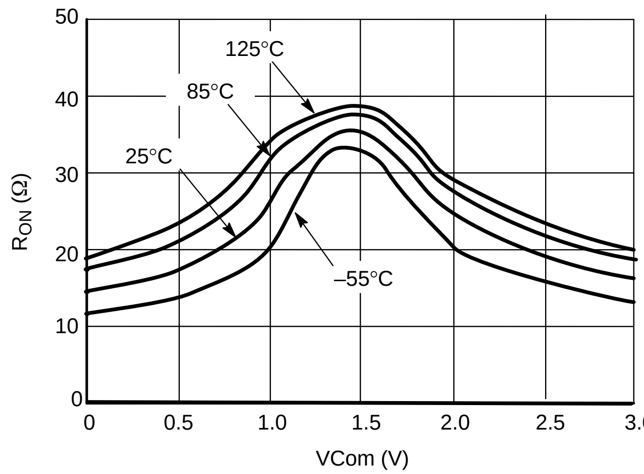


Figure 6. Typical On Resistance
V_{CC} = 3.0 V, V_{EE} = 0 V

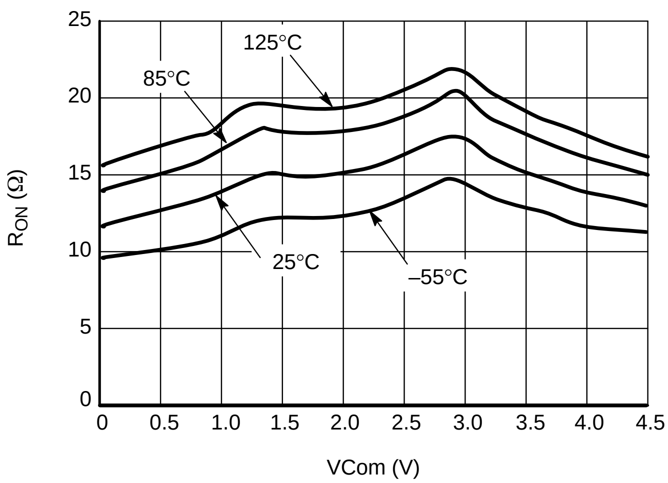


Figure 7. Typical On Resistance
V_{CC} = 4.5 V, V_{EE} = 0 V

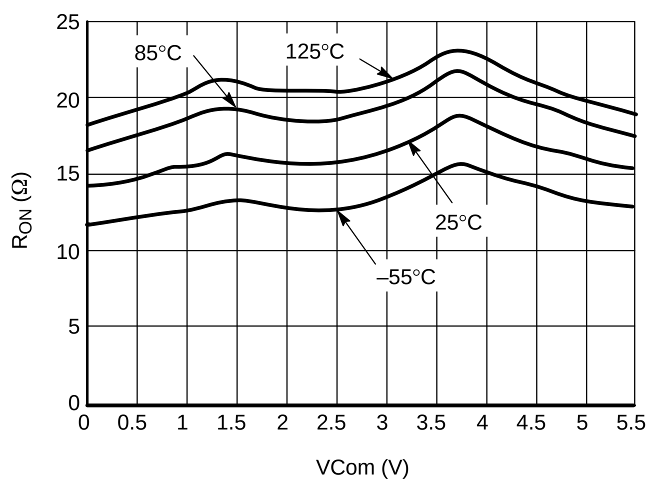


Figure 8. Typical On Resistance
V_{CC} = 5.5 V, V_{EE} = 0 V

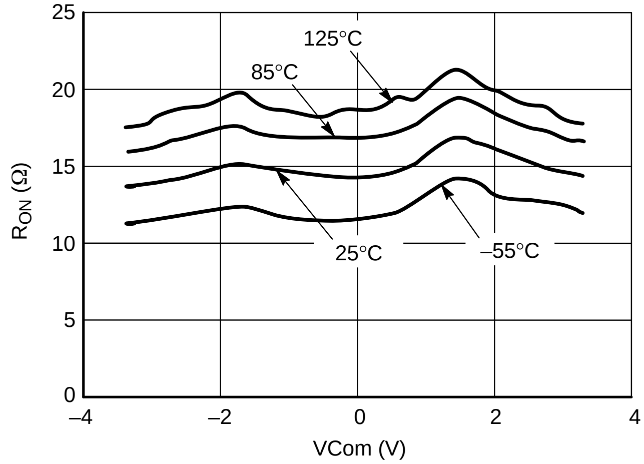


Figure 9. Typical On Resistance
V_{CC} = 3.0 V, V_{EE} = –3.0 V

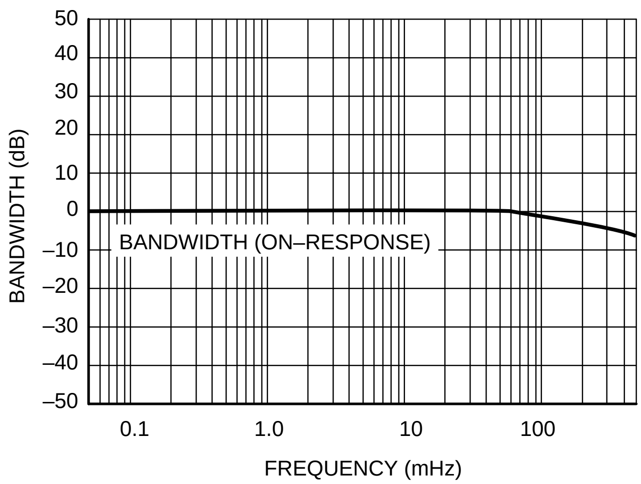


Figure 10. Bandwidth

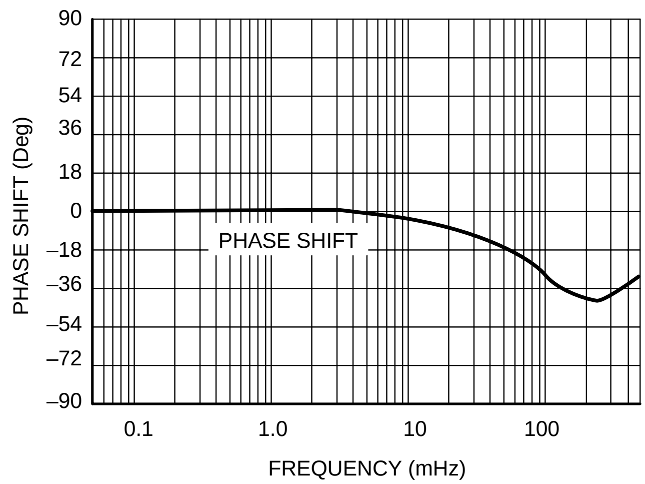


Figure 11. Phase Shift

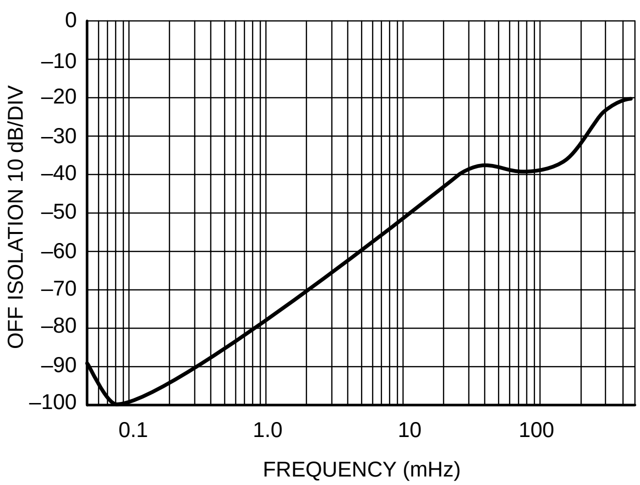


Figure 12. Off Isolation

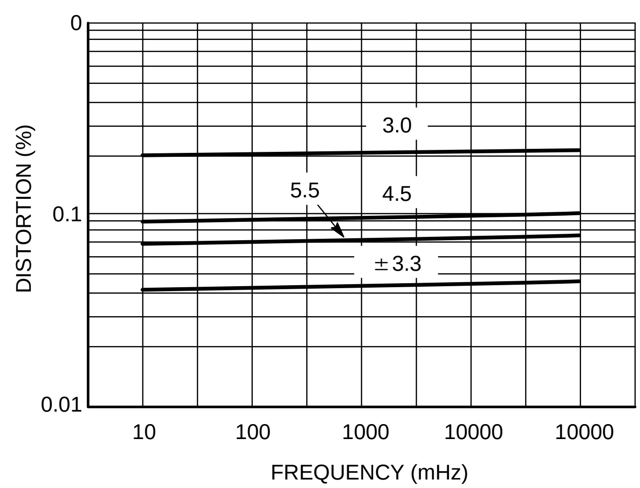


Figure 13. Total Harmonic Distortion

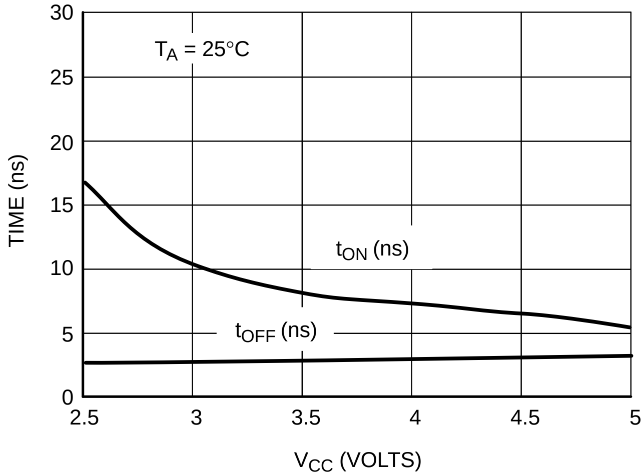


Figure 14. t_{ON} and t_{OFF} versus V_{CC}

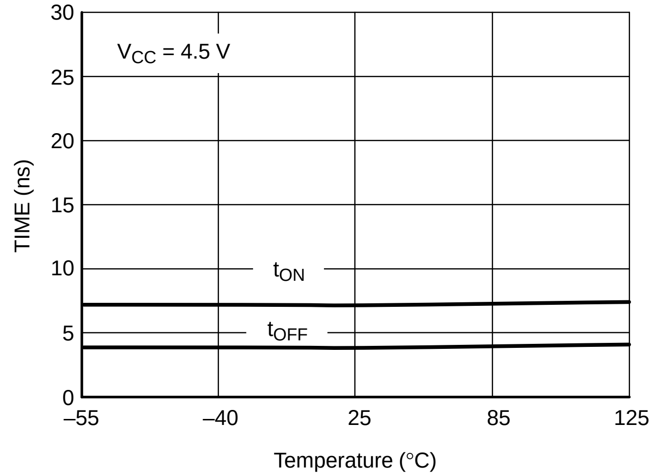


Figure 15. t_{ON} and t_{OFF} versus Temp

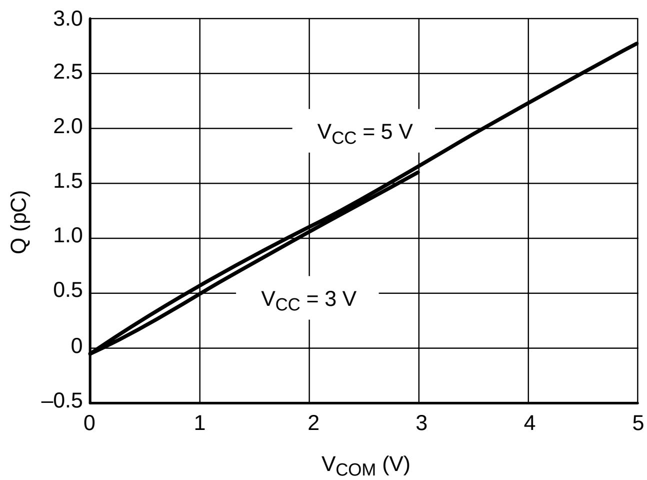


Figure 16. Charge Injection versus COM Voltage

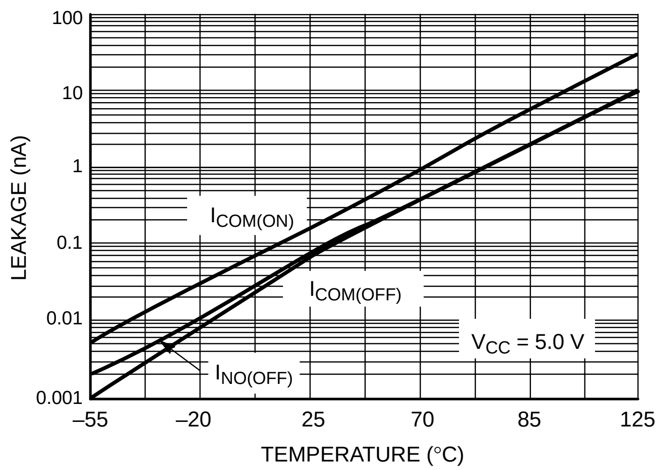


Figure 17. Switch Leakage versus Temperature

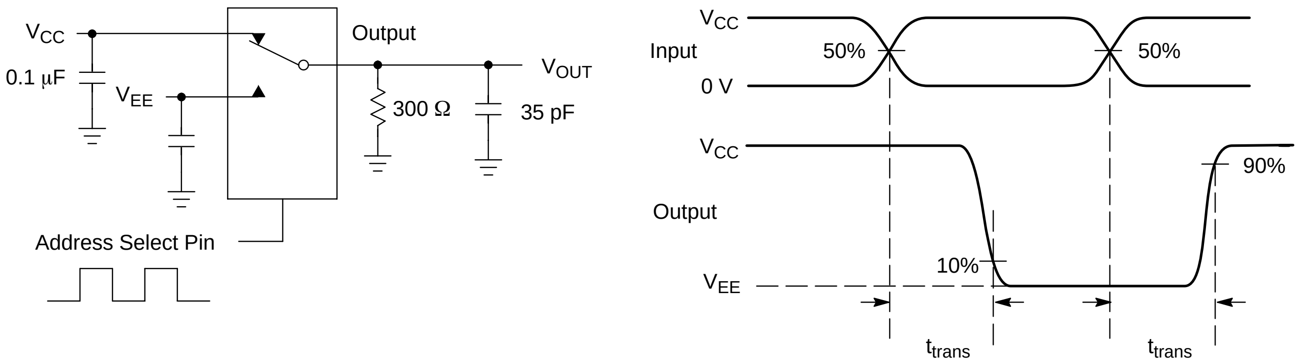


Figure 18. Channel Selection Propagation Delay

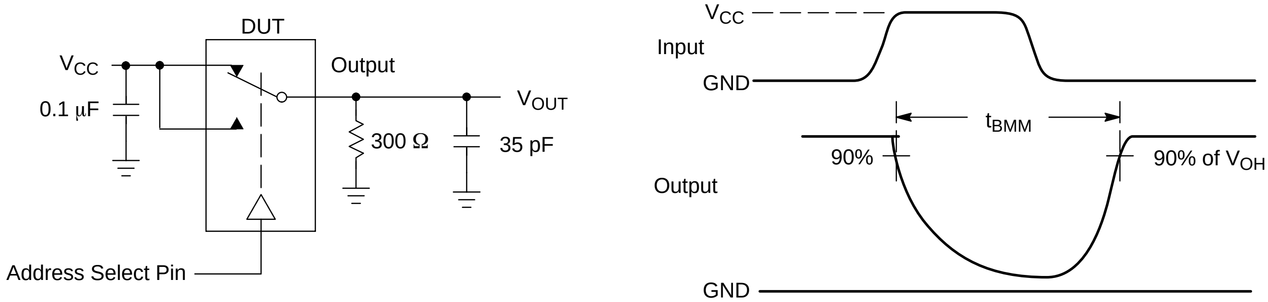


Figure 19. t_{BBM} (Time Break–Before–Make)

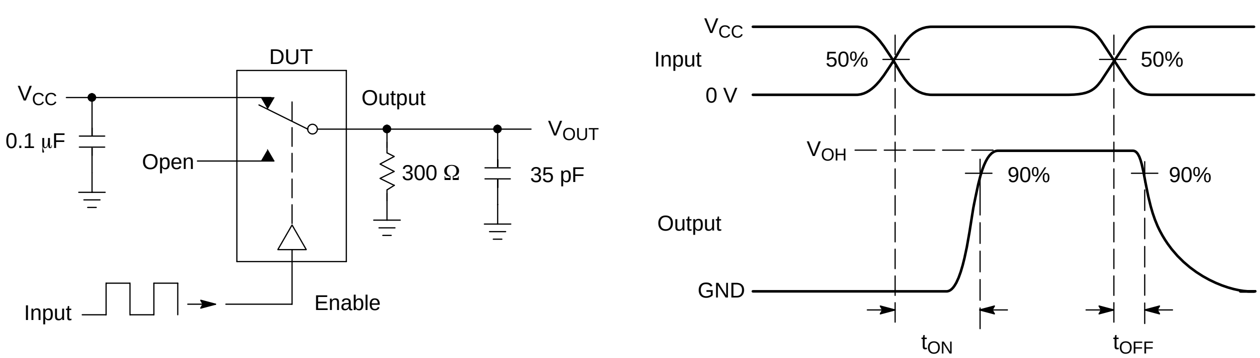


Figure 20. t_{ON}/t_{OFF}

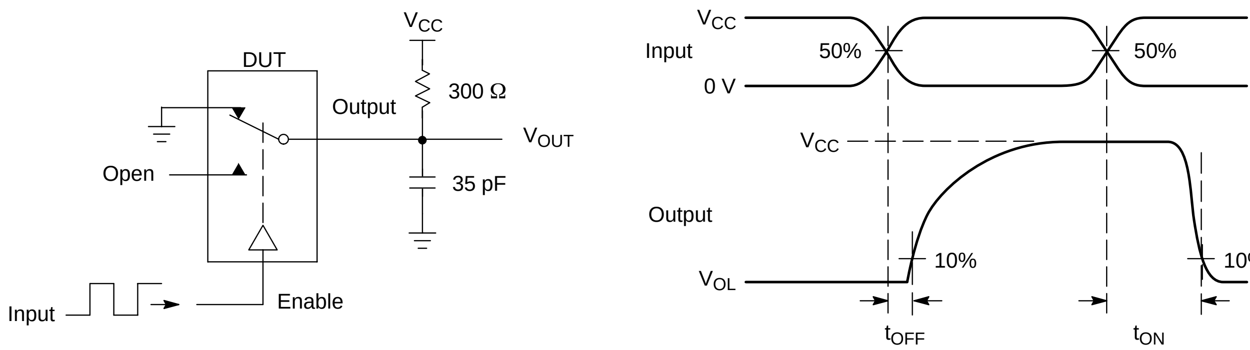
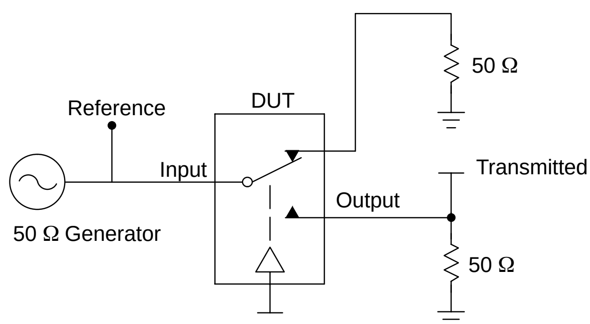


Figure 21. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 22. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

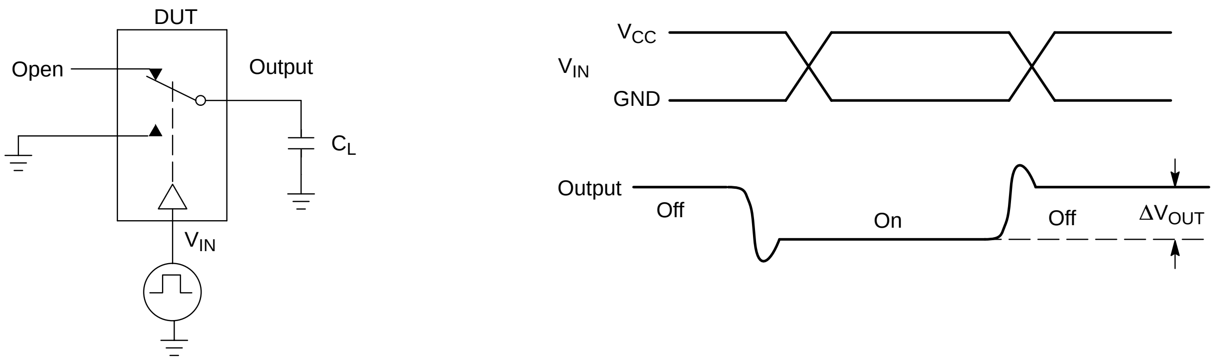


Figure 23. Charge Injection: (Q)

TYPICAL OPERATION

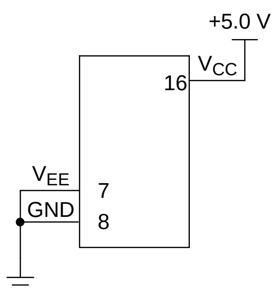


Figure 24. 5.0 Volts Single Supply
V_{CC} = 5.0 V, V_{EE} = 0

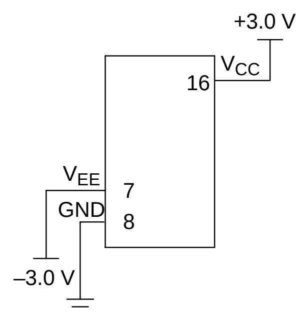
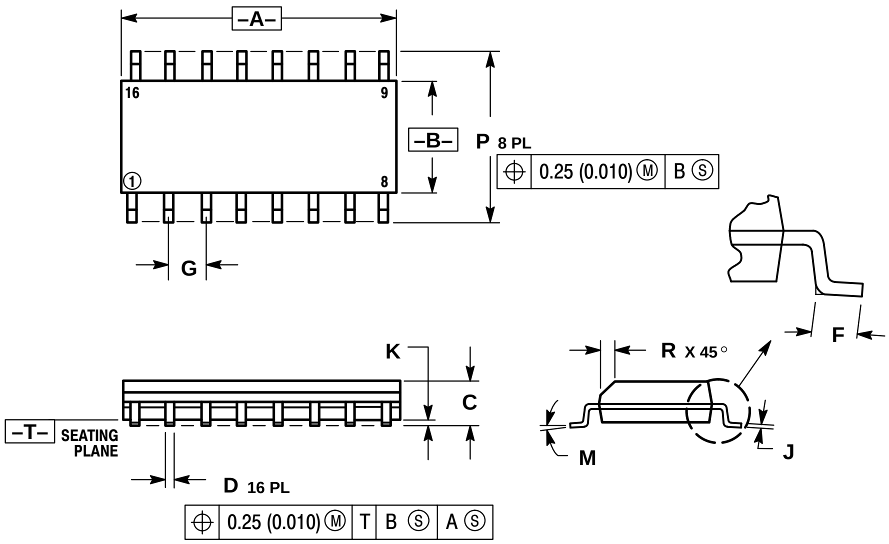


Figure 25. Dual Supply
V_{CC} = 3.0 V, V_{EE} = –3.0 V

PACKAGE DIMENSIONS

SOIC–16
D SUFFIX
CASE 751B–05
ISSUE J

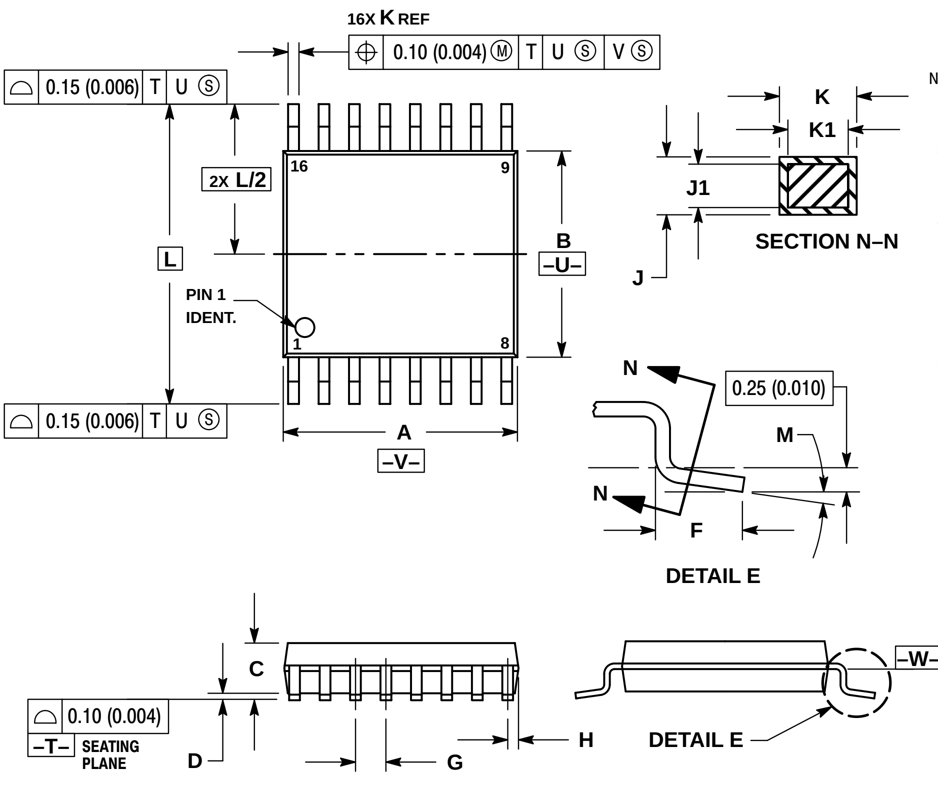


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP–16
DT SUFFIX
CASE 948F–01
ISSUE O

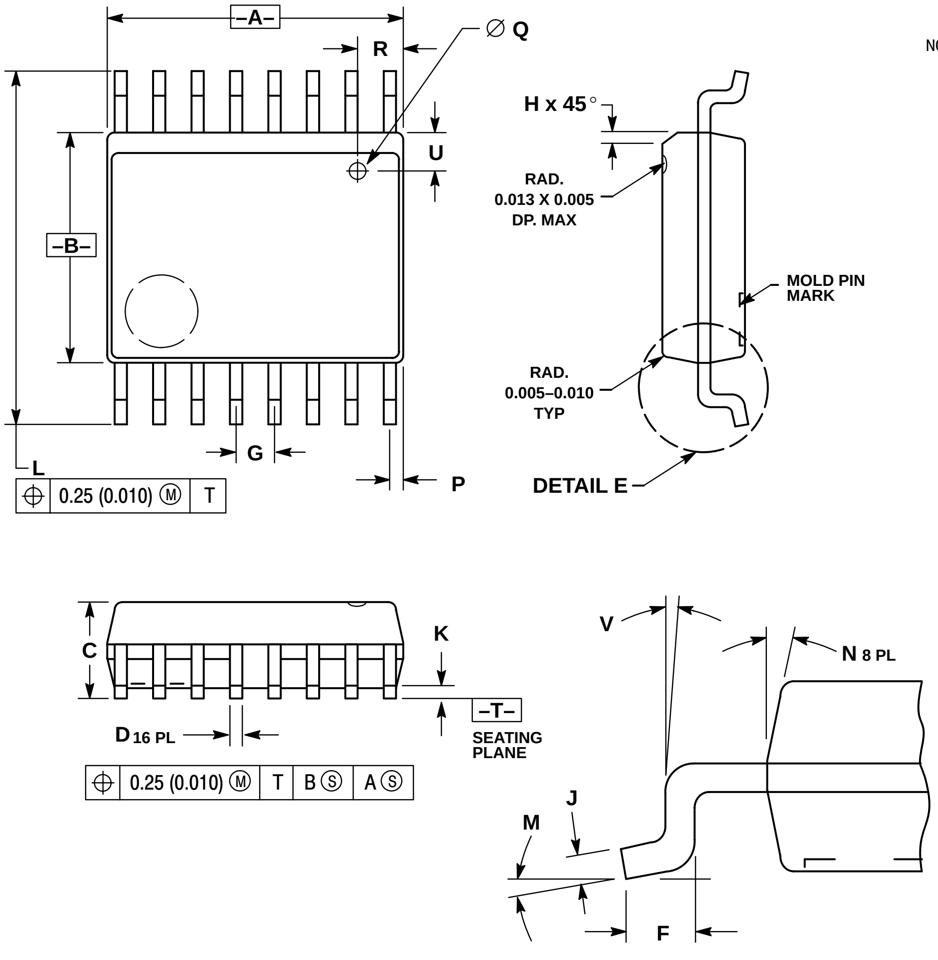


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

QSOP–16
M SUFFIX
CASE 492–01
ISSUE O



DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.189	0.196	4.80	4.98
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.007	0.011	0.18	0.28
Q	0.020 DIA		0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
V	0°	8°	0°	8°

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