

## Features

- Temperature ranges
  - Automotive -A: -40 °C to 85 °C
  - Automotive-E: -40 °C to 125 °C
- High speed
  - $t_{AA} = 10$  ns
- Low active power
  - 360 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features

## Functional Description

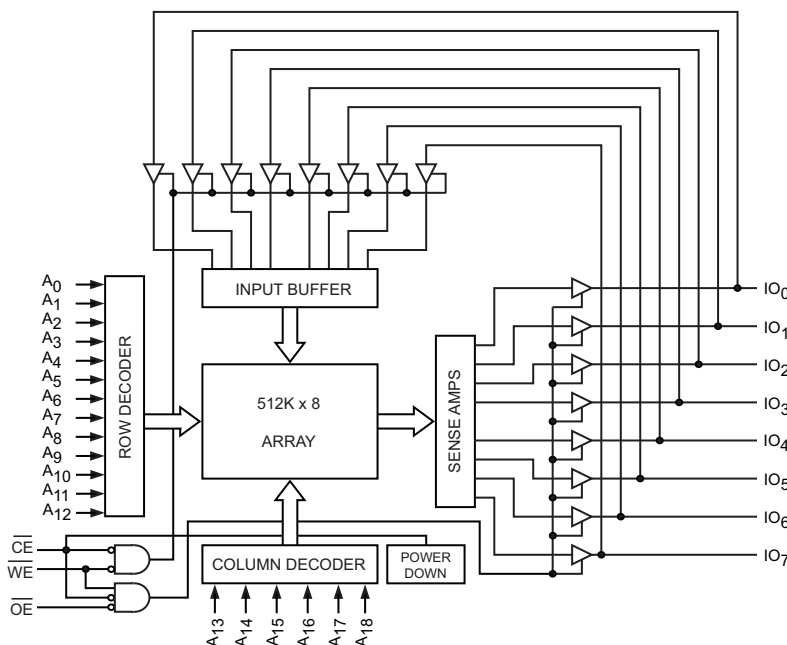
The CY7C1049CV33 Automotive is a high performance CMOS Static RAM organized as 524,288 words by eight bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1049CV33 Automotive is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



## Contents

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Selection Guide

| Description                  |              | -10 | -12 | -15 | Unit |
|------------------------------|--------------|-----|-----|-----|------|
| Maximum Access Time          |              | 10  | 12  | 15  | ns   |
| Maximum Operating Current    | Automotive-A | 100 | 95  | –   | mA   |
|                              | Automotive-E | –   | –   | 95  | mA   |
| Maximum CMOS Standby Current | Automotive-A | 10  | 10  | –   | mA   |
|                              | Automotive-E | –   | –   | 15  | mA   |

Pin Configuration

Figure 1. 36-pin SOJ pinout (Top View)

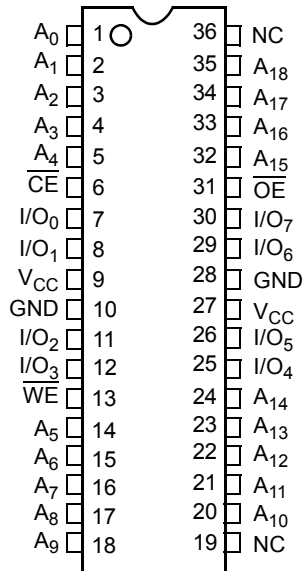
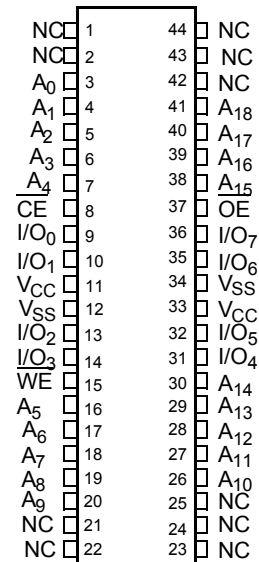


Figure 2. 44-pin TSOP II pinout (Top View)



Pin Definitions

| Pin Name                           | 36-pin SOJ Pin Number        | 44-pin TSOP II Pin Number            | I/O Type      | Description  |
|------------------------------------|------------------------------|--------------------------------------|---------------|--|
| A <sub>0</sub> –A <sub>18</sub>    | 1–5, 14–18, 20–24, 32–35     | 3–7, 16–20, 26–30, 38–41             | Input         | <b>Address inputs used to select one of the address locations.</b>   |
| I/O <sub>0</sub> –I/O <sub>7</sub> | 7, 8, 11, 12, 25, 26, 29, 30 | 9, 10, 13, 14, 31, 32, 35, 36        | Input/Output  | <b>Bidirectional data I/O lines.</b> Used as input or output lines depending on operation.   |
| NC <sup>[1]</sup>                  | 19, 36                       | 1, 2, 21, 22, 23, 24, 25, 42, 43, 44 | No Connect    | <b>No connects.</b> This pin is not connected to the die.  |
| $\overline{WE}$                    | 13                           | 15                                   | Input/Control | <b>Write Enable input, active LOW.</b> When selected LOW, a WRITE is conducted.  |
| $\overline{CE}$                    | 6                            | 8                                    | Input/Control | <b>Chip Enable input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.   |
| $\overline{OE}$                    | 31                           | 37                                   | Input/Control | <b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-state, and act as input data pins. |
| V <sub>SS</sub> , GND              | 10, 28                       | 12, 34                               | Ground        | <b>Ground for the device.</b> Should be connected to ground of the system.   |
| V <sub>CC</sub>                    | 9, 27                        | 11, 33                               | Power Supply  | <b>Power supply inputs to the device.</b>  |

Note  
1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C  
 Ambient Temperature with Power Applied ..... -55 °C to +125 °C  
 Supply Voltage on V<sub>CC</sub> to Relative GND [2] ..... -0.5 V to +4.6 VDC  
 Voltage Applied to Outputs in High Z State [2] ..... -0.5 V to V<sub>CC</sub> + 0.5 V

Input Voltage [2] ..... -0.5 V to V<sub>CC</sub> + 0.5 V  
 Current into Outputs (LOW) ..... 20 mA  
 Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V  
 Latch up current ..... > 200 mA

## Operating Range

| Range        | Ambient Temperature | V <sub>CC</sub> |
|--------------|---------------------|-----------------|
| Automotive-A | -40 °C to +85 °C    | 3.3 V ± 0.3 V   |
| Automotive-E | -40 °C to +125 °C   |                 |

## Electrical Characteristics

Over the Operating Range

| Parameter        | Description                                   | Test Conditions   | -10    |                       | -12  |                       | -15  |                       | Unit |    |
|------------------|---|---|--------|-----------------------|------|-----------------------|------|-----------------------|------|----|
|                  |   |   | Min    | Max                   | Min  | Max                   | Min  | Max                   |      |    |
| V <sub>OH</sub>  | Output HIGH Voltage                           | V <sub>CC</sub> = Min; I <sub>OH</sub> = -4.0 mA  | 2.4    | -                     | 2.4  | -                     | 2.4  | -                     | V    |    |
| V <sub>OL</sub>  | Output LOW Voltage                            | V <sub>CC</sub> = Min; I <sub>OL</sub> = 8.0 mA   | -      | 0.4                   | -    | 0.4                   | -    | 0.4                   | V    |    |
| V <sub>IH</sub>  | Input HIGH Voltage                            |   | 2.0    | V <sub>CC</sub> + 0.3 | 2.0  | V <sub>CC</sub> + 0.3 | 2.0  | V <sub>CC</sub> + 0.3 | V    |    |
| V <sub>IL</sub>  | Input LOW Voltage [2]                         |   | -0.3   | 0.8                   | -0.3 | 0.8                   | -0.3 | 0.8                   | V    |    |
| I <sub>IX</sub>  | Input Load Current                            | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | Auto-A | -1                    | +1   | -1                    | +1   | -                     | -    | μA |
|                  |   |   | Auto-E | -                     | -    | -                     | -    | -20                   | +20  |    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>   | Auto-A | -                     | 100  | -                     | 95   | -                     | -    | mA |
|                  |   |   | Auto-E | -                     | -    | -                     | -    | -                     | 95   |    |
| I <sub>SB1</sub> | Automatic CE Power Down Current - TTL Inputs  | Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> ; V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> | Auto-A | -                     | 40   | -                     | 40   | -                     | -    | mA |
|                  |   |   | Auto-E | -                     | -    | -                     | -    | -                     | 45   |    |
| I <sub>SB2</sub> | Automatic CE Power Down Current - CMOS Inputs | Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0           | Auto-A | -                     | 10   | -                     | 10   | -                     | -    | mA |
|                  |   |   | Auto-E | -                     | -    | -                     | -    | -                     | 15   |    |

**Note**

2. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.5 V for pulse durations of less than 20 ns.

### Capacitance

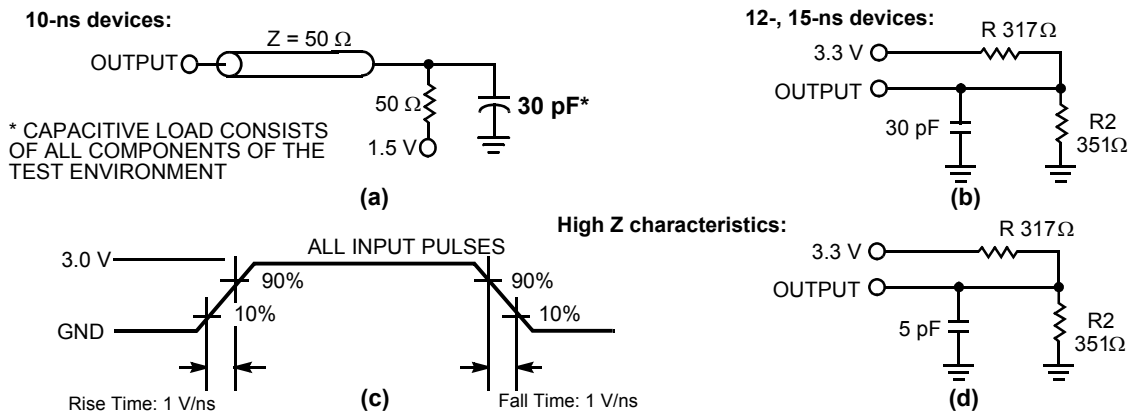
| Parameter [3]    | Description        | Test Conditions  | Max | Unit |
|------------------|--------------------|--|-----|------|
| C <sub>IN</sub>  | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V | 8   | pF   |
| C <sub>OUT</sub> | Output capacitance |  | 8   | pF   |

### Thermal Resistance

| Parameter [3]   | Description                              | Test Conditions  | 36-pin SOJ | 44-pin TSOP II | Unit |
|-----------------|--|--|------------|----------------|------|
| Θ <sub>JA</sub> | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | 46.51      | 41.66          | °C/W |
| Θ <sub>JC</sub> | Thermal resistance (junction to case)    |  | 18.8       | 10.56          | °C/W |

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [4]



**Notes**

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) for 10 ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

## AC Switching Characteristics

Over the Operating Range

| Parameter <sup>[5]</sup>              | Description                                      | -10 |     | -12 |     | -15 |     | Unit    |
|---------------------------------------|--|-----|-----|-----|-----|-----|-----|---------|
|                                       |  | Min | Max | Min | Max | Min | Max |         |
| <b>Read Cycle</b>                     |  |     |     |     |     |     |     |         |
| $t_{power}^{[6]}$                     | $V_{CC}$ (typical) to the first access           | 100 | –   | 100 | –   | 100 | –   | $\mu$ s |
| $t_{RC}$                              | Read Cycle Time                                  | 10  | –   | 12  | –   | 15  | –   | ns      |
| $t_{AA}$                              | Address to Data Valid                            | –   | 10  | –   | 12  | –   | 15  | ns      |
| $t_{OHA}$                             | Data Hold from Address Change                    | 3   | –   | 3   | –   | –   | 3   | ns      |
| $t_{ACE}$                             | $\overline{CE}$ LOW to Data Valid                | –   | 10  | –   | 12  | –   | 15  | ns      |
| $t_{DOE}$                             | $\overline{OE}$ LOW to Data Valid                | –   | 5   | –   | 6   | –   | 7   | ns      |
| $t_{LZOE}$                            | $\overline{OE}$ LOW to Low Z <sup>[7]</sup>      | 0   | –   | 0   | –   | 0   | –   | ns      |
| $t_{HZOE}$                            | $\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup> | –   | 5   | –   | 6   | –   | 7   | ns      |
| $t_{LZCE}$                            | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>      | 3   | –   | 3   | –   | 3   | –   | ns      |
| $t_{HZCE}$                            | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> | –   | 5   | –   | 6   | –   | 7   | ns      |
| $t_{PU}$                              | $\overline{CE}$ LOW to Power Up                  | 0   | –   | 0   | –   | 0   | –   | ns      |
| $t_{PD}$                              | $\overline{CE}$ HIGH to Power Down               | –   | 10  | –   | 12  | –   | 15  | ns      |
| <b>Write Cycle <sup>[9, 10]</sup></b> |  |     |     |     |     |     |     |         |
| $t_{WC}$                              | Write Cycle Time                                 | 10  | –   | 12  | –   | 15  | –   | ns      |
| $t_{SCE}$                             | $\overline{CE}$ LOW to Write End                 | 7   | –   | 8   | –   | 10  | –   | ns      |
| $t_{AW}$                              | Address Setup to Write End                       | 7   | –   | 8   | –   | 10  | –   | ns      |
| $t_{HA}$                              | Address Hold from Write End                      | 0   | –   | 0   | –   | 0   | –   | ns      |
| $t_{SA}$                              | Address Setup to Write Start                     | 0   | –   | 0   | –   | 0   | –   | ns      |
| $t_{PWE}$                             | $\overline{WE}$ Pulse Width                      | 7   | –   | 8   | –   | 10  | –   | ns      |
| $t_{SD}$                              | Data Setup to Write End                          | 5   | –   | 6   | –   | 7   | –   | ns      |
| $t_{HD}$                              | Data Hold from Write End                         | 0   | –   | 0   | –   | 0   | –   | ns      |
| $t_{LZWE}$                            | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup>     | 3   | –   | 3   | –   | 3   | –   | ns      |
| $t_{HZWE}$                            | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  | –   | 5   | –   | 6   | –   | 7   | ns      |

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at stable, typical  $V_{CC}$  values until the first memory access can be performed.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of [Figure 3 on page 5](#). Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

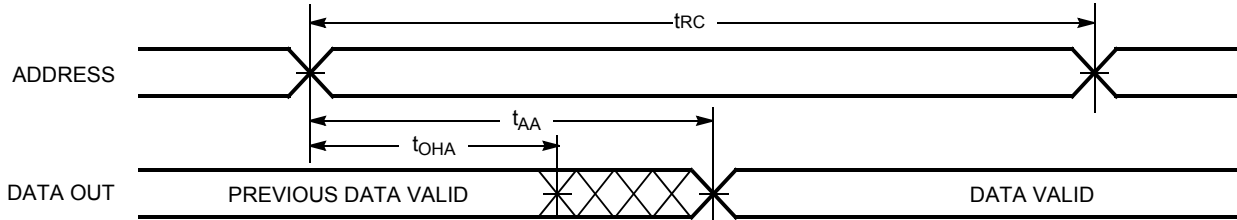


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [12, 13]

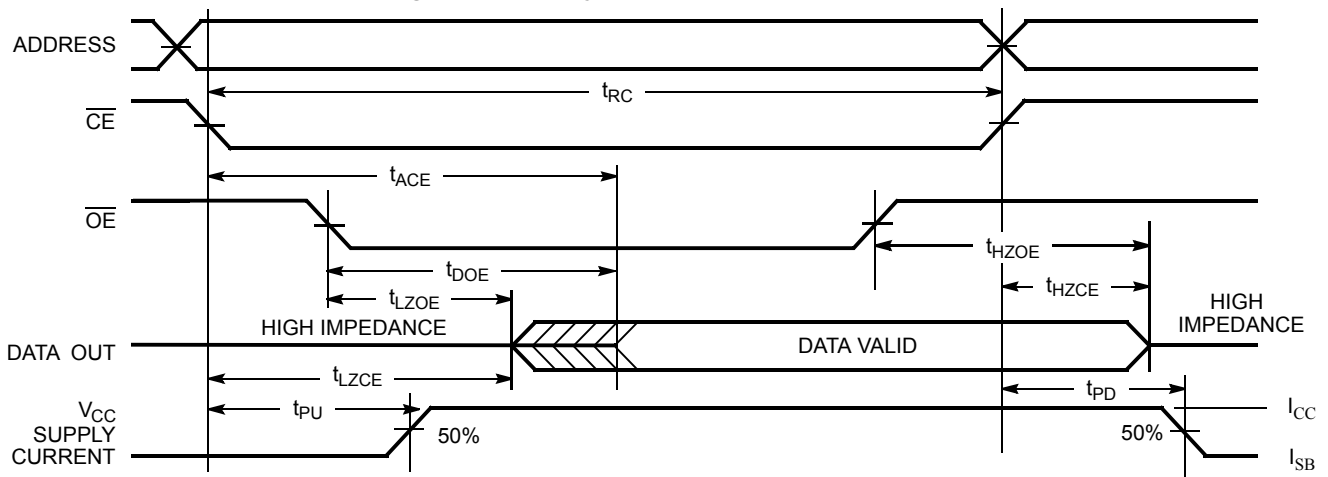
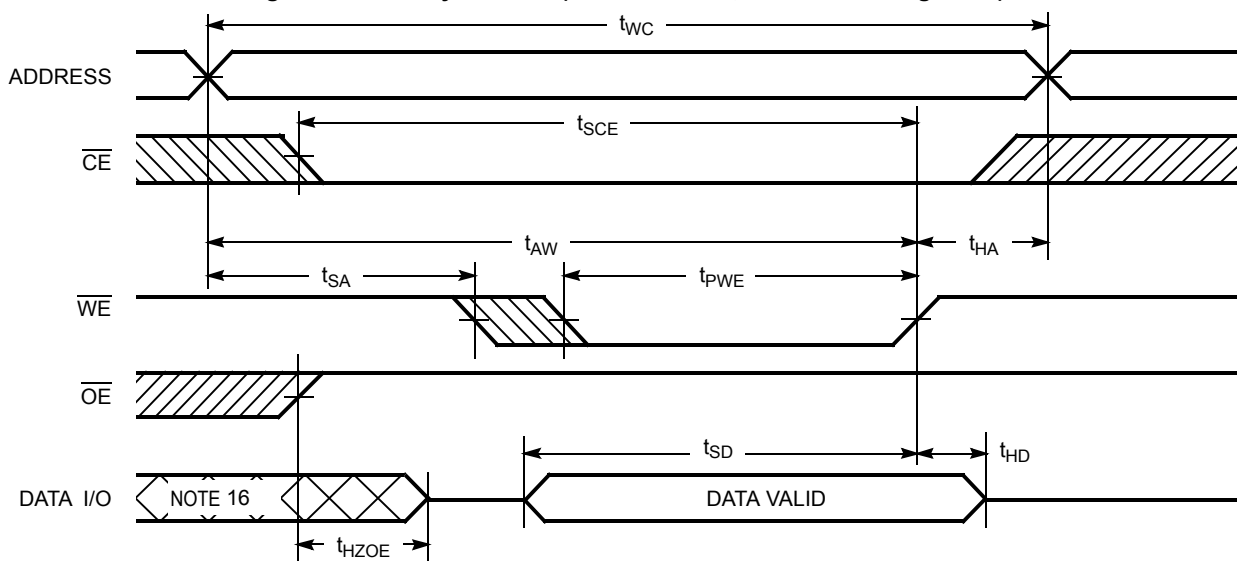


Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write) [14, 15]

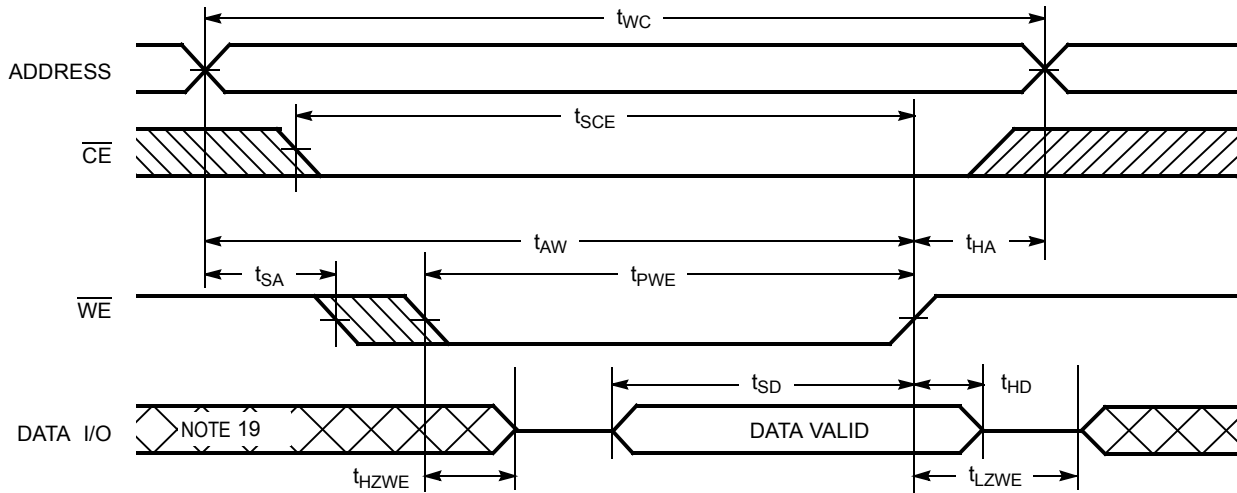


Notes

- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- 12.  $\overline{WE}$  is HIGH for read cycles.
- 13. Address valid before or similar to  $\overline{CE}$  transition LOW.
- 14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 16. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [17, 18]



Notes

- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 18. The minimum Write cycle time for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 19. During this period, the I/Os are in output state. Do not apply input signals.



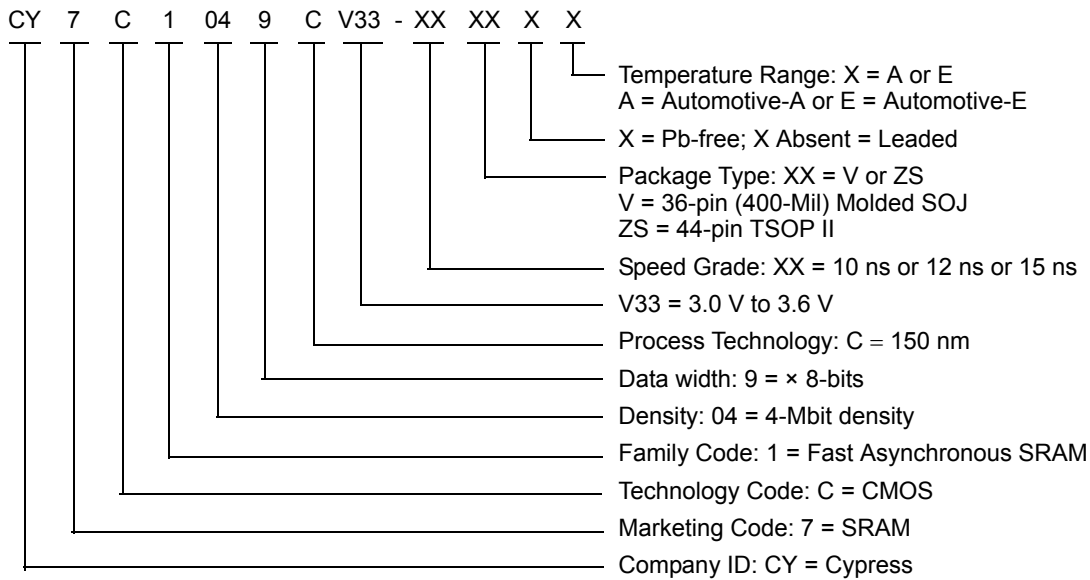
**Truth Table**

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O <sub>0</sub> -I/O <sub>7</sub> | Mode                       | Power                      |
|-----------------|-----------------|-----------------|------------------------------------|----------------------------|----------------------------|
| H               | X               | X               | High Z                             | Power Down                 | Standby (I <sub>SB</sub> ) |
| L               | L               | H               | Data Out                           | Read                       | Active (I <sub>CC</sub> )  |
| L               | X               | L               | Data In                            | Write                      | Active (I <sub>CC</sub> )  |
| L               | H               | H               | High Z                             | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |

**Ordering Information**

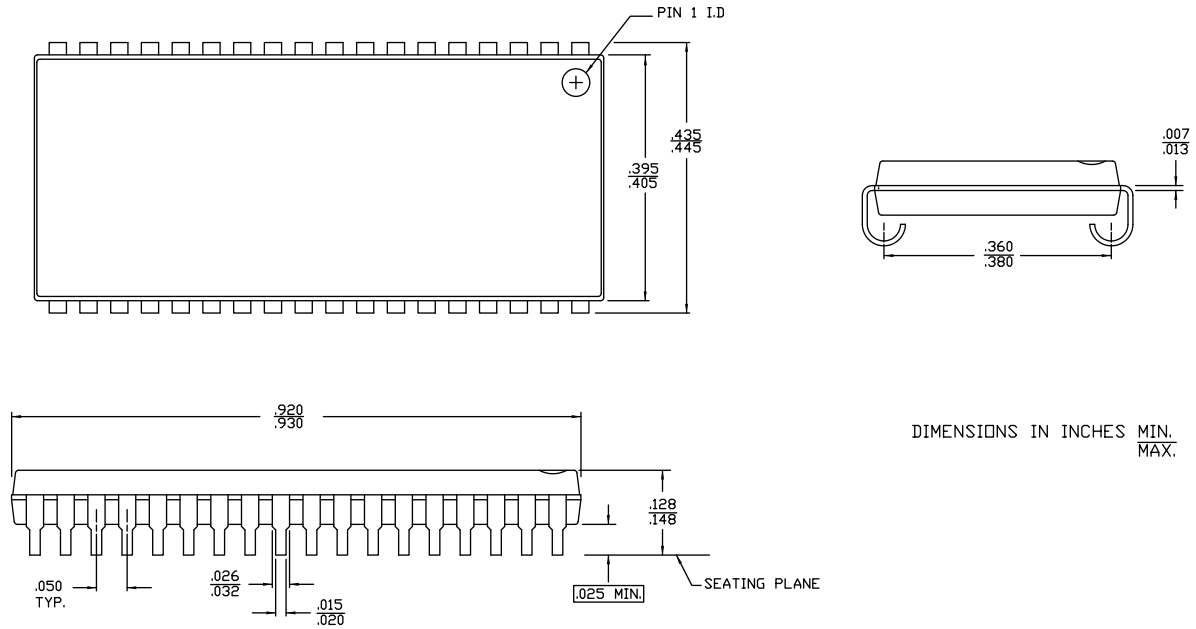
| Speed (ns) | Ordering Code       | Package Diagram | Package Type                          | Operating Range |
|------------|---------------------|-----------------|---------------------------------------|-----------------|
| 10         | CY7C1049CV33-10VXA  | 51-85090        | 36-pin (400-Mil) Molded SOJ (Pb-free) | Automotive-A    |
| 12         | CY7C1049CV33-12ZSXA | 51-85087        | 44-pin TSOP II (Pb-free)              | Automotive-A    |
| 15         | CY7C1049CV33-15VXE  | 51-85090        | 36-pin (400-Mil) Molded SOJ (Pb-free) | Automotive-E    |
|            | CY7C1049CV33-15ZSXE | 51-85087        | 44-pin TSOP II (Pb-free)              | Automotive-E    |

**Ordering Code Definitions**



**Package Diagrams**

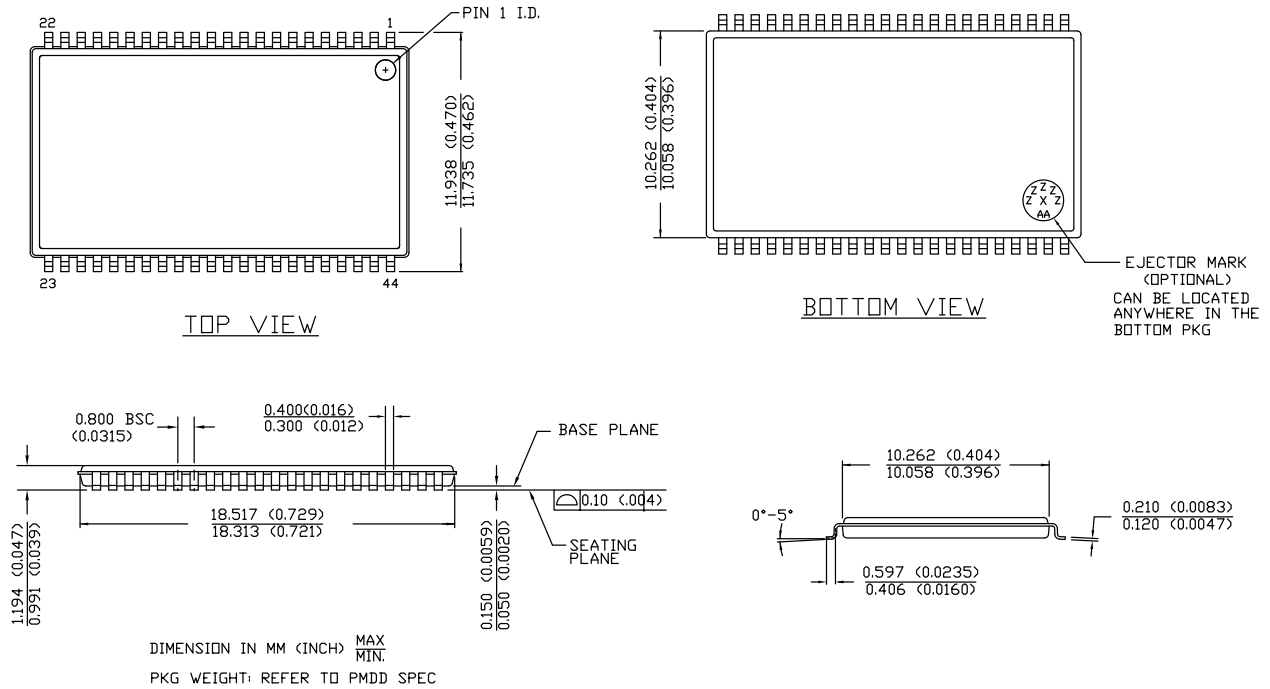
**Figure 8. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090**



51-85090 \*F

Package Diagrams (continued)

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E

## Acronyms

| Acronym         | Description                             |
|-----------------|---|
| $\overline{CE}$ | Chip Enable                             |
| CMOS            | Complementary Metal Oxide Semiconductor |
| I/O             | Input/Output                            |
| $\overline{OE}$ | Output Enable                           |
| SOJ             | Small Outline J-lead                    |
| SRAM            | Static Random Access Memory             |
| TSOP            | Thin Small Outline Package              |
| TTL             | Transistor-Transistor Logic             |
| $\overline{WE}$ | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| μs     | microsecond     |
| mA     | milliampere     |
| mm     | millimeter      |
| ms     | millisecond     |
| mW     | milliwatt       |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

**Document History Page**

| Document Title: CY7C1049CV33 Automotive, 4-Mbit (512 K × 8) Static RAM<br>Document Number: 001-67511 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Rev.   | ECN     | Orig. of Change | Submission Date | Description of Change  |
| **   | 3186792 | PRAS            | 03/03/2011      | Separation of the automotive data sheet from CY7C1049CV33 spec no. 38-05006 Rev. *J. Further rev of 38-05006 would include only industrial / commercial parts.   |
| *A   | 3265070 | PRAS            | 05/24/2011      | Updated <a href="#">Functional Description</a> (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”).<br>Updated in new template.   |
| *B   | 3546915 | NILE            | 03/09/2012      | Updated <a href="#">Pin Definitions</a> (Updated description of $\overline{WE}$ and $\overline{OE}$ pins).<br>Updated <a href="#">Package Diagrams</a> .   |
| *C   | 4311615 | NILE / VINI     | 03/21/2014      | Updated <a href="#">Maximum Ratings</a> :<br>Added “Static discharge voltage” and “Latch up current” details.<br><br>Updated <a href="#">AC Switching Characteristics</a> :<br>Updated Note 10.<br><br>Updated <a href="#">Switching Waveforms</a> :<br>Added Note 18 and referred the same note in <a href="#">Figure 7</a> .<br><br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85087 – Changed revision from *D to *E.<br><br>Updated in new template.<br><br>Completing Sunset Review. |

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