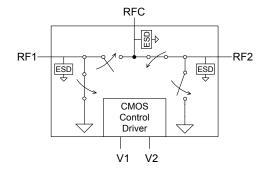


Product Description

The PE4250 is a HaRP™-enhanced Reflective SPDT (single pole double throw) RF Switch for use in general switching applications and mobile infrastructure. This device offers a flexible supply voltage of 3.3/5V, single-pin or complementary pin control inputs, and 4000 V ESD tolerance. It presents a simple alternative solution to pin diode and mechanical relay switches.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram



Product Specification PE4250

SPDT UltraCMOS™ RF Switch 10 - 3000 MHz, Reflective

Features

- HaRP-Technology Enhanced
- Low Insertion Loss: 0.65 dB @ 1000 MHz
- High Isolation: 51 dB @ 1000 MHz
- P1dB typical: +30.5 dBm
- IIP3 typical: +59 dBm
- Fast switching time: 150 ns
- Flexible supply voltage: 3.3 V ±10% or 5.0 V ±10% supply (see table 3)
 - Excellent ESD protection: 4000 V HBM
- No blocking capacitors required
- Single pin or complementary control inputs

Figure 2. Package Type

8-lead MSOP



Table 1. Target Electrical Specifications Temp = 25°C, V_{DD} = 3.3 or 5.0 V

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency ¹		10		3000	MHz
	10 MHz		0.6	0.65	dB
Incombine Long (DE4/DE2)	1000 MHz		0.65	0.70	dB
Insertion Loss (RF1/RF2)	2000 MHz		0.75	0.80	dB
	3000 MHz		0.75	0.90	dB
Isolation (RFC to RF1/RF2)	1000 MHz	50	51		dB
	2000 MHz	46	48		dB
	3000 MHz	35	40		dB
	1000 MHz		25		dB
Return Loss	2000 MHz		23		dB
	3000 MHz		20		dB
Input 1 dB Compression ²	50 - 3000 MHz		30.5		dBm
Input IP3	50 - 3000 MHz, +18 dBm per tone, 5 MHz spacing		59		dBm
Switching Time	50% CTRL to 10/90% RF		150	300	ns

1. Device linearity will begin to degrade below 10 MHz. Notes:

2. Note Absolute Maximum rating of $P_{IN} = 27$ dBm.



Figure 3. Pin Configuration (Top View)

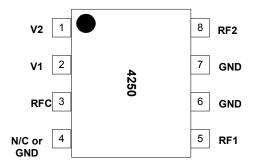


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V2	This pin supports two interface options: Single-pin control mode. A nominal 3-volt or 5-volt supply connection is required. Complementary-pin control mode. A complementary CMOS control signal to V1 is supplied to this pin.
2	V1	Switch control input, CMOS logic level.
3	RFC	RF Common port.3
4	N/C or GND	No Connect or Ground
5	RF1 ³	RF1 port. ³
6	GND	Ground Connection. Traces should be physically short and connected to ground plane for best performance.
7	GND	Ground Connection. Traces should be physically short and connected to ground plane for best performance.
8	RF2 ³	RF2 port. ³

Note 3. All RF pins must be DC blocked with an external series capacitor or held at 0 $V_{\rm DC}$.

Table 3. Operating Ranges

Parameter	Min	Тур	Max	Units
V _{DD} Power Supply Voltage ⁴	3.0 4.5	3.3 5.0	3.6 5.5	> >
$ \begin{aligned} I_{DD} & \text{Power Supply Current} \\ & V_{DD} = V_{CNTL} = 3.3V \\ & V_{DD} = V_{CNTL} = 5.0V \end{aligned} $		55 75	60 80	μ Α μ Α
Control Voltage High	0.8 x V _{DD}			V
Control Voltage Low			0.2 x V _{DD}	V
P _{IN} RF Input Power (50Ω)			27	dBm
T _{OP} Operating temperature range	-40	25	85	°C
T _{ST} Storage temperature range	-65	25	150	°C

Note 4. Customer must choose either 3.3 V or 5.0 V power supply range

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	3	5.5	V
Vı	Voltage on any control input	-0.3	5.5	V
T _{ST}	Storage temperature range	-65	150	°C
P _{IN}	RF Input power (50Ω)		27	dBm
V _{ESD}	ESD voltage (HBM) ⁵ ESD voltage (Machine Model)		4000 250	٧

Note: 5. Human Body Model (HBM, MIL_STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Switching Frequency

The PE4250 has a maximum 25 kHz switching rate.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4250 in the 8-lead MSOP package is MSL1.

Document No. 70-0254-02

UltraCMOS™ RFIC Solutions



Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path	
Pin 1 (V2) = V _{DD} Pin 2 (V1) = High	RFC to RF1	
Pin 1 (V2) = V _{DD} Pin 2 (V1) = Low	RFC to RF2	

Table 6. Complementary-pin Control Logic **Truth Table**

Control Voltages	Signal Path
Pin 1 (V2) = Low Pin 2 (V1) = High	RFC to RF1
Pin 1 (V2) = High Pin 2 (V1) = Low	RFC to RF2

Control Logic Input

The PE4250 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 2) supporting a +3.3 or 5.0-volt CMOS logic input, and requires a dedicated +3.3 or 5.0-volt power supply connection (pin 1). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS µProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins V1 and V2 (pins 2 & 1), that can be directly driven by +3.3 or 5.0-volt CMOS logic or a suitable μProcessor I/O port. This enables the PE4250 to operate in positive control voltage mode within the PE4250 operating limits.



Evaluation Kit

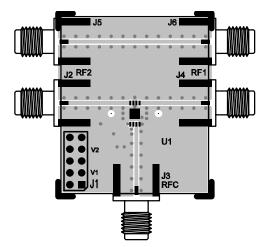
The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4250 SPDT switch. The RF common port is connected through a 50 Ω transmission line to the bottom SMA connector, J3. Port 1 and Port 2 are connected through 50 Ω transmission lines to two SMA connectors on either side of the board, J4 and J2. A through transmission line connects SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.0322". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.033", trace gaps of 0.010", dielectric thickness of 0.028", copper thickness of 0.0021" and ε_r of 4.3.

J1 provides a means for controlling the DC inputs to the device. The second-to-bottom lower right pin (J1-3) is connected to the device V1 input. The second-to-top upper right pin (J1-7) is connected to the device V2 input. Footprints for decoupling capacitors are provided on both V1 and V2 traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 4. Evaluation Board Layouts

Peregrine specification 101/0337



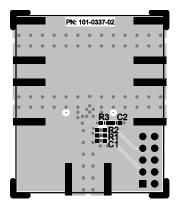
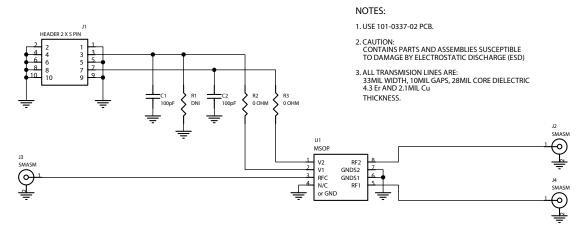
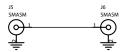


Figure 5. Evaluation Board Schematic Peregrine specification 102/0408





©2008-2009 Peregrine Semiconductor Corp. All rights reserved.

Document No. 70-0254-02

UltraCMOS™ RFIC Solutions



Figure 6. Insertion Loss: RFC-RF @ 25 °C

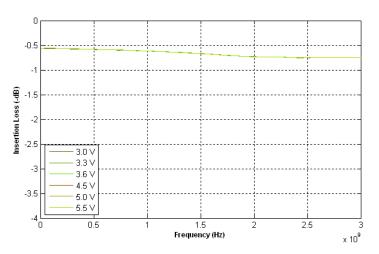


Figure 7. Insertion Loss: RFC-RF @ 3.3 V

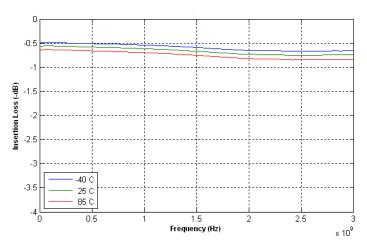


Figure 8. Isolation: RFC-RF @ 25 °C

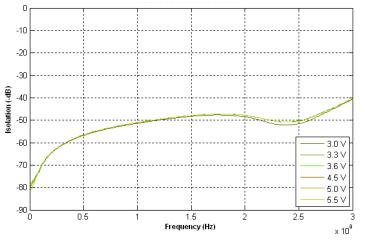


Figure 9. Isolation: RFC-RF @ 3.3 V

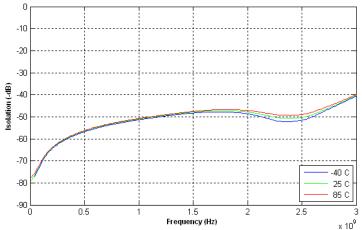


Figure 10. Return Loss at active port @ 25 °C

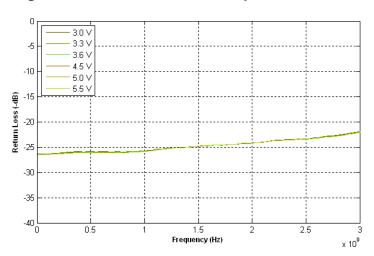


Figure 11. Return Loss at active port @ 3.3 V

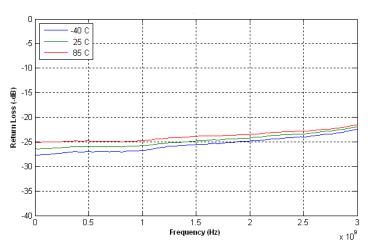
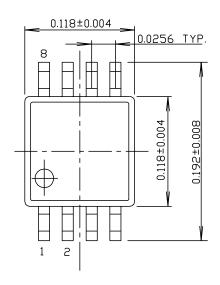
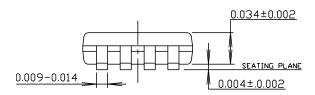




Figure 12. Package Drawing

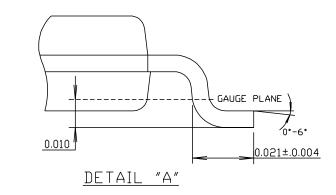
8-lead MSOP: 19-0118-01





NOTE:

- 1) CONTROLLING DIMENSION: INCHES.
- PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR.
- PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTROSIONS.



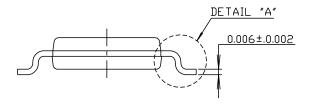
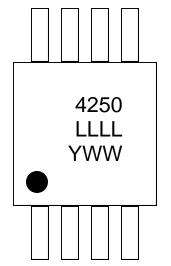


Figure 13. Top Marking Specification



AAAA: Product Number, last 4 digits, Exp.

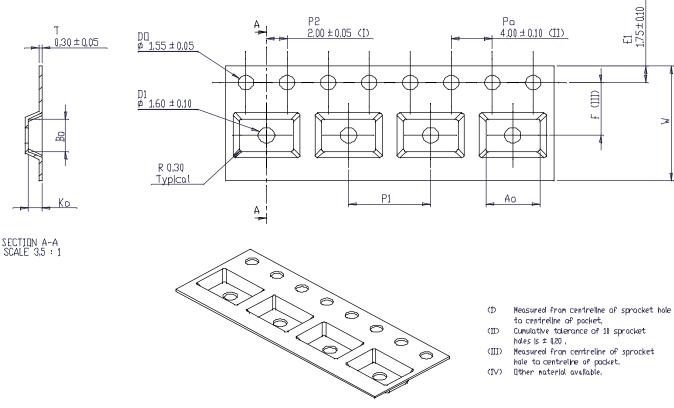
LLLL: Last four digits of the Assembly lot number

YWW: Date Code, last digit of the year and work week



Figure 14. Tape and Reel Specifications

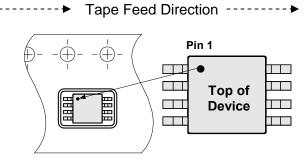
8-lead MSOP



ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

Table 7. Dimensions

Dimension	MSOP-8
Ao	5.30 ± 0.1
Во	3.40 ± 0.1
Ko	1.40 ± 0.1
F	5.50 ± 0.05
P ₁	8 ± 0.1
W	12 ± 0.3



Device Orientation in Tape

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
EK4250-01	PE4250-EK	PE4250-08MSOP-EK	Evaluation Kit	1 / Box
PE4250MLI	4250	PE4250G-08MSOP-cut tape or loose	Green 8-lead MSOP	Cut tape or loose
PE4250MLI-Z	4250	PE4250G-08MSOP-2000C	Green 8-lead MSOP	2000 units / T&R



Sales Offices

The Americas

Peregrine Semiconductor Corporation

9380 Carroll Park Drive San Diego, CA 92121 Tel: 858-731-9400 Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine 13-15 rue des Quatre Vents F-92380 Garches, France Tel: +33-1-4741-9173 Fax: +33-1-4741-9173

High-Reliability and Defense Products

Americas San Diego, CA, USA Phone: 858-731-9475 Fax: 848-731-9499

Europe/Asia-Pacific Aix-En-Provence Cedex 3, France Phone: +33-4-4239-3361

Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)

Shanghai, 200040, P.R. China Tel: +86-21-5836-8276 Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea

#B-2607, Kolon Tripolis, 210 Geumgok-dong, Bundang-gu, Seongnam-si Gyeonggi-do, 463-943 South Korea Tel: +82-31-728-3939

Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan

Teikoku Hotel Tower 10B-6 1-1-1 Uchisaiwai-cho, Chiyoda-ku Tokyo 100-0011 Japan

Tel: +81-3-3502-5211 Fax: +81-3-3502-5213

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS, HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp.

©2008-2009 Peregrine Semiconductor Corp. All rights reserved.