EMC-OPTIMIZED CAN TRANSCEIVER

Check for Samples: SN65HVD1050-Q1

FEATURES

- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Improved Drop-In Replacement for TJA1050
- Meets or Exceeds the Requirements of ISO 11898-2
- GIFT/ICT Compliant
- ESD Protection up to ±8 kV (Human-Body Model) on Bus Pins
- High Electromagnetic Immunity (EMI)
- Low Electromagnetic Emissions (EME)
- Bus-Fault Protection of –27 V to 40 V
- Dominant Time-Out Function
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Bus Inputs and Outputs
  - High Input Impedance With Low V_{CC}
  - Monotonic Outputs During Power Cycling

APPLICATIONS

- GMW3122 Dual-Wire CAN Physical Layer
- SAE J2284 High-Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface
- Industrial Automation
  - DeviceNet™ Data Buses (Vendor ID #806)

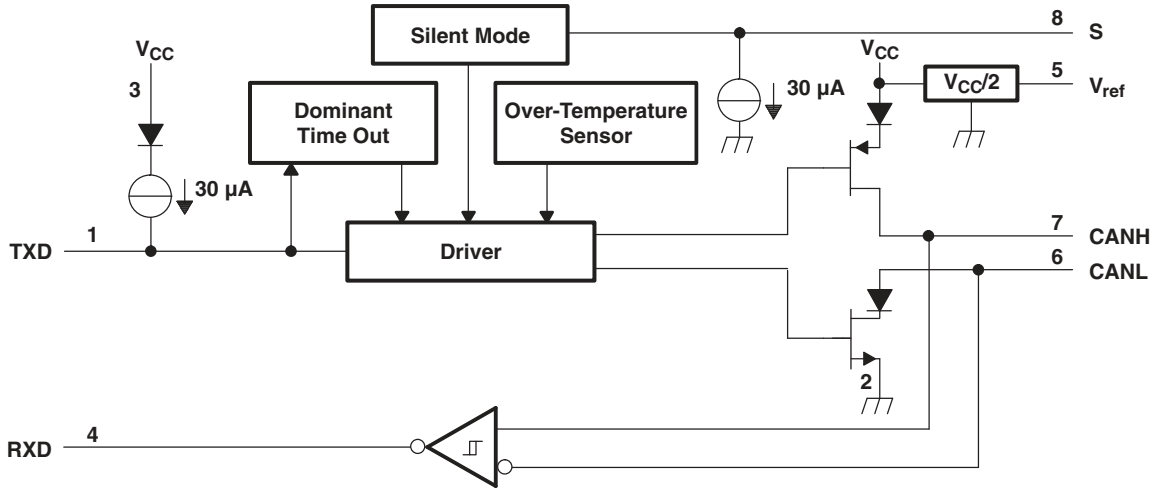
DESCRIPTION

The SN65HVD1050 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications.

As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps)(1).

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

FUNCTION BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Designed for operation is especially harsh environments, the SN65HVD1050 features cross-wire, over-voltage, and loss of ground protection from –27 V to 40 V, over-temperature protection, a –12-V to 12-V common-mode range, and withstands voltage transients from –200 V to 200 V according to ISO 7637.

Pin 8 provides for two different modes of operation: high-speed or silent mode. The high-speed mode of operation is selected by connecting S (pin 8) to ground.

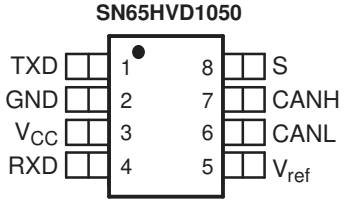
If a high logic level is applied to the S pin of the SN65HVD1050, the device enters a listen-only silent mode during which the driver is switched off while the receiver remains fully functional.

In silent mode, all bus activity is passed by the receiver output to the local protocol controller. When data transmission is required, the local protocol controller reverses this low-current silent mode by placing a logic low on the S pin to resume full operation.

A dominant time-out circuit in the SN65HVD1050 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

V_{ref} (pin 5) is available as a $V_{CC}/2$ voltage reference.

The SN65HVD1050 is characterized for operation from –40°C to 125°C.



ORDERING INFORMATION(1)

PART NUMBER	PACKAGE(2)	MARKED AS	ORDERING NUMBER
SN65HVD1050-Q1	SOIC-8	H1050Q	SN65HVD1050QDRQ1 (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Application Hint: CAN Nodes Using Common-Mode Chokes

The SN65HVD1050 has been EMC optimized to allow use in CAN systems without a common-mode choke. However, sometimes the CAN network and termination architecture may require their use. If a common-mode choke is used in a CAN node where bus-line shorts to dc voltages may be possible, care should be taken in the choice of common-mode choke (winding type, core type, and value) along with the termination and protection scheme of the node and bus. During CAN bus shorts to dc voltages the inductance of the common-mode choke may cause inductive flyback transients. Some combinations of common-mode chokes, bus termination, and shorting voltages take the bus voltages outside the absolute maximum ratings of the device, possibly leading to damage.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{CC}	Supply voltage range(2)	–0.3 V to 6 V
	Voltage range at any bus terminal (CANH, CANL, V_{ref})	–27 V to 40 V
I_O	Receiver output current	20 mA
V_I	Voltage input range, ac transient pulse(3) (CANH, CANL)	–200 V to 200 V
V_I	Voltage input range (TXD, S)	–0.3 V to 6 V
T_J	Junction temperature range	–40°C to 170°C
T_A	Operating free-air temperature range	–40°C to 125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637-1, test pulses 1, 2, 3a, 3b, 5, 6, and 7. ISO 7637-1 transient tests are ac only; if dc may be coupled in with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal (–27 V to 40 V). If common-mode chokes are used in the system and the bus lines may be shorted to dc, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients

ELECTROSTATIC DISCHARGE PROTECTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		UNIT
Electrostatic discharge (1)	Human-Body Model(2)	Bus terminals and GND	±8 kV
		All pins	±4 kV
	Charged-Device Model(3)	All pins	±1.5 kV
	Machine Model		±200 V

(1) All typical values at 25°C.
(2) Tested in accordance JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, S	2	5.25	V
V_{IL}	Low-level input voltage	TXD, S	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver		2	
T_J	Junction temperature	See Thermal Characteristics table		150	°C

SUPPLY CURRENT

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	5-V supply current	Silent mode	S at V_{CC}, $V_I = V_{CC}$		6	10	mA
		Dominant	V_I = 0 V, 60-Ω load, S at 0 V		50	70	
		Recessive	$V_I = V_{CC}$, No load, S at 0 V		6	10	

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	S at 0 V, See Figure 9	90	230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	S at 0 V, See Figure 9	90	230	ns

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, S at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	2.9	3.4	4.5	V
		CANL		0.8		1.5	
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, S at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	2	2.3	3	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, S at 0 V, See Figure 1, Figure 2, and Figure 3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, S at 0 V, See Figure 1, Figure 2, and Figure 3	1.4		3	V
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, S at 0 V, See Figure 1 and Figure 2	–0.012		0.012	V
			V_I = 3 V, S at 0 V, No Load	–0.5		0.05	
$V_{OC(ss)}$	Steady state common-mode output voltage		S at 0 V, Figure 8	2	2.3	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage				30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	μA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL open, See Figure 11	–105	–72		mA
			V_{CANH} = 12 V, CANL open, See Figure 11		0.36	1	
			V_{CANL} = –12 V, CANH open, See Figure 11	–1	–0.5		
			V_{CANL} = 12 V, CANH open, See Figure 11		71	105	
C_O	Output capacitance		See receiver input capacitance				

(1) All typical values are at 25°C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	S at 0 V, See Figure 4	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low level output	S at 0 V, See Figure 4	25	45	120	ns
t_r	Differential output signal rise time	S at 0 V, See Figure 4		25		ns
t_f	Differential output signal fall time	S at 0 V, See Figure 4		50		ns
t_{en}	Enable time from silent mode to dominant	See Figure 7			1	μs
$t_{(dom)}$	Dominant time out	↓V_I, See Figure 10	300	450	700	μs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	S at 0 V, See Table 3		800	900	mV
V_{IT-}	Negative-going input threshold voltage	S at 0 V, See Table 3	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		100	125		mV
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 6	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 6		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH or CANL = 5 V, Other pin at 0 V, V_{CC} at 0 V, TXD at 0 V		165	250	μA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	μA
C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		5		pF
R_{ID}	Differential input resistance	TXD at 3 V, S at 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, S at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching $[1 - (R_{IN\ (CANH)} / R_{IN\ (CANL)})] \times 100\%$	$V_{(CANH)} = V_{(CANL)}$	–3	0	3	%

(1) All typical values are at 25°C with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0 V or V_{CC}, See Figure 6	60	100	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		45	70	130	ns
t_r	Output signal rise time			8		ns
t_f	Output signal fall time			8		ns

S PIN CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High level input current	S at 2 V	20	40	70	μA
I_{IL}	Low level input current	S at 0.8 V	5	20	30	μA

VREF PIN CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Reference output voltage	–50 μA < I_O < 50 μA	0.4 V_{CC}	0.5 V_{CC}	0.6 V_{CC}	V

THERMAL CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance(1)		211		°C/W
		High-K thermal resistance		131		
θ_{JB}	Junction-to-board thermal resistance			53		°C/W
θ_{JC}	Junction-to-case thermal resistance			79		°C/W
P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, CL at RXD = 15 pF		112		mW
		V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, CL at RXD = 15 pF			170	
	Thermal shutdown temperature			190		°C

(1) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.

FUNCTION TABLES

Table 1. DRIVER(1)

INPUTS		OUTPUTS		BUS STATE
TXD	S	CANH	CANL	
L	L or Open	H	L	Dominant
H	X	Z	Z	Recessive
Open	X	Z	Z	Recessive
X	H	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

Table 2. RECEIVER(1)

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	Dominant
0.5 V < V_{ID} < 0.9 V	?	?
$V_{ID} \leq 0.5$ V	H	Recessive
Open	H	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

PARAMETER MEASUREMENT INFORMATION

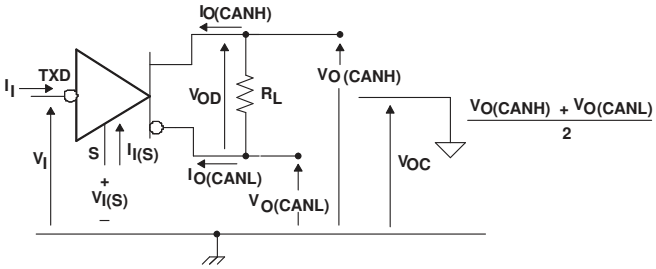


Figure 1. Driver Voltage, Current, and Test Definition

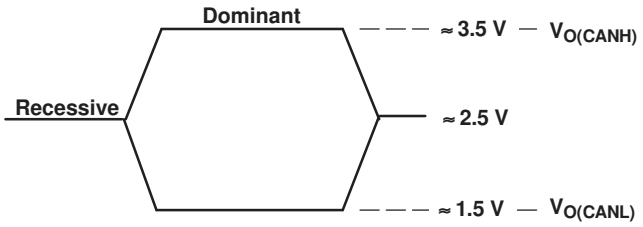


Figure 2. Bus Logic State Voltage Definitions

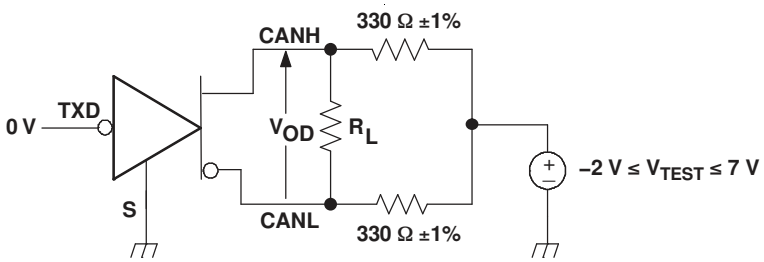


Figure 3. Driver V_{OD} Test Circuit

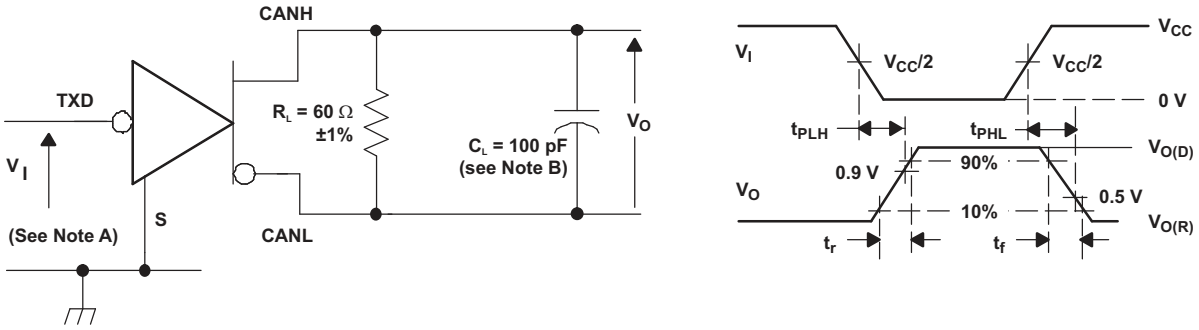


Figure 4. Driver Test Circuit and Voltage Waveforms

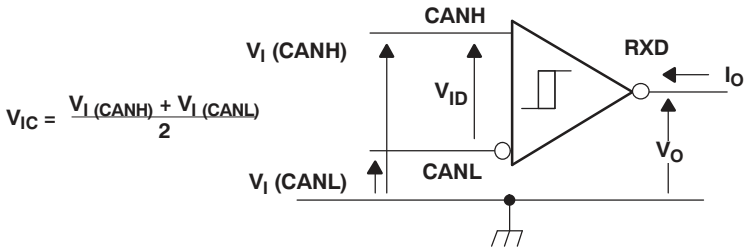
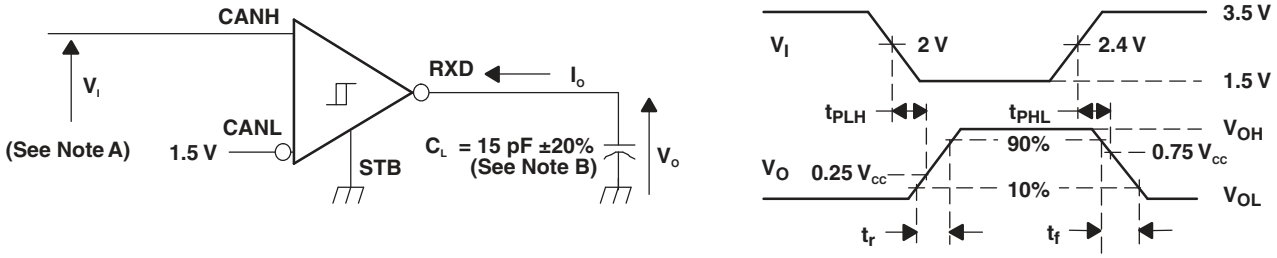


Figure 5. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



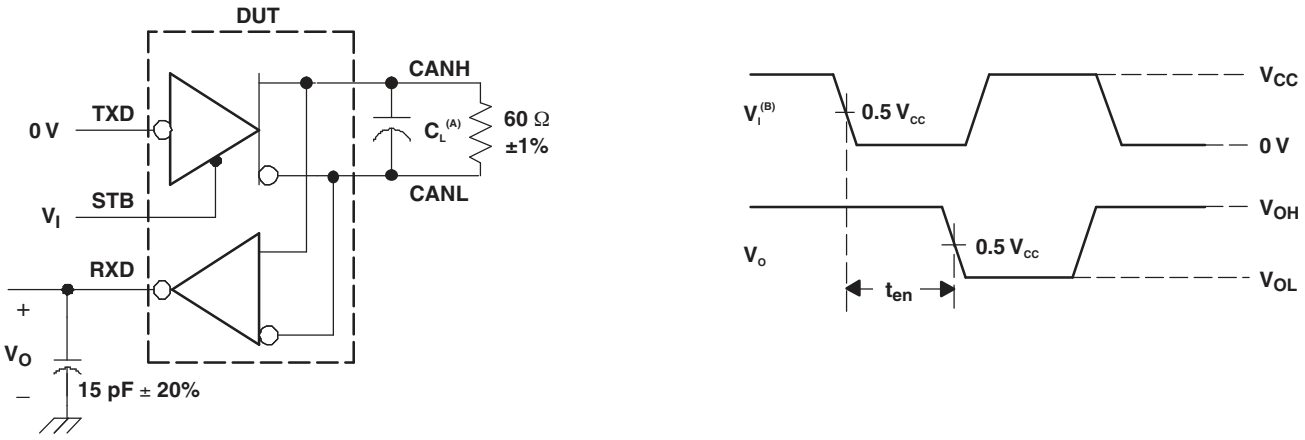
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 3. Differential Input Voltage Threshold Test

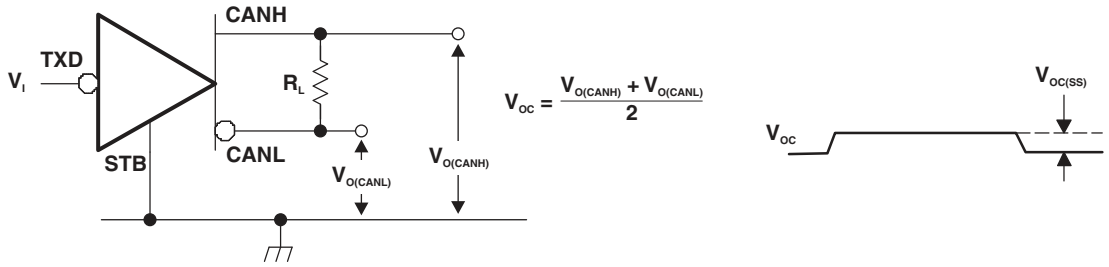
INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

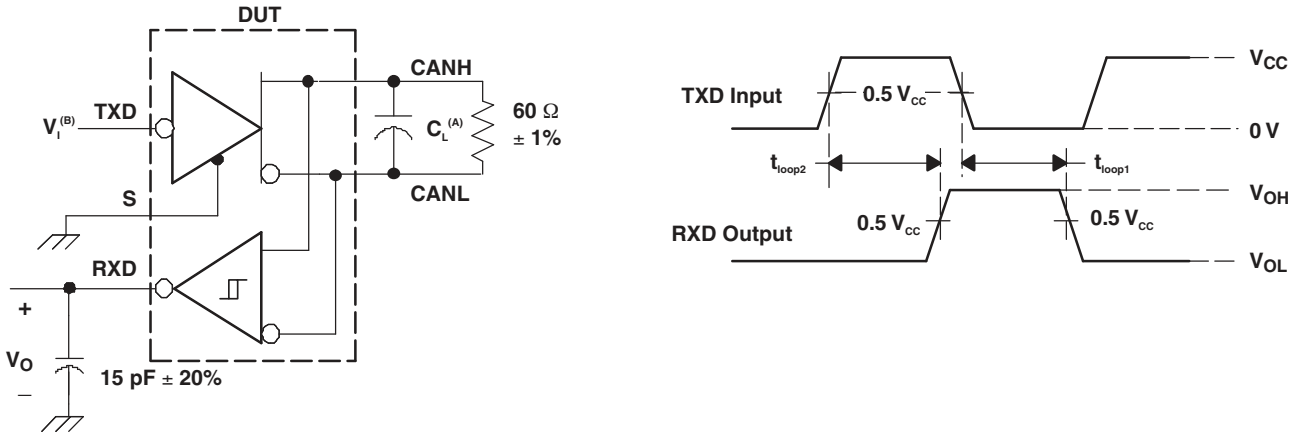
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 7. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

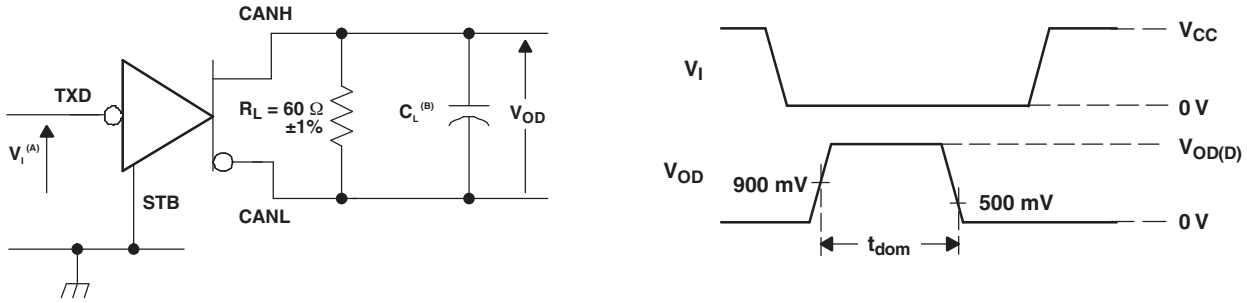
Figure 8. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 10. Dominant Time-Out Test Circuit and Waveforms

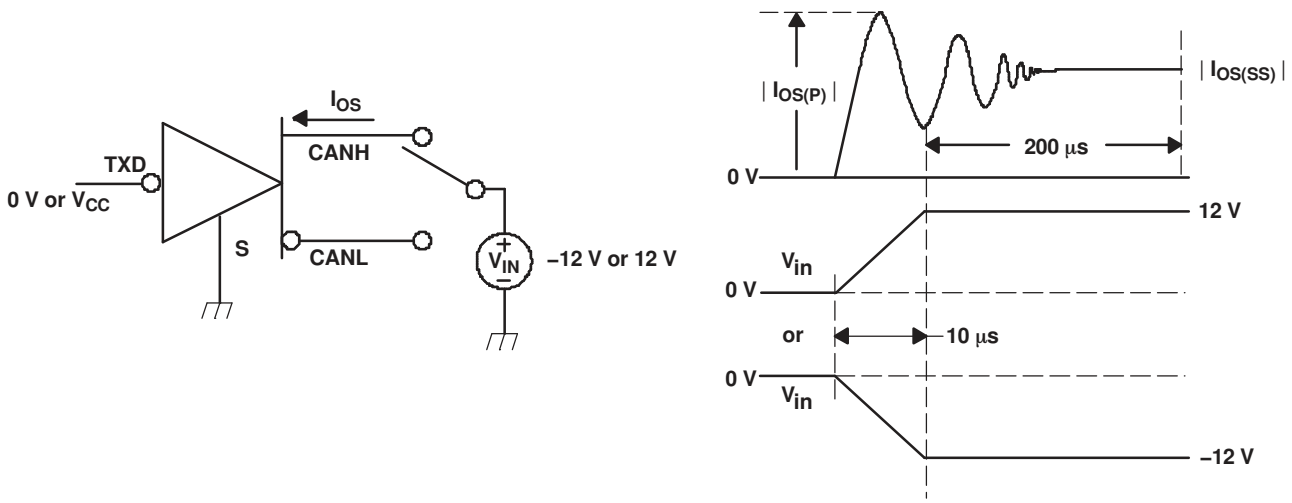
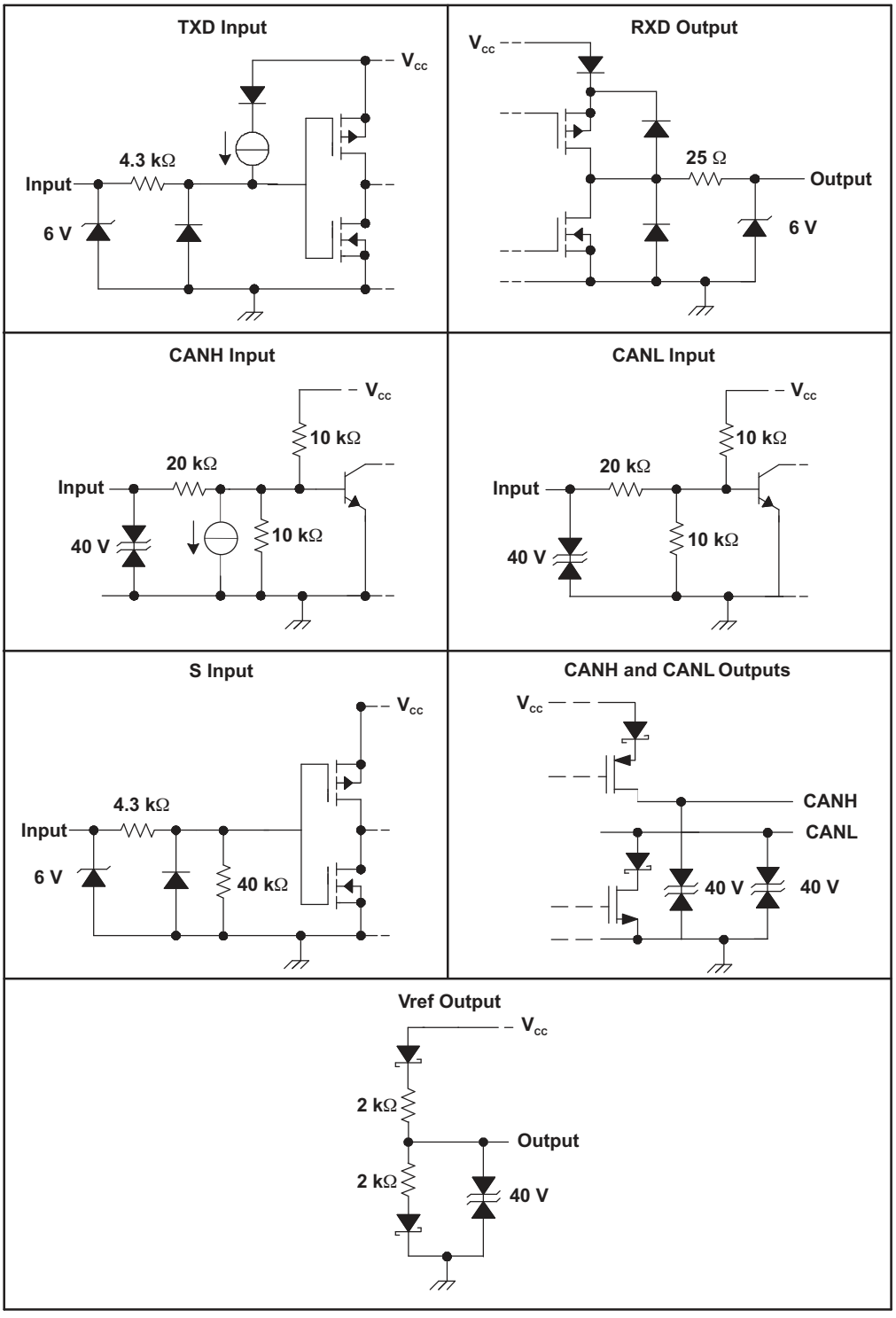


Figure 11. Driver Short-Circuit Current Test and Waveforms

Equivalent Input and Output Schematic Diagrams



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1050QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H1050Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN65HVD1050-Q1 :

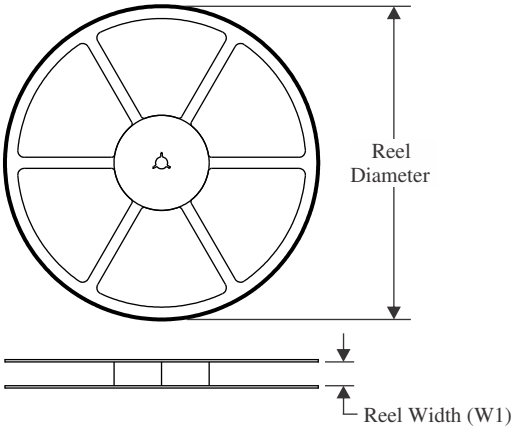
- Catalog: SN65HVD1050
- Enhanced Product: SN65HVD1050-EP

NOTE: Qualified Version Definitions:

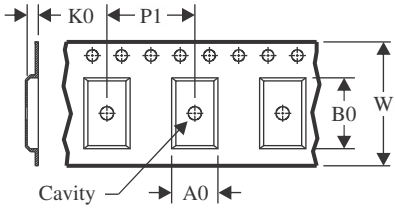
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

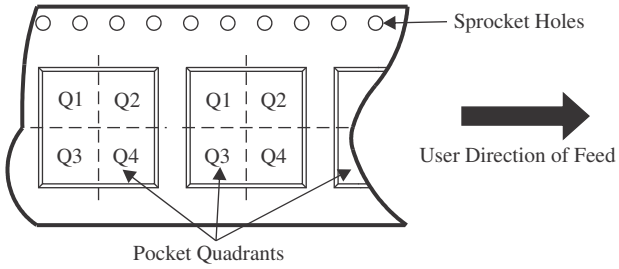


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

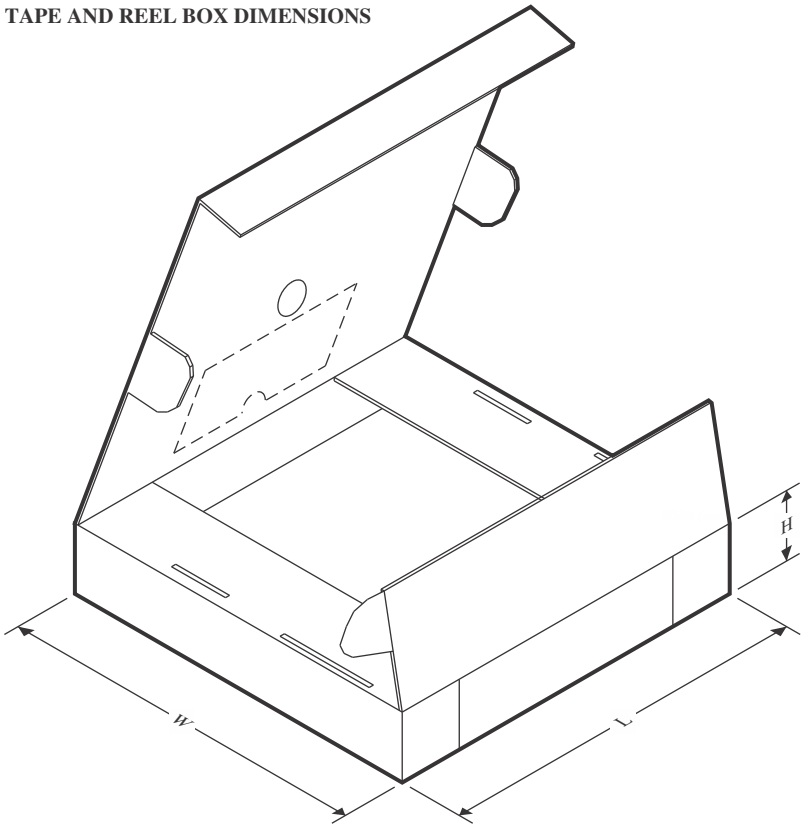
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

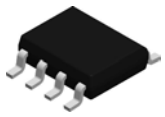
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1050QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1050QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

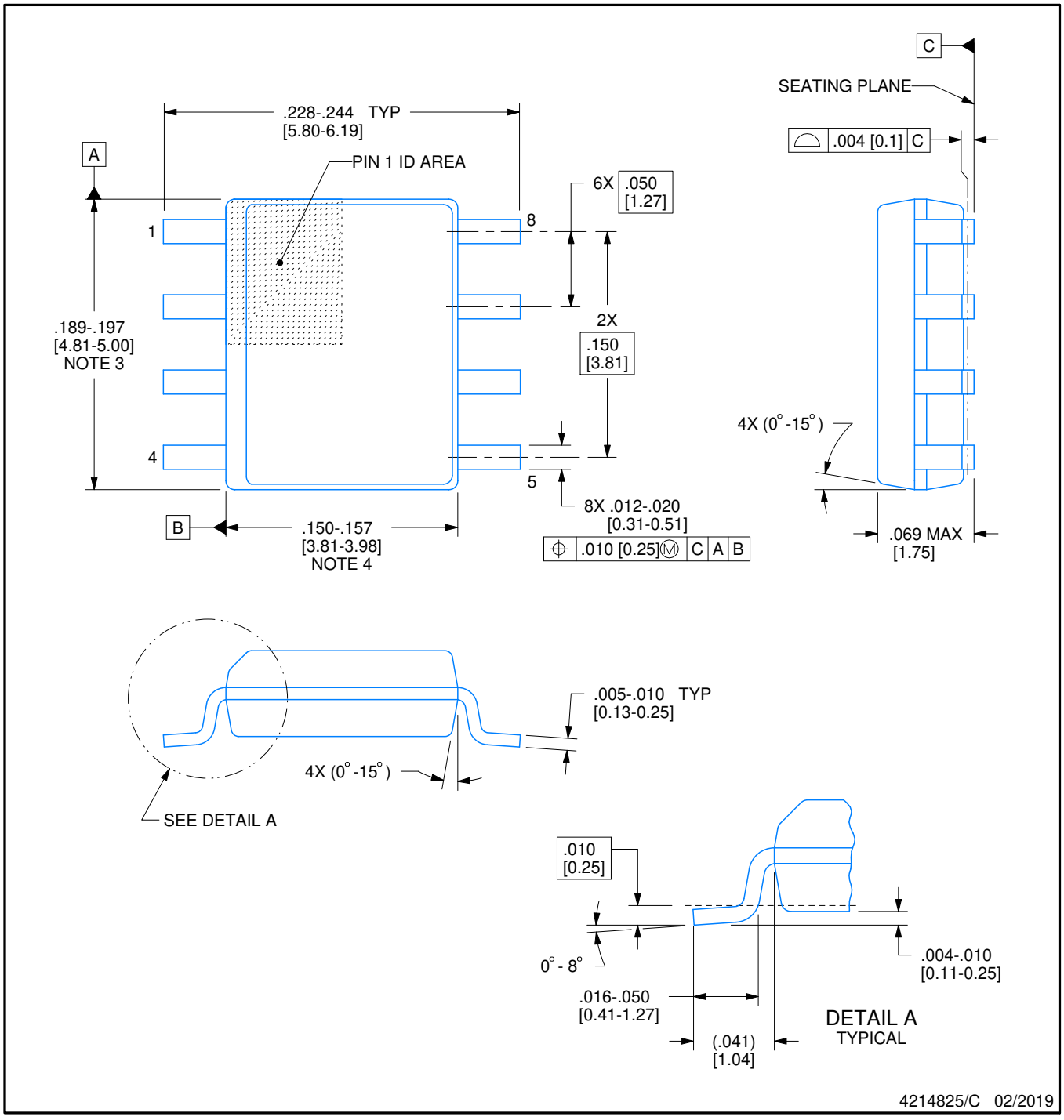


PACKAGE OUTLINE

D0008A

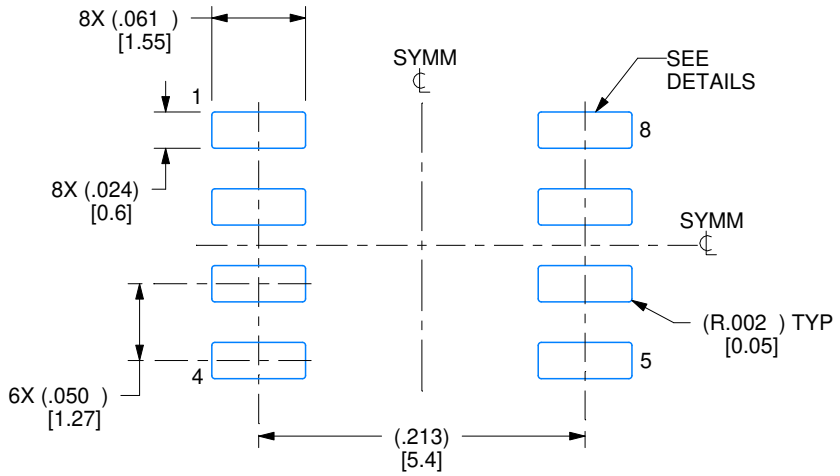
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

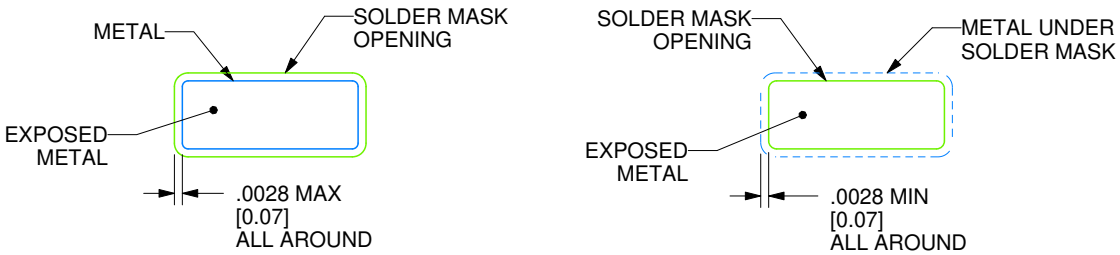


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

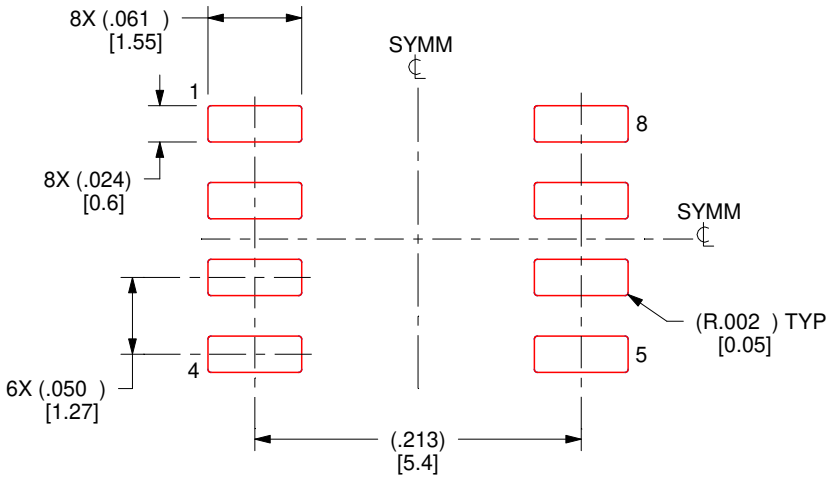
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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