

# N-channel 25 V 8.65 m $\Omega$ logic level MOSFET in LFPAK33 using NextPower Technology

Rev. 3 — 15 June 2012

**Product data sheet** 

### 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

#### 1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

### 1.3 Applications

- DC-to-DC converters
- Load switching

Synchronous buck regulator

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25^{\circ}C$	-	-	25	V
I <sub>D</sub>	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u>	-	-	55	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	45	W
Tj	junction temperature		-55	-	175	°C
Static characte	eristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	9.8	11.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	7.55	8.65	mΩ
Dynamic chara	acteristics					
$Q_{GD}$	gate-drain charge	$V_{GS}$ = 4.5 V; $I_D$ = 15 A; $V_{DS}$ = 12.5 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	1.2	-	nC
Q <sub>G(tot)</sub>	total gate charge	$V_{GS}$ = 4.5 V; $I_D$ = 15 A; $V_{DS}$ = 12.5 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	5.4	-	nC



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		D
3	S	source		$G \longrightarrow \overline{A}$
4	G	gate		9-1-1
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 S
			SOT1210 (LFPAK33)	

## 3. Ordering information

Table 3. Ordering information

Type number	number Package				
	Name	Description	Version		
PSMN9R0-25MLC	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210		

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25^{\circ}C$	-	25	V
$V_{GS}$	gate-source voltage		-20	20	٧
$I_D$	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{}$	-	55	Α
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <u>Figure 1</u>	-	39	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; see Figure 4	-	219	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	45	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
$V_{ESD}$	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	120	-	V
Source-drain	n diode				
Is	source current	T <sub>mb</sub> = 25 °C	-	41	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$	-	219	Α
Avalanche ru	ıggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 55 A; $V_{sup} \le$ 25 V; $R_{GS}$ = 50 Ω; unclamped; see <u>Figure 3</u>	-	8.7	mJ

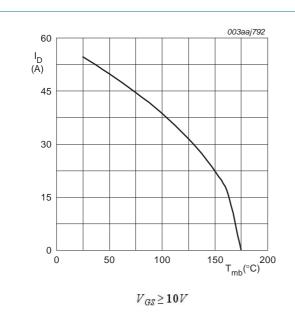


Fig 1. Continuous drain current as a function of mounting base temperature

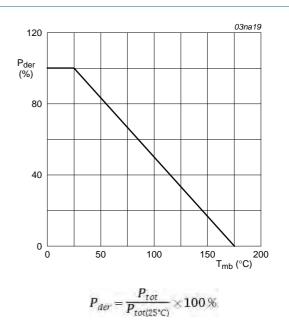


Fig 2. Normalized total power dissipation as a function of mounting base temperature

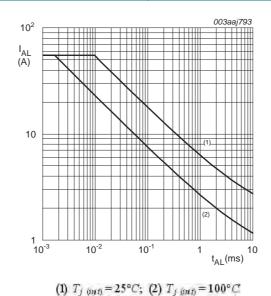
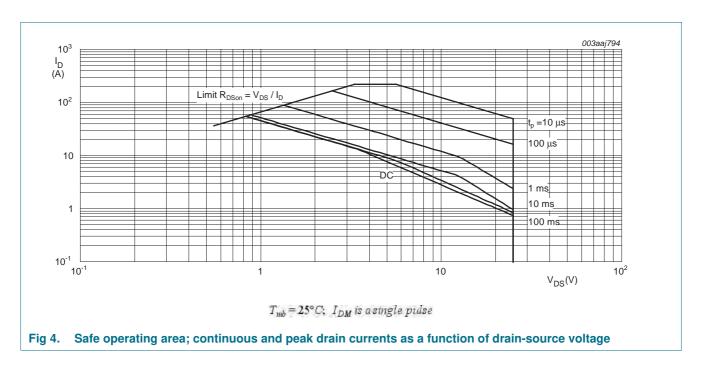


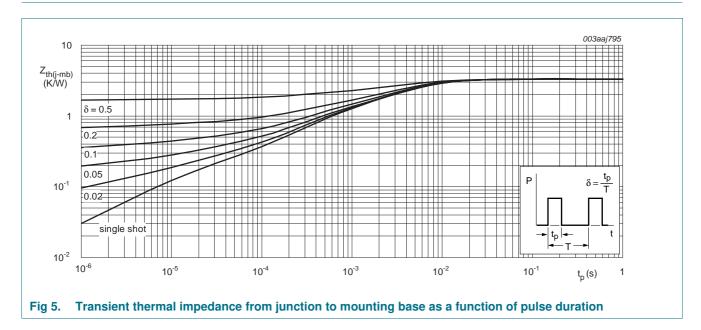
Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see <u>Figure 5</u>	-	3.1	3.32	K/W



## 6. Characteristics

Table 6 Characteristics

Table 6. C	haracteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac	eteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	25	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^{\circ}C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1.3	1.5	1.95	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature		-	-3.5	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μΑ
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see Figure 10	-	9.8	11.3	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 150 \text{ °C};$ see Figure 10; see Figure 11	-	-	18.1	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	7.55	8.65	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 ^{\circ}\text{C};$ see <u>Figure 10</u> ; see <u>Figure 11</u>	-	-	13.9	mΩ
$R_{G}$	gate resistance	f = 1 MHz	0.95	1.9	3.8	Ω
Dynamic cha	aracteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 12.5 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 12; see Figure 13	-	11.7	-	nC
		$I_D = 15 \text{ A}; V_{DS} = 12.5 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	5.4	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	11.1	-	nC
Q <sub>GS</sub>	gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 12.5 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	1.8	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge	see Figure 12; see Figure 13	-	1.2	-	nC
$Q_{GS(th\text{-}pI)}$	post-threshold gate-source charge		-	0.6	-	nC
Q <sub>GD</sub>	gate-drain charge		-	1.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I <sub>D</sub> = 15 A; V <sub>DS</sub> = 12.5 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	2.5	-	V
C <sub>iss</sub>	input capacitance	$V_{DS} = 12.5 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	705	-	pF
Coss	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	206	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	67	-	pF

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS}=12.5~V;~R_L=0.8~\Omega;~V_{GS}=4.5~V;$	-	7.1	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$	-	10.1	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	11.1	-	ns
t <sub>f</sub>	fall time		-	6.1	-	ns
Q <sub>oss</sub>	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 12.5 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	5.3	-	nC
Source-drai	in diode					
$V_{SD}$	source-drain voltage	$I_S = 15 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see Figure 15	-	0.83	1.1	V
t <sub>rr</sub>	reverse recovery time	$I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	14.8	-	ns
Q <sub>r</sub>	recovered charge	$V_{DS} = 12.5 \text{ V}$	-	7.5	-	nC
ta	reverse recovery rise time	$V_{GS} = 0 \text{ V; } I_S = 15 \text{ A; } dI_S/dt = -100 \text{ A/}\mu\text{s;}$ $V_{DS} = 12.5 \text{ V; see } \frac{\text{Figure } 16}{\text{Miss}}$	-	8.9	-	ns
t <sub>b</sub>	reverse recovery fall time		-	5.9	-	ns

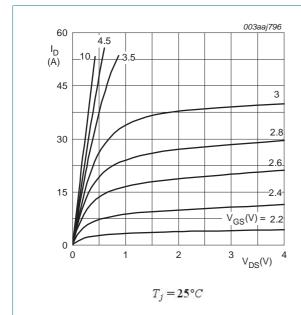


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

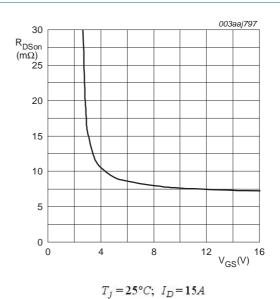


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

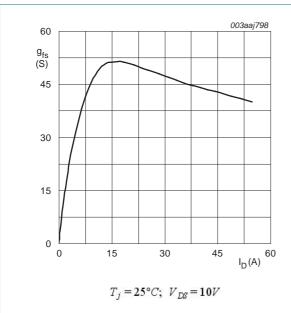


Fig 8. Forward transconductance as a function of drain current; typical values

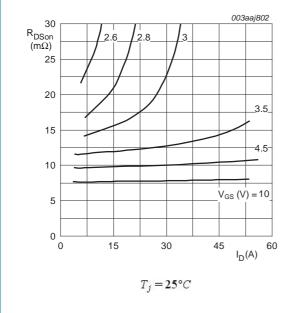


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

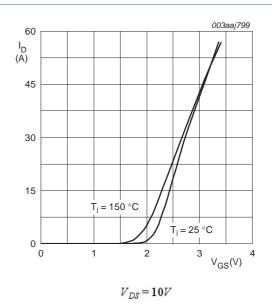


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

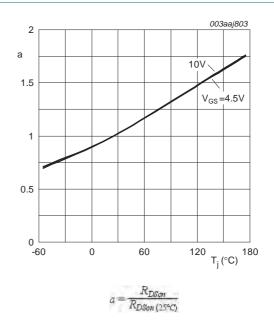


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature

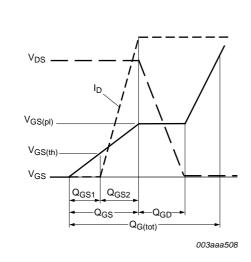


Fig 12. Gate charge waveform definitions

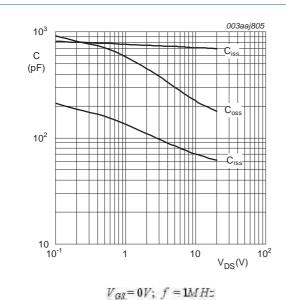


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

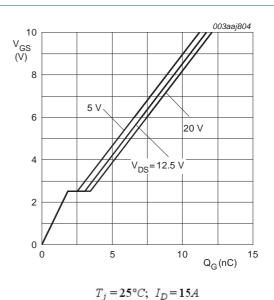


Fig 13. Gate-source voltage as a function of gate charge; typical values

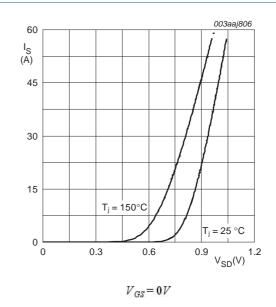
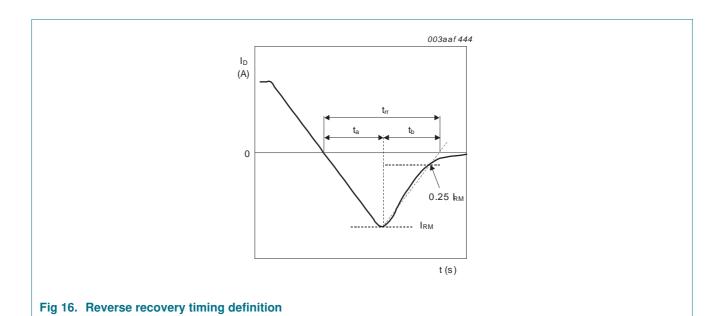


Fig 15. Source current as a function of source-drain voltage; typical values



## 7. Package outline

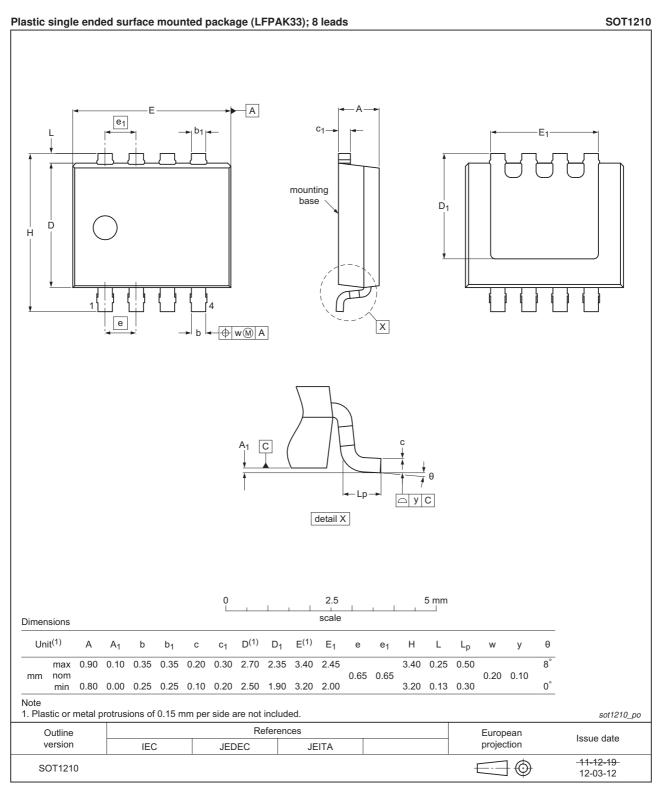


Fig 17. Package outline SOT1210 (LFPAK33)

PSMN9R0-25MLC

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N-channel 25 V 8.65 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

## 8. Revision history

### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN9R0-25MLC v.3	20120615	Product data sheet	-	PSMN9R0-25MLC v.2
Modifications:	<ul> <li>Various changes to</li> </ul>	content.		
PSMN9R0-25MLC v.2	20120607	Product data sheet	-	PSMN9R0-25MLC v.1

### N-channel 25 V 8.65 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

### 9. Legal information

#### 9.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions".
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## PSMN9R0-25MLC

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