

## Description

The 8V97053 is a high-performance Wideband RF Synthesizer / PLL optimized for use as the local oscillator (LO) in Multi-Carrier, Multi-mode FDD, and TDD Base Station radio card. It is offered in a compact  $5 \times 5$ , 32-VFQFPN.

The 8V97053 Wideband RF Synthesizer / PLL offers a default Fractional Mode with the option to use it with an Integer mode. It requires an external loop filter.

The 8V97053 with integrated Voltage Controlled Oscillator (VCO) supports output frequencies from 34.375MHz to 4400MHz, and maintains superior phase noise and spurious performance.

RF\_OUT<sub>[A:B]</sub> output drivers have independently programmable output power ranging from -4dBm to +7dBm. The RF\_OUT outputs can be muted. The mute function is accessible via a SPI command or mute pin.

The operation of the 8V97053 is controlled by writing to registers through a 3-wire SPI interface. The 8V97053 has an additional option that allows users to read back values from registers by configuring the MUX\_OUT pin as a SDO for the SPI interface. The SPI interface is compatible with 1.8V logic and is tolerant to 3.3V.

In multi-service base stations, very low noise oscillators are required to generate a large variety of frequencies to the mixers while maintaining excellent phase noise performance and low power. The 8V97053 offers a large tuning range capable of providing multi-band local oscillator (LO) frequency synthesis in multi-mode base stations, thus limiting the use of multiple narrow band RF Synthesizers and reducing the BOM complexity and cost. The device can operate over -40°C to +85°C industrial temperature range.

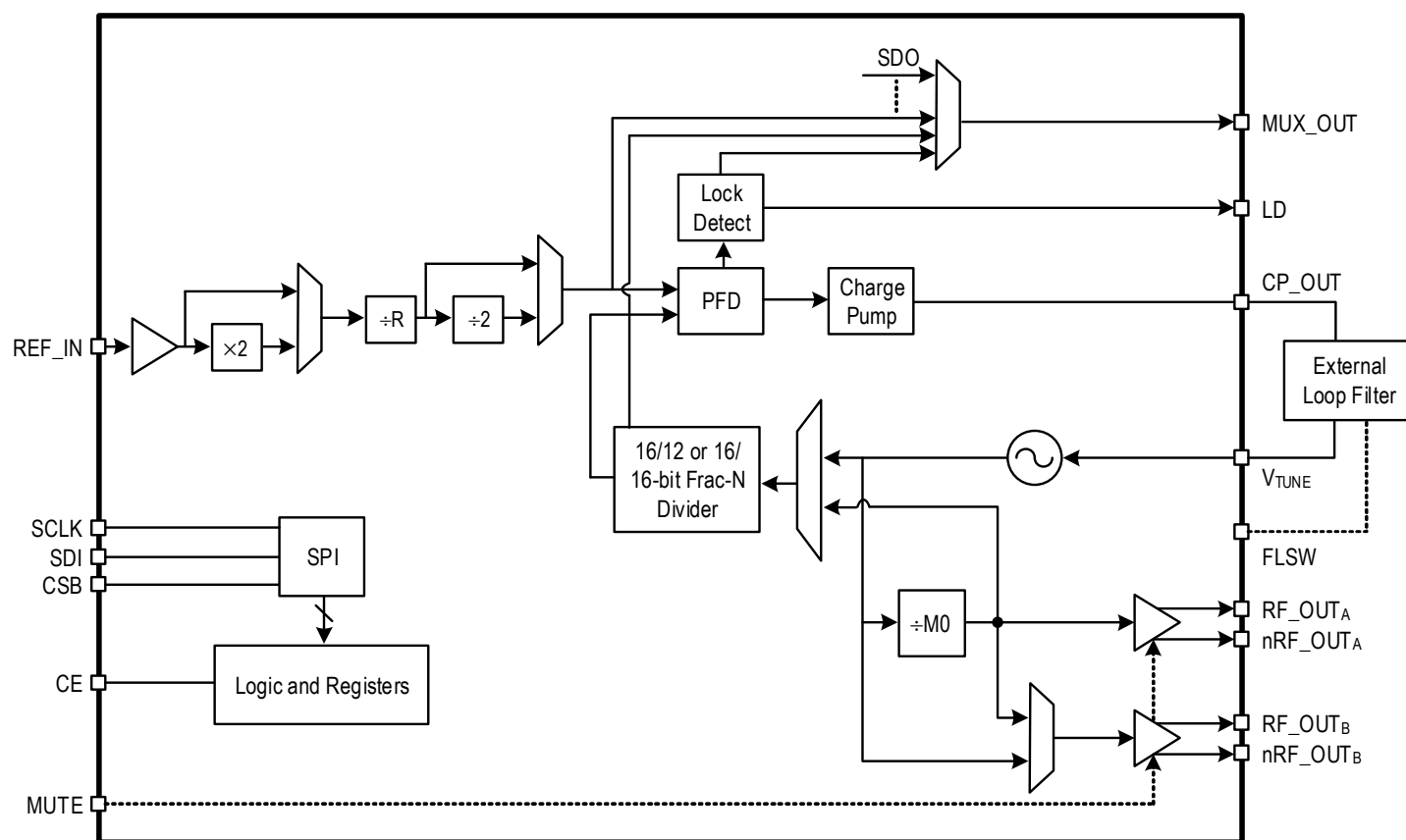
## Typical Applications

- Wireless infrastructure
- Test equipment
- CATV equipment
- Military and aerospace
- Wireless LAN
- Clock generation

## Features

- Dual Differential Outputs
- Output frequency range: 34.375MHz to 4400MHz (continuous range)
- RF Output Divide by 1, 2, 4, 8, 16, 32, 64
- Open Drain Outputs (see [Output Clock Distribution](#))
- Fractional-N synthesizer (also supports Integer-N mode)
- 16-bit integer and 12-bit fractional (16-bit fractional when using the register 7)
- 3- or 4-wire SPI interface (compatible with 3.3V and 1.8V)
- Single 3.3V supply
- Logic compatibility: 1.8V
- Programmable output power level: -4dBm to +5dBm (up to +7 when using register 6)
- Mute function
- Ultra low PN for 1.65GHz LO: -142.08dBc/Hz at 1MHz Offset, (typical)
- Lock Detect Indicators
- Input reference frequency: 5MHz to 310MHz
- Automatic VCO band selection (Autocal feature)
- -40°C to +85°C ambient operating temperature
- Supports case temperature  $\leq 105^\circ\text{C}$  operations
- Lead-free (RoHS 6), 32-VFQFPN,  $5 \times 5$  mm package

## Block Diagram



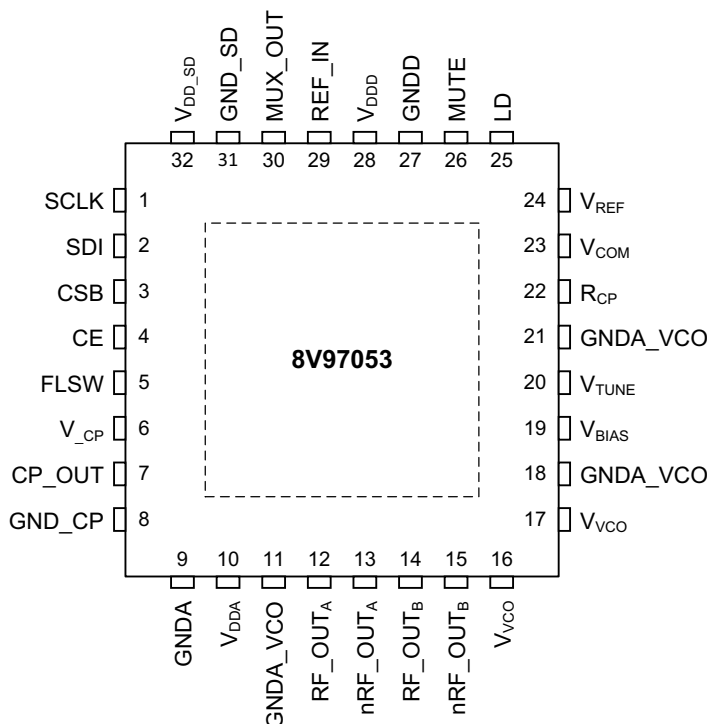
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# Pin Assignments

**Figure 1. Pin Assignments for 32-VFQFPN, 5 x 5 Package – Top View**



# Pin Descriptions

**Table 1. Pin Description<sup>[a]</sup>**

Pin	Name	Type	Description
1	SCLK	LVC MOS Input Pulldown	Serial Clock Input. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant.
2	SDI	LVC MOS Input Pullup	Serial Data Input. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant.
3	nCS	LVC MOS Input Pulldown	Load Enable. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant. Active Low.
4	CE	LVC MOS Input Pullup	Chip Enable. On logic Low, powers down the device and puts the charge pump into High-Impedance mode. Powers up the device on logic High.
5	FLSW	Analog	Fast Lock Switch. A connection should be made from the loop filter to this pin when using the fast lock mode.
6	V <sub>CP</sub>	Power	Charge Pump Power Supply. V <sub>CP</sub> must have the same value as V <sub>DDA</sub> . Place decoupling capacitors to the ground plane as close to this pin as possible.
7	CP_OUT	Analog	Charge Pump Output. When enabled, this output provides ±ICP to the external loop filter. The output of the loop filter is connected to V <sub>TUNE</sub> to drive the internal VCO.
8	GND_CP	Ground	Charge Pump Power Supply Ground.
9	GNDA	Ground	Analog Power Supply Ground.
10	V <sub>DDA</sub>	Power	Analog Supply. This pin ranges from 3.3V ± 5%. V <sub>DDA</sub> must have the same value as V <sub>DDD</sub> .

**Table 1. Pin Description<sup>[a]</sup> (Cont.)**

Pin	Name	Type		Description
11	GNDA_VCO	Ground		VCO Analog Power Supply Ground.
12	RF_OUT <sub>A</sub>	Output		Clock Output pair A. The output level is programmable.
13	nRF_OUT <sub>A</sub>	Output		Clock Output pair A. The output level is programmable.
14	RF_OUT <sub>B</sub>	Output		Clock Output pair B. The output level is programmable.
15	nRF_OUT <sub>B</sub>	Output		Clock Output pair B. The output level is programmable.
16	V <sub>VCO</sub>	Power		VCO Supply. This pin ranges from 3.3V ± 5%. V <sub>VCO</sub> must have the same value as V <sub>DDA</sub> .
17	V <sub>VCO</sub>	Power		VCO Supply. This pin ranges from 3.3V ± 5%. V <sub>VCO</sub> must have the same value as V <sub>DDA</sub> .
18	GNDA_VCO	Ground		VCO Analog Power Supply Ground.
19	V <sub>BIAS</sub>	Analog		Place decoupling capacitors (≥ 0.1μF) to ground, as close to this pin as possible.
20	V <sub>TUNE</sub>			Control Input to tune the VCO.
21	GNDA_VCO	Ground		VCO Analog Power Supply Ground.
22	R <sub>CP</sub>	Analog		Sets the charge pump current. Requires external resistor.
23	V <sub>COM</sub>	Analog		Place decoupling capacitors (≥ 0.1μF) to ground, as close to this pin as possible.
24	V <sub>REF</sub>	Analog		Place decoupling capacitors (≥ 0.1μF) to ground, as close to this pin as possible.
25	LD	LVC MOS Output		Lock Detect. Logic High indicates PLL lock. Logic Low indicates loss of PLL lock.
26	MUTE	LVC MOS Input	Pullup	RF_OUT <sub>A</sub> and RF_OUT <sub>B</sub> Power-Down. A logic low on this pin mutes the RF_OUT outputs and puts them in High-Impedance.
27	GNDD	Ground		Digital Power Supply Ground.
28	V <sub>DDD</sub>	Power		Digital Supply. V <sub>DDD</sub> must have the same value as V <sub>DDA</sub> .
29	REF_IN	LVC MOS Input	Analog	Reference Input. This CMOS input has a nominal threshold of V <sub>DDA</sub> /2 and a DC equivalent input resistance of 100kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be AC-coupled.
30	MUX_OUT	LVC MOS Output		Multiplexed Output and Serial Data Out. Refer to <a href="#">Table 13</a> .
31	GND_SD	Ground		Digital Sigma Delta Modulator Power Supply Ground.
32	V <sub>DD_SD</sub>	Power		Digital Sigma Delta Modulator Supply. V <sub>DD_SD</sub> must have the same value as V <sub>DDA</sub> .
EP	Exposed Pad	Ground		Must be connected to GND.

[a] Pullup and Pulldown refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$C_{in}$	Input Capacitance			4		pF
$R_{OUT}$	LVC MOS Output Impedance	MUX_OUT and LD		38		$\Omega$
$R_{PULLUP}$	Input Pullup Resistor			51		k $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k $\Omega$

**Table 3. Supply Pins and Associated Current Return Paths**

Power Supply Pin Number	Power Supply Pin Name	Associated Ground Pin Number	Associated Ground Pin Name
10	$V_{DDA}$	9	GNDA
28	$V_{DDD}$	27	GNDD
32	$V_{DD\_SD}$	31	GND_SD
16, 17	$V_{VCO}$	11, 18, 21	GNDA_VCO
6	$V_{\_CP}$	8	GND_CP

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V97053 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 4. Absolute Maximum Ratings**

Item	Rating
Supply Voltage, $V_{DDX}^{[a]}$	3.63V
Analog Supply Voltage, $V_{DDA}$	3.63V
Input, $V_I$ REF_IN Other Inputs (MUTE, SDI, FLSW, $V_{TUNE}$ )	-0.5 to $V_{DDA} + 0.5V$
Outputs, $V_O$ RF_OUT <sub>A-B</sub> , nRF_OUT <sub>A-B</sub>	-0.5 to $V_{DDA} + 0.5V$
Outputs, $V_O$ (SCLK, LD, nCS, MUX_OUT)	-0.5 to $V_{DDA} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	40mA 65mA
Outputs, $I_O$ (SCLK, LD, nCS, MUX_OUT) Continuous Current Surge Current	8mA 13mA
Junction Temperature, $T_J$	125°C
Storage Temperature, $T_{STG}$	-65°C to 150°C

[a]  $V_{DDX}$  denotes  $V_{DDD}$ ,  $V_{\_CP}$ ,  $V_{DD\_SD}$ ,  $V_{VCO}$ .

## DC Electrical Characteristics

**Table 5. Power Supply DC Characteristics,  $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  [a] [b] [c]**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DDX}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$I_{DDX}$ [d]	Power Supply Current			130	145	mA
$I_{DDA}$ [e]	Analog Supply Current	RF_OUT <sub>A</sub> / nRF_OUT <sub>A</sub> - Active RF_OUT <sub>B</sub> / nRF_OUT <sub>B</sub> - Muted		60	77	mA
		RF_OUT <sub>A</sub> / nRF_OUT <sub>A</sub> - Active RF_OUT <sub>B</sub> / nRF_OUT <sub>B</sub> - Active		85	105	mA
		RF_OUT <sub>A</sub> / nRF_OUT <sub>A</sub> - Muted RF_OUT <sub>B</sub> / nRF_OUT <sub>B</sub> - Muted		40	50	mA
$I_{VCO}$	VCO Supply Current			85		mA
	Power Down Mode			10	15	mA

[a]  $V_{DDX}$  denotes  $V_{DD}$ ,  $V_{CP}$ ,  $V_{DD\_SD}$ ,  $V_{VCO}$ .

[b] RF Outputs Terminated  $50\Omega \pm 1\%$  to  $V_{DDA}$ .

[c] Output Power set to +2dBm.

[d]  $I_{DDX}$  denotes  $I_{DD} + I_{CP} + I_{DD\_SD} + I_{VCO}$ .

[e]  $I_{DDA}$  is dependent on the value of the M0 output divider. The numbers indicated for  $I_{DDA}$  show the current consumption when using the output divider M0 = 64, for which  $I_{DDA}$  is higher than when using any other M0 divider value.

**Table 6. Output Divider Incremental Current [a]**

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Output Divider Supply Current	Divide by 2		8.0		mA
	Divide by 4		7.0		mA
	Divide by 8		1.5		mA
	Divide by 16		1.5		mA
	Divide by 32		1.5		mA
	Divide by 64		1.5		mA

[a] RF Output divider ( $\div M0$ ) has an incremental increase in current as the divider value increases. This specification is the incremental current change per output divider step. For example, current of divide-by-2 is 8mA more than divide-by-1, current of divide-by-4 is 7mA more than divide-by-2, and so on. The total increase from  $\div 1$  to  $\div 64$  is  $8mA + 7mA + 1.5mA + 1.5mA + 1.5mA + 1.5mA = 21mA$ .



**Table 7. Typical Current by Power Domain<sup>[a]</sup>**

Pin Name	Pin Number	Typical Current	Unit
V <sub>CP</sub>	6	24	mA
V <sub>VCO</sub>	16, 17	22	mA
V <sub>DDD</sub>	28	0.8	mA
V <sub>DD_SD</sub>	32	9	mA
V <sub>DDA</sub>	10	63	mA

[a] Operating conditions are: REF\_IN = 25MHz, INT = 100 (integer mode), RF Divider = ÷1,  
RF\_OUT<sub>A</sub> = RF\_OUT<sub>B</sub> = 2.5GHz, RF<sub>POWER</sub> = -1dBm, Charge Pump = 0.31mA

**Table 8. LVCMOS DC Characteristics, V<sub>DDX</sub> = V<sub>DDA</sub> = 3.3V ± 5%, T<sub>A</sub> = -40°C to 85°C<sup>[a]</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input High Voltage	MUTE, CE		1.8		V <sub>DDX</sub>	V
		SDI, SCLK, nCS		1.5		V <sub>DDX</sub>	V
V <sub>IL</sub>	Input Low Voltage			-0.3		0.6	V
I <sub>IH</sub>	Input High Current	SDI, MUTE, CE	V <sub>DDX</sub> = 3.465V, V <sub>IN</sub> = 1.8V			5	μA
		SCLK, nCS	V <sub>DDX</sub> = 3.465V, V <sub>IN</sub> = 1.8V			150	μA
I <sub>IL</sub>	Input Low Current	SDI, MUTE, CE	V <sub>DDX</sub> = 3.465V, V <sub>IN</sub> = 0V	-150			μA
		SCLK, nCS	V <sub>DDX</sub> = 3.465V, V <sub>IN</sub> = 0V	-5			μA
V <sub>OH</sub>	Output High Voltage	MUX_OUT, LD	V <sub>DDX</sub> = 3.465V; I <sub>OH</sub> = -500μA	V <sub>DDX</sub> - 0.4			V
V <sub>OL</sub>	Output Low Voltage	MUX_OUT, LD	V <sub>DDX</sub> = 3.465V; I <sub>OL</sub> = 500μA			0.4	V

[a] V<sub>DDX</sub> denotes V<sub>DDD</sub>, V<sub>CP</sub>, V<sub>DD\_SD</sub>, V<sub>VCO</sub>.

# AC Electrical Characteristics

**Table 9. AC Characteristics,  $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  [a]**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
REF_IN	Input Reference Frequency [b]		Ref Doubler Disabled	5		310	MHz
			Ref Doubler Enabled	5		100	MHz
$V_{PP}$	Input Sensitivity	REF_IN	Biased at $V_{DDA}/2$ [c]	0.7		$V_{DDA}$	V
$f_{VCO}$	VCO Frequency		Fundamental VCO Mode	2200		4400	MHz
$f_{RF\_OUT}$	Output Frequency		Divider Values: 1, 2, 4, 8, 16, 32, 64	34.375		4400	MHz
$f_{PFD}$	PFD Frequency		Fractional Mode			125	MHz
			Integer Mode			310	MHz
$K_{VCO}$	VCO Sensitivity				60		MHz/V
$t_{LOCK}$	PLL Lock Time		Time from Low to High nCS until at Normal Mode, Low to High LD		250		$\mu s$
-	Output Power Variation				$\pm 1$		dB
-	RF Output Power		Muted, ( $M0 \neq 1$ )		< -80		dBm
-	Min/Max VCO Tuning Voltage				0.5 / 2.5		V

[a]  $V_{DDX}$  denotes  $V_{DD}$ ,  $V_{CP}$ ,  $V_{DD\_SD}$ ,  $V_{VCO}$ .

[b] For REF\_IN < 10MHz, the slew rate must be > 21V/ $\mu s$ .

[c] AC-coupling: the device provides an internal  $V_{DDA}/2$  bias.

**Table 10. RF\_OUT [A:B] Phase Noise and Jitter Characteristics,  $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  [a] [b]**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$\phi_N(100k)$	RF Output Phase Noise Performance at 730MHz (Open Loop)	100kHz Offset from Carrier		-124.75		dBc/Hz
$\phi_N(800k)$		800kHz Offset from Carrier		-147.14		dBc/Hz
$\phi_N(1M)$		1MHz Offset from Carrier		-148.72		dBc/Hz
$\phi_N(5M)$		5MHz Offset from Carrier		-154.56		dBc/Hz
$\phi_N(10M)$		10MHz Offset from Carrier		-155.59		dBc/Hz
$\phi_N(\infty)$		Noise Floor ( $\geq 30MHz$ from Carrier)		-156		dBc/Hz
$\phi_N(100k)$	RF Output Phase Noise Performance at 1.1GHz (Open Loop)	100kHz Offset from Carrier		-115.11		dBc/Hz
$\phi_N(800k)$		800kHz Offset from Carrier		-137.79		dBc/Hz
$\phi_N(1M)$		1MHz Offset from Carrier		-139.94		dBc/Hz
$\phi_N(5M)$		5MHz Offset from Carrier		-152.11		dBc/Hz
$\phi_N(10M)$		10MHz Offset from Carrier		-154.5		dBc/Hz
$\phi_N(\infty)$		Noise Floor ( $\geq 30MHz$ from Carrier)		-156		dBc/Hz

**Table 10. RF\_OUT<sub>[A:B]</sub> Phase Noise and Jitter Characteristics, V<sub>DDX</sub> = V<sub>DDA</sub> = 3.3V ± 5%, T<sub>A</sub> = -40°C to 85°C [a] [b] (Cont.)**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$\varphi_N(100k)$	RF Output Phase Noise Performance at 1.65GHz (Open Loop)	100kHz Offset from Carrier		-115.57		dBc/Hz
$\varphi_N(800k)$		800kHz Offset from Carrier		-139.83		dBc/Hz
$\varphi_N(1M)$		1MHz Offset from Carrier		-142.08		dBc/Hz
$\varphi_N(5M)$		5MHz Offset from Carrier		-152.36		dBc/Hz
$\varphi_N(10M)$		10MHz Offset from Carrier		-153.62		dBc/Hz
$\varphi_N(\infty)$		Noise Floor ( $\geq 30$ MHz from Carrier)		-153.81		dBc/Hz
$\varphi_N(100k)$	RF Output Phase Noise Performance at 2.3GHz (Open Loop)	100kHz Offset from Carrier		-109		dBc/Hz
$\varphi_N(800k)$		800kHz Offset from Carrier		-132.18		dBc/Hz
$\varphi_N(1M)$		1MHz Offset from Carrier		-134.37		dBc/Hz
$\varphi_N(5M)$		5MHz Offset from Carrier		-148.66		dBc/Hz
$\varphi_N(10M)$		10MHz Offset from Carrier		-152.86		dBc/Hz
$\varphi_N(\infty)$		Noise Floor ( $\geq 30$ MHz from Carrier)		-154.85		dBc/Hz
$\varphi_N(100k)$	RF Output Phase Noise Performance at 3.8GHz (Open Loop)	100kHz Offset from Carrier		-104.7		dBc/Hz
$\varphi_N(800k)$		800kHz Offset from Carrier		-128.95		dBc/Hz
$\varphi_N(1M)$		1MHz Offset from Carrier		-131.27		dBc/Hz
$\varphi_N(5M)$		5MHz Offset from Carrier		-146.09		dBc/Hz
$\varphi_N(10M)$		10MHz Offset from Carrier		-150.17		dBc/Hz
$\varphi_N(\infty)$		Noise Floor ( $\geq 30$ MHz from Carrier)		-154		dBc/Hz
$\varphi_N(100k)$	RF Output Phase Noise Performance at 4.4GHz (Open Loop)	100kHz Offset from Carrier		-101.72		dBc/Hz
$\varphi_N(800k)$		800kHz Offset from Carrier		-126.78		dBc/Hz
$\varphi_N(1M)$		1MHz Offset from Carrier		-129.23		dBc/Hz
$\varphi_N(5M)$		5MHz Offset from Carrier		-145.21		dBc/Hz
$\varphi_N(10M)$		10MHz Offset from Carrier		-149.97		dBc/Hz
$\varphi_N(\infty)$		Noise Floor ( $\geq 30$ MHz from Carrier)		-152.1		dBc/Hz
-	Spurious Signals Due to PFD Frequency	f <sub>PFD</sub> = 50MHz; RF_OUT <sub>A</sub> = 2.2GHz		-74		dBc

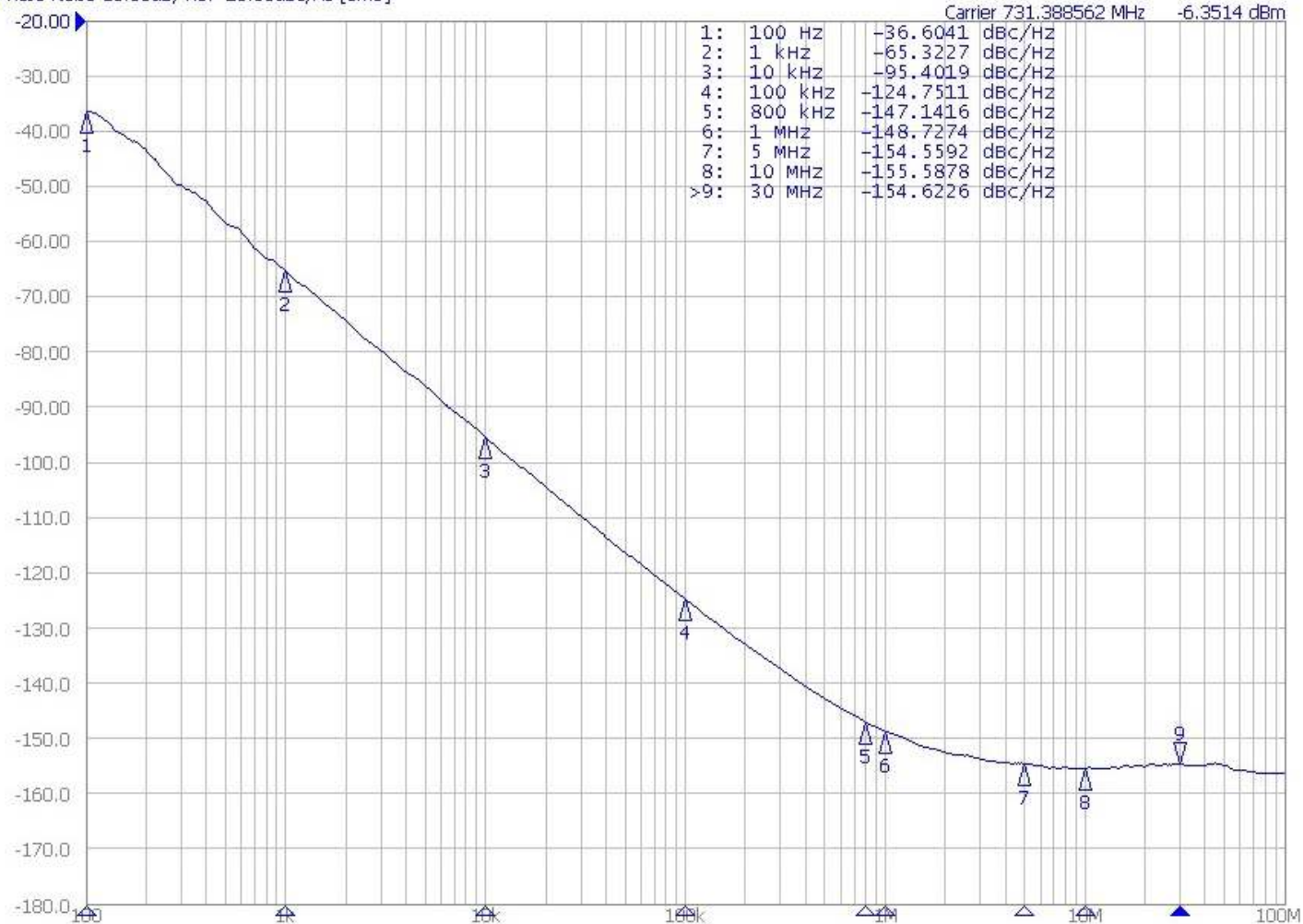
[a] V<sub>DDX</sub> denotes V<sub>DD</sub>, V<sub>CP</sub>, V<sub>DD\_SD</sub>, V<sub>VCO</sub>.

[b] RF\_OUT<sub>[A:B]</sub> output power setting = +2dBm.

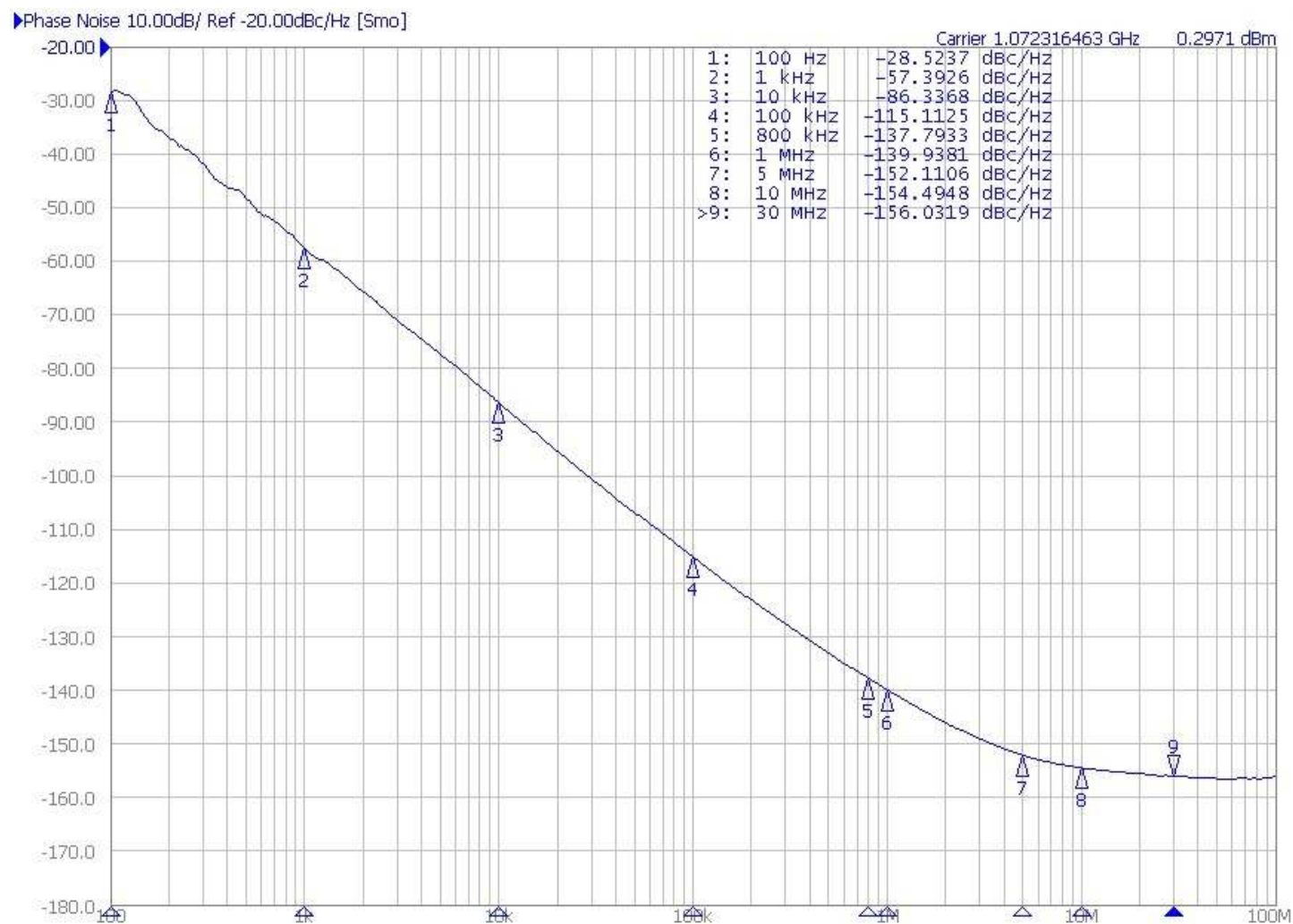
# Phase Noise (Open-Loop) at 730MHz (3.3V)

Phase Noise 10.00dB/ Ref -20.00dBc/Hz [Smo]

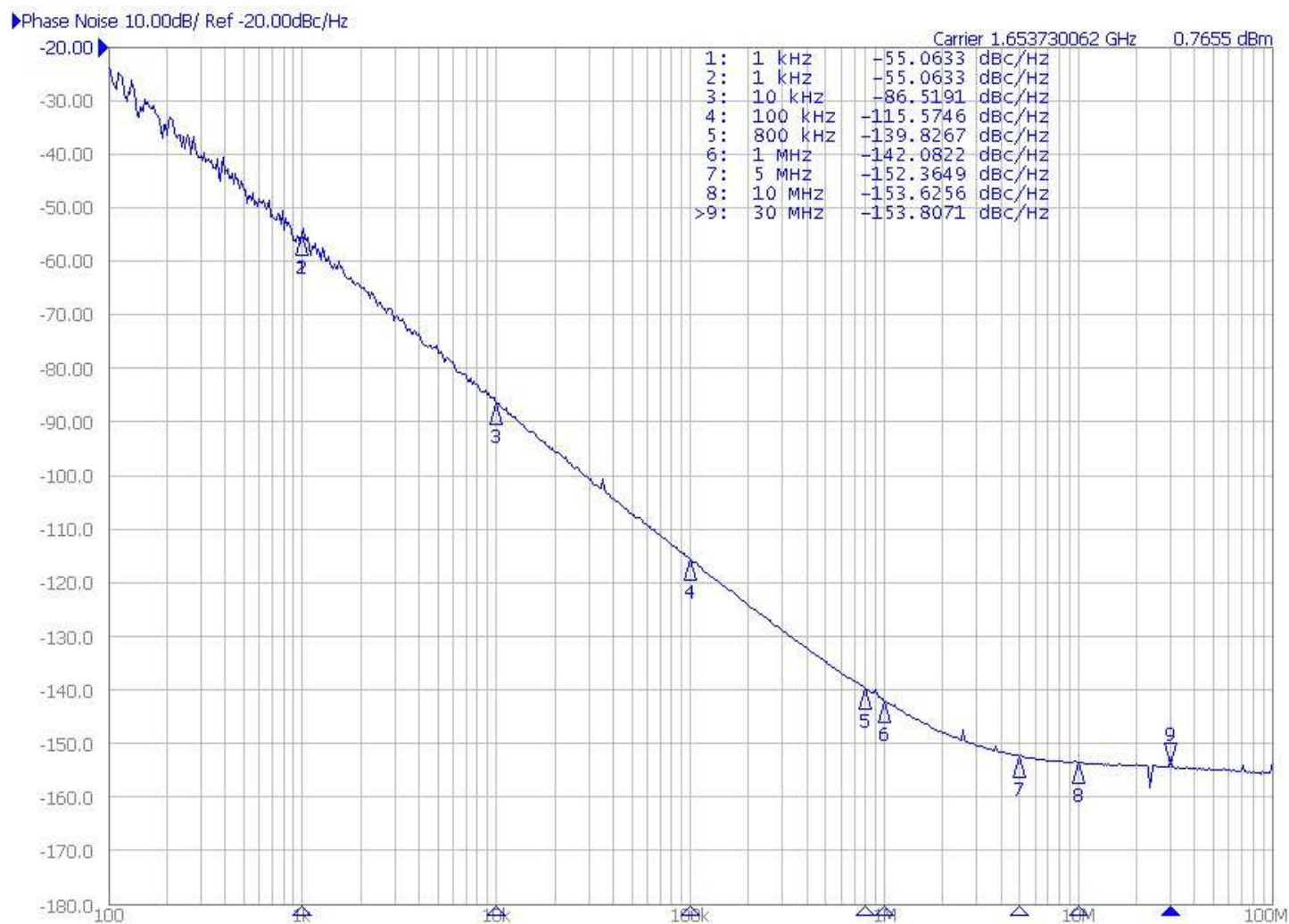
Carrier 731.388562 MHz -6.3514 dBm



# Phase Noise Performance (Open-Loop) at 1.1GHz (3.3V)



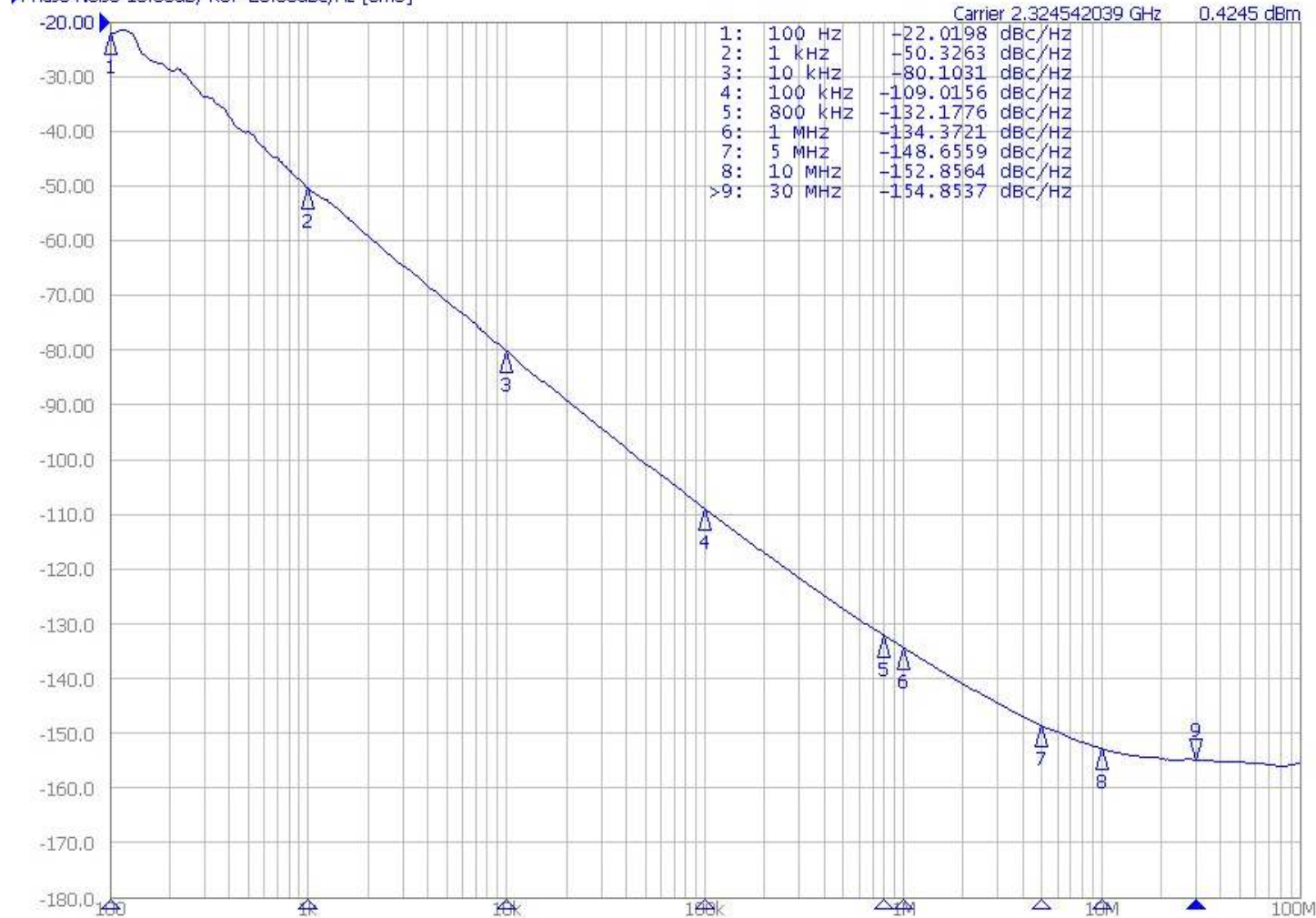
# Phase Noise Performance (Open-Loop) at 1.65GHz (3.3V)



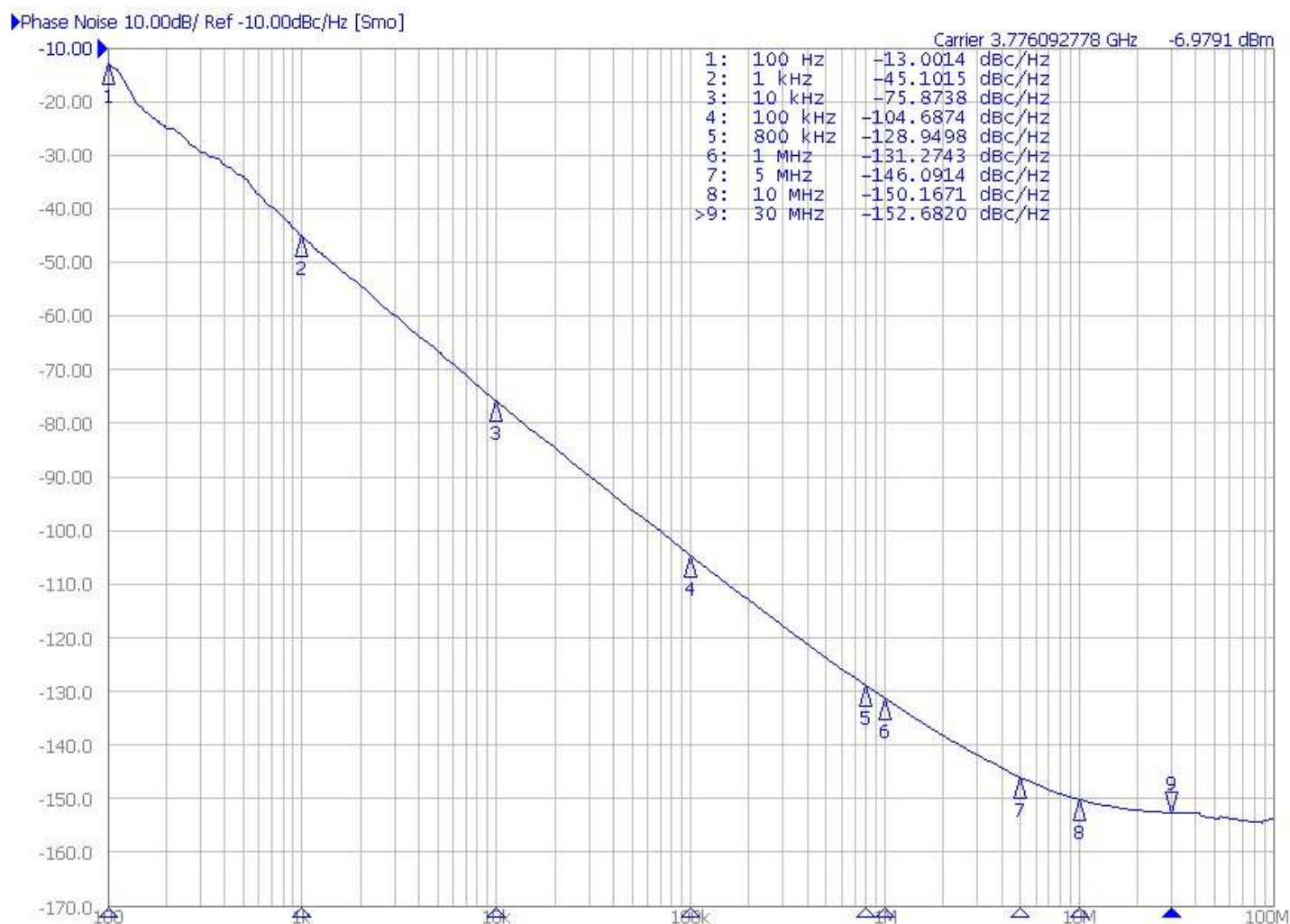
# Phase Noise Performance (Open-Loop) at 2.3GHz (3.3V)

Phase Noise 10.00dB/ Ref -20.00dBc/Hz [Smo]

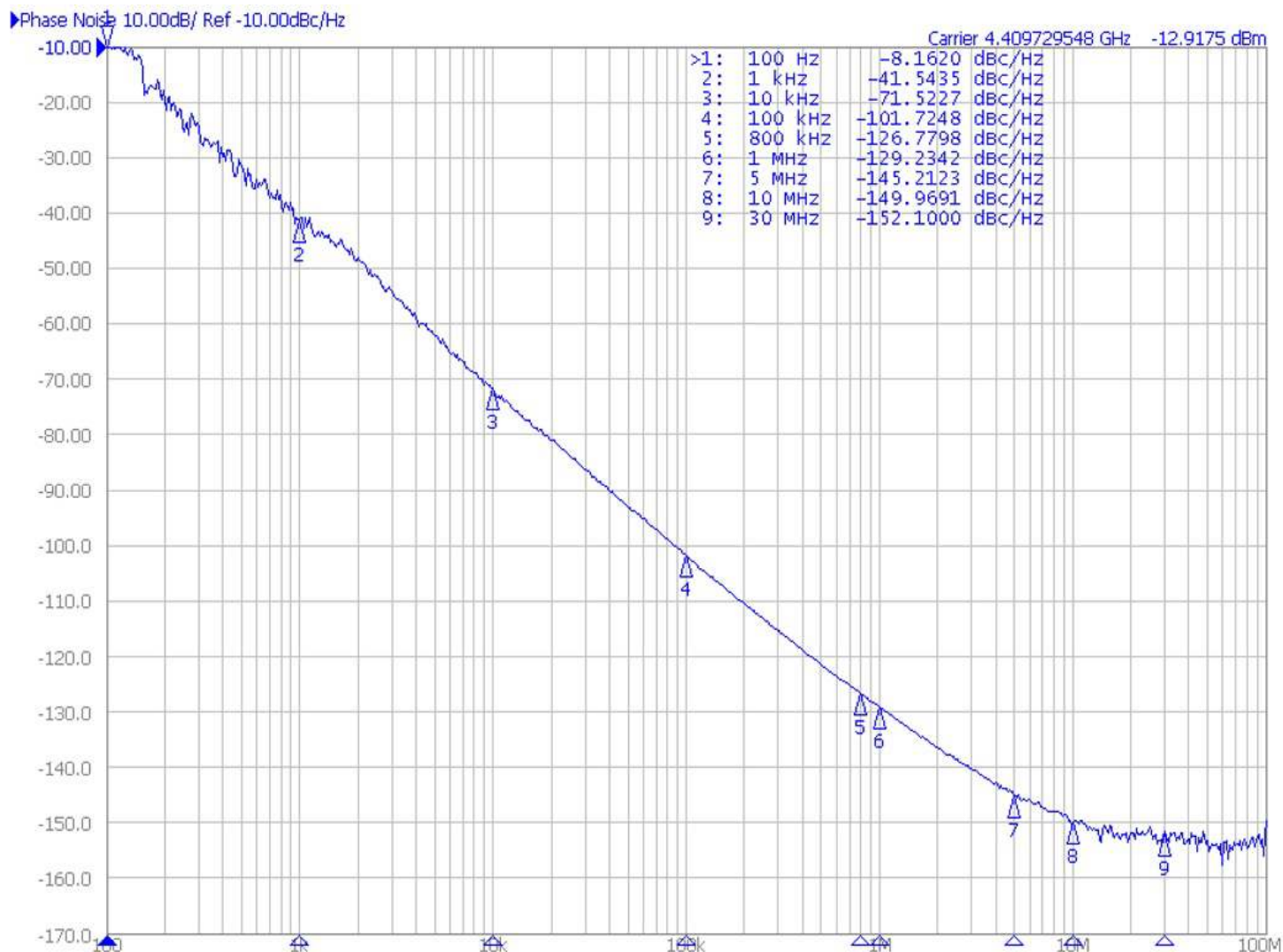
Carrier 2.324542039 GHz 0.4245 dBm



# Phase Noise Performance (Open-Loop) at 3.8GHz (3.3V)





**Phase Noise Performance (Open-Loop) at 4.4GHz (3.3V)**

## Principles of Operation

### Synthesizer Programming

The Fractional-N architecture is implemented via a cascaded programmable dual modulus prescaler. The N divider offers a division ratio in the feedback path of the PLL, and is given by programming the value of INT, FRAC and MOD in the following equation:

$$N = \text{INT} + \text{FRAC}/\text{MOD}(1)$$

**INT** is the divide ratio of the binary 16-bits counter (see [Table 18](#)).

**FRAC** is the numerator value of the fractional divide ratio. It is programmable from 0 to (MOD – 1). Refer to [Table 19](#) when in 12-bit mode, or [Table 83](#) when in 16-bit mode.

**MOD** is the 12-bit or 16-bit modulus. It is programmable from 2 to 4095 in 12-bit mode, and 2 to 65535 in 16-bit mode. Refer to [Table 24](#) when in 12-bit mode, or [Table 82](#) when in 16-bit mode.

The **VCO** frequency ( $f_{\text{VCO}}$ ) at RF\_OUT<sub>A</sub> or RF\_OUT<sub>B</sub> is given by the following equation:

$$f_{\text{VCO}} = f_{\text{PFD}} \times (\text{INT} + \text{FRAC}/\text{MOD})(2)$$

$f_{\text{PFD}}$  is the frequency at the input of the Phase and Frequency Detector (PFD).

The 8V97053 offers an Integer mode. To enable that mode, the user has to program the FRAC value to 0.

The device's VCO features three VCO band-splits to cover the entire range with sufficient margin for process, voltage, and temperature variations. These are automatically selected by invoking the Autocal feature. The charge pump current is also programmable via the ICP SETTING register for maximum flexibility.

Via [Register 4](#), one can enable RF\_OUT<sub>A</sub> or both outputs. Similarly, one can disable RF\_OUT<sub>B</sub> or both outputs.

### Reference Input Stage

The 8V97053 features one single-ended reference clock input (REF\_IN). This single-ended input can be driven by an ac-coupled sine wave or square wave.

In Power Down mode this input is set to High-Impedance to prevent loading of the reference source. The reference input signal path also includes an optional doubler.

### Reference Doubler

To improve the phase noise performance of the device, the reference doubler can be used. By using the doubler, the PFD frequency is also doubled and the phase noise performance typically improves by 3dB. When operating the device in Fractional mode, the speed of the Sigma Delta modulator of the N counter is limited to 125MHz, which is also the maximum PFD frequency that can be used in the fractional mode. When the part operates in Integer-N mode, the PFD frequency is limited to 310MHz.

1. The user has the possibility to select a higher PFD frequency (up to 310MHz in Integer mode) by doing the following steps using registers 6 and 7.
2. The user needs to increase the size of the Band Select Clock Divider (normally 8-bits) by setting the bit [D6:D3] in the Register 6 to divide down to a frequency lower than 500kHz and higher than 125kHz.

Use the Bit[D27:D26] to increase the lock detect precision for the faster PFD frequency.

The Lock Detect window should be set as large as possible but less than a period of the phase detector. The phase detector frequency should be greater than 500kHz.

**Table 11. Lock Detect Precision (LDP)**

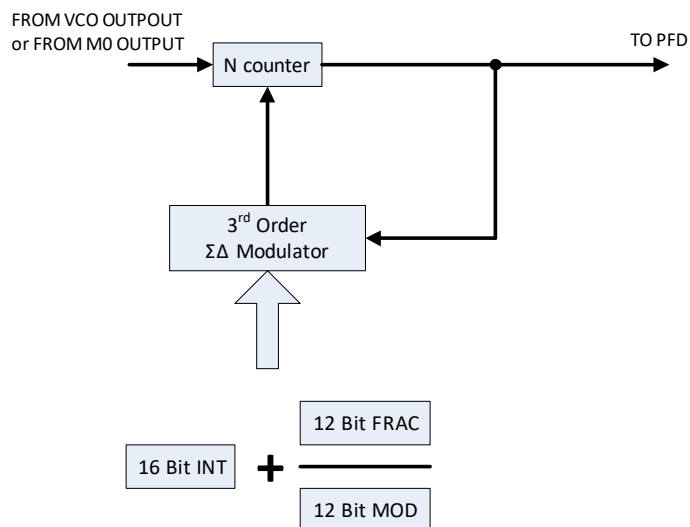
LDP_Ext2 (D27 of Register 6)	LDP_Ext1 (D26 of Register 6)	LDP (D7 of Register 2)	LDP value (ns)
0	0	0	10
0	0	1	6
Use of Register 6			
0	1	0	3
0	1	1	3
1	0	0	4
1	0	1	4.5
1	1	0	1.5
1	1	1	1.5

## Feedback Divider

The feedback divider N supports fractional division capability in the PLL feedback path. It consists in an integer N divider of 16 bits, and a Fractional divider of 12 bits (FRAC) over 12-bits (MOD). FRAC and MOD can be extended to 16 bits when using register 7.

To select an integer mode only, the user sets FRAC to 0.

**Figure 2. RF Feedback N Divider**



The 16 INT bits (Bit[D30:D15] in [Register 0](#)) set the integer part of the feedback division ratio.

The 12 FRAC bits (Bit[D14:D3] in [Register 1](#)) set the numerator of the fraction that goes into the Sigma Delta modulator. FRAC can be extended to 16 bits using the EXT\_FRAC bits in [Register 7](#).

The 12 MOD bits (Bit[D14:D3] in [Register 1](#)) set the denominator of the fraction that goes into the Sigma Delta modulator. MOD can be extended to 16 bits using the EXT\_MOD bits in [Register 7](#).

From the relation (2), the VCO minimum step frequency is determined by  $(1/\text{MOD}) * f_{\text{PFD}}$ .

FRAC values from 0 to (MOD – 1) cover channels over a frequency range equal to the PFD reference frequency.

The PFD frequency is calculated as follows:

(3)

$$f_{PFD} = REF_{CLK} \frac{1+D}{R}$$

Use 2R instead of R if the Reference Divide by 2 is used.

$REF_{CLK}$  = the input reference frequency (REF\_IN)

$D$  = the input reference doubler (0 if not active or 1 if active)

$R$  = the 10-Bits programmable input reference pre-divider

The programmable modulus (MOD) is determined based on the input reference frequency (REF\_IN) and the desired channelization (or output frequency resolution). The high resolution provided on the R counter and the Modulus allows the user to choose from several configuration (by using the doubler or not) of the PLL to achieve the same channelization. Using the doubler may offer better phase noise performance. The high resolution Modulus also allows to use the same input reference frequency to achieve different channelization requirements. Using a unique PFD frequency for several needed channelization requirements allows the user to design a loop filter for the different needed setups and ensure the stability of the loop.

The channelization is given by  $\frac{f_{PFD}}{MOD}$  (4)

In low noise mode (dither disabled), the Sigma Delta modulator can generate some fractional spurs that are due to the quantization noise.

The spurs are located at regular intervals equal to  $f_{PFD}/L$  where L is the repeat length of the code sequence in the Sigma Delta modulator. That repeat length depends on the MOD value, as described in [Table 12](#).

**Table 12. Fractional Spurs Due to the Quantization Noise**

Condition (Dither Disabled)	L	Spur Intervals
MOD can be divided by 2, but not by 3	$2 \times MOD$	$f_{PFD}/(2 \times MOD)$
MOD can be divided by 3, but not by 2	$3 \times MOD$	$f_{PFD}/(3 \times MOD)$
MOD can be divided by 6	$6 \times MOD$	$f_{PFD}/(6 \times MOD)$
Other conditions	MOD	$f_{PFD}/MOD$ (channel step)

In order to reduce the spurs, the user can enable the dither function to increase the repeat length of the code sequence in the Sigma Delta modulator. The increased repeat length is  $2^{21}$  cycles so that the resulting quantization error is spread to appear like broadband noise. As a result, the in-band phase noise may be degraded when using the dither function.

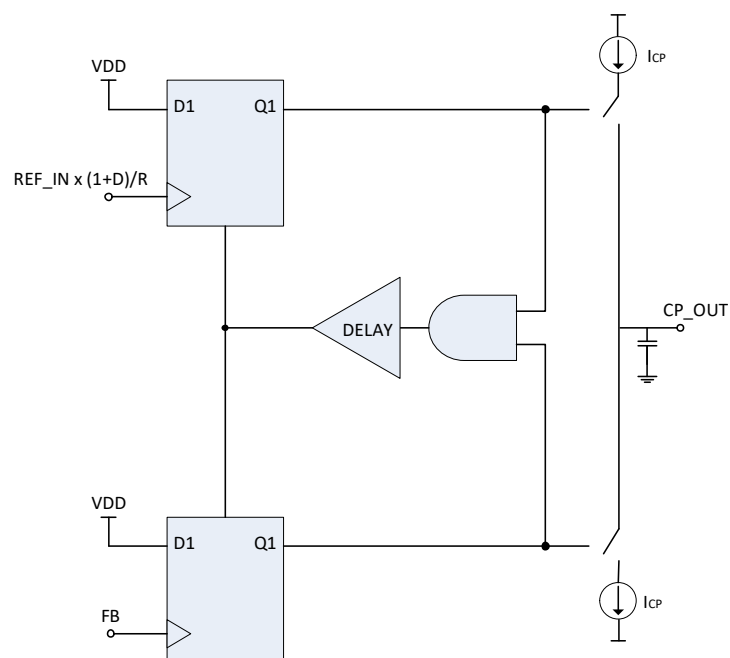
When the application requires the lowest possible phase noise and when the loop bandwidth is low enough to filter most of the undesirable spurs, or if the spurs won't affect the system performance, it is recommended to use the low noise mode with dither disabled.

## Phase and Frequency Detector (PFD) and Charge Pump

The phase detector compares the outputs from the R counter and from the N counter and generates an output corresponding to the phase and frequency difference between the two inputs the PFD. The charge pump current is programmable through the serial port (SPI) to several different levels.

The PFD offers an anti-backlash function that helps to avoid any dead zone in the PFD transfer function.

**Figure 3. Simplified PFD Circuit using D-type Flip-flop**



The Band Select logic operates between 125kHz and 500kHz. The Band Select clock divider needs to be set to divide down the PFD frequency to between 125kHz to 500kHz (logic maximum frequency).

## PFD Frequency

The VCO Band Selection can be used while operating at PFD frequencies up to 310MHz.

If the application requires the PFD frequency to be higher than 125MHz, the user can use one of the following two techniques (Technique A is the recommended procedure):

- Technique A – The user can use the ExtBndSelDiv[4:1] bits (Bits[D6:D3]) in [Register 6](#). These additional band select divider bits extend the band select divider from 8-bits (available in [Register 4](#)) to 12-bits. The four additional band select divider bits in Register 4 are the most significant bits of the divide value. For proper VCO band selection, the PFD frequency divided by the band select divide value must be  $\leq 500\text{kHz}$  and  $\geq 125\text{kHz}$ .
- Technique B – If choosing this second technique, the user must follow the three following steps:

Disable the Phase Adjust function by setting the bit D28 In Register 1 to 0, keep the PFD frequency lower than 125MHz, and program the desired VCO frequency.

Enable the phase adjust function by setting BAND\_SEL\_DISABLE (Bit D28 in [Register 1](#)) to 1.

Set the desired PFD frequency and program the relevant R divider and N counter values.

In either technique, the Lock Detect Precision should be programmed to be lower than the PFD period using the bit [D7] in [Register 2](#) and the bits [D27:D26] in [Register 6](#) (see [Table 11](#)).

## External Loop Filter

The 8V97053 requires an external loop filter. The design of that filter is application specific. For additional information, refer to the [Applications Information](#).

## Phase Detector Polarity

The phase detector polarity is set by bit D6 in [Register 2](#). This bit should be set to 1 when using a passive loop filter or a non-inverting active loop filter. If an inverting active filter is used, this bit should be set to 0.

## Charge Pump High-Impedance

In order to put the charge pump into three-state mode, the user must set the bit D4 [CP HIGHZ] in [Register 2](#) to [Register 1](#). This bit should be set to 0 for normal operation.

## Integrated Low Noise VCO

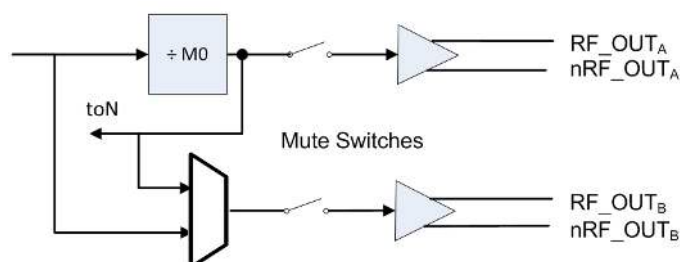
The VCO function of the 8V97053 consists in three separate VCOs. This allows keeping narrow tuning ranges for the VCOs while offering a large frequency tuning range for VCO core. Keeping narrow VCO tuning ranges allows for lower VCO sensitivity ( $K_{VCO}$ ), which results in the best possible VCO phase noise and spurious performance.

The user does not have to select the different VCO bands. The VCO band select logic of the 8V97053 will automatically select the most suitable band of operation at power up or when [Register 0](#) is written.

## Output Clock Distribution

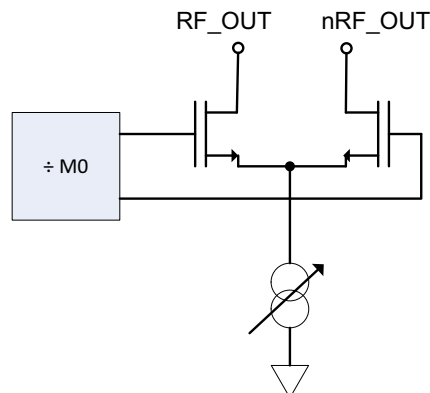
The 8V97053 device provides two outputs. These two outputs can generate the same frequency ( $f_{VCO} / M0$ ) or two integer related different frequencies (in this case, RF\_OUT<sub>B</sub> would generate a frequency equal to the VCO frequency and RF\_OUT<sub>A</sub> would generate  $f_{VCO} / M0$ ).

**Figure 4. Output Clock Distribution**



RF\_OUT and nRF\_OUT are derived from the drain of an NMOS differential pair driven by the VCO output (or by the M0 Divider), as shown in [Figure 5](#).

**Figure 5. Output Stage**



Eight programmable output power levels can be programmed from -4dBm to +7dBm (see [RF Output Power](#)).

The 8V97053 offers an auxiliary output (RF\_OUT<sub>B</sub>). If the auxiliary output stage is not used, it can be powered down by using the RF\_OutB\_En bit in [Register 4](#).

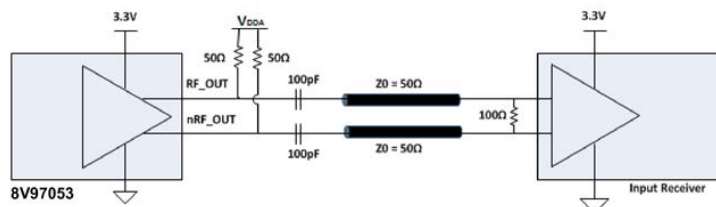
The supply current to the output stage can be shut down until the part achieves lock. To enable this mode, the user will set the MTLD bit in [Register 4](#). The MUTE pin can be used to mute all outputs and be used as a similar function.

## Output Matching

The outputs of the 8V97053 are Open Drain Output and can be matched in different ways.

A simple broadband matching is to terminate the open drain RF\_OUT output with, for example, a 50Ω to V<sub>DDA</sub>, and with an AC coupling capacitor in series. An example of this termination scheme is shown on [Figure 6](#).

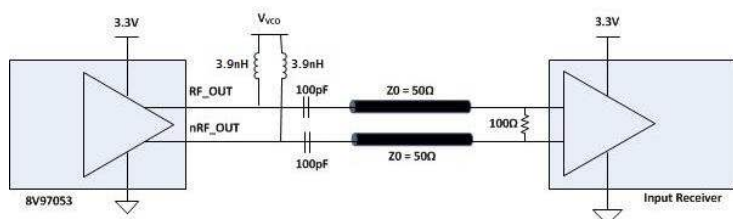
**Figure 6. Broadband Matching Termination**



This termination scheme allows to provide one of the selected output power on the differential pair when connected to a 50Ω load. (See the [RF Output Power](#) for more information about the output power selection).

The 50Ω resistor connected to V<sub>DDA</sub> can also be replaced by a choke, for better performance and optimal power transmission.

**Figure 7. Optimal Matching Termination**



The pull up inductor value is frequency dependent. For impedance of 50Ω pull-up, the inductance value can be calculated as  $L = 50 / (2 \cdot 3.14 \cdot F)$ , where F is operating frequency. In this example, L = 3.9nH is for an operating frequency of approximately 2GHz.

For more recommendations on the termination scheme, see [Applications Information](#).

## Band Selection Disable

For a given frequency, the output phase can be adjusted when using the Band\_Sel\_Disable bit (Bit D28 in [Register 1](#)). When this bit is enabled (Bit D28 set to 1), the part does not do a VCO band selection or phase resync after an update to [Register 0](#).

When the Band\_Sel\_Disable bit is set to 0, and when [Register 0](#) is updated, the part proceeds to a VCO band selection, and to a phase resync if phase\_resync is also enabled in [Register 3](#) (Bits[D16:D15] set to D16 = 1 and D15 = 0).

The “Band\_Sel\_Disable” bit is useful when the user wants to make small changes in the output frequency (<1MHz from the nominal frequency) without recalibrating the VCO and minimizing the settling time.

## Phase Adjust

The output phase is controlled by the 12-bit phase value Bits[D26:D15] in [Register 1](#). The output phase can vary over 360° with a 360°/MOD step. For dynamic adjustments of the phase after an initial phase setting, it is recommended to select the BAND\_SEL\_DISABLE function by setting the Band\_Sel\_Disable bit (D28 in [Register 1](#)) to 1.

## Phase Resync

The phase alignment function operates based on adjusting the “fractional” phase, so the phase can settle to any one of the MOD phase offsets, MOD being the modulus of the fractional feedback divider.

The phase adjustment can provide a 0-360° of phase adjust, assuming that the output divider ratio is set to 1.

The phase step is TVCO/MOD for the normal case of fundamental feedback. TVCO is the period of the VCO.

The feedback select bit (FbkSel bit, Bit D23 in [Register 4](#)) gives the choices of fundamental feedback or divided feedback. This bit controls the mux that sends the VCO signal or the output divider signal to the feedback loop. The user can get larger phase steps in the divided mode, but the phase noise may be degraded, especially in fractional mode. Should the user select this option, the phase adjustment step would be  $\sim T_{OUT}/MOD$ , where  $T_{OUT}$  is the output signal period.

When the part is in fractional mode, the device is dithering the feedback divider value. As an example, when using a 4GHz VCO frequency, the feedback divider value may dither between Div-by-20 and Div-by-21. Since the period is 250ps, there will be 250ps of jitter added to the phase detector. This jitter is filtered by the loop, but can still show up at the output if the loop bandwidth is high. When using a divider before the feedback divider, the effective VCO period is increased. If a Div-by-64 is used for example, the period becomes  $64 \times 250ps = 16ns$ . This means that there could be an additional 16ns of jitter at the PFD, rather than 250ps. It is more challenging for the loop to filter this larger amount of jitter and this will degrade the overall performance of the part, unless the user chooses to use a very low loop bandwidth. With normal loop bandwidth configurations (for optimal noise), the phase noise would be degraded when using a divided feedback mode.

The Phase Resync is controlled by setting Bits[D16:D15] in [Register 3](#) to D16 = 1 and D15 = 0. When phase resync is used, an internal timer generates sync signals every  $T_{SYNC}$  where:

$$T_{SYNC} = ClkDiv \times MOD \times T_{PFD} \quad (5)$$

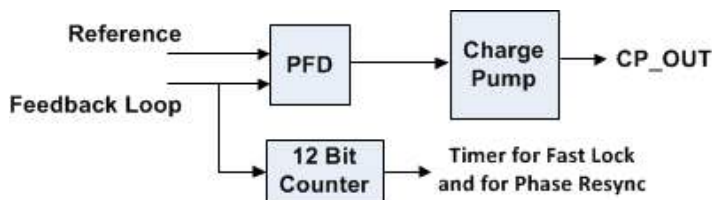
**ClkDiv** = the value (from 1 and 4095) programmed in the 12-bit clock counter in Bits[D14:D3] in [Register 4](#). The 12-bit counter is used as a timer for Fast Lock and for the Phase Resync function.

**MOD** = the Modulus value (Bits[D14:D3] of [Register 1](#))

**$T_{PFD}$**  = the PFD period

In *Equation 5*, the minimum of either MOD value or 4095 is used for calculating  $T_{SYNC}$  when in 16-bit mode.



**Figure 8. 12-bit Counter for Fast Lock and Phase Resync**


After the user program a frequency, the second sync pulse coming from the 12-bit counter, after the nCS is asserted high, is used to resynchronize the output phase to the input phase. To ensure that the PLL is locked before to resynchronize the output phase, TSYNC must be larger than the worst case lock time.

## Fast Lock Function

The device uses a fast-lock mode to decrease lock time.

In order to allow the Fast Lock mode, the Fast Lock Switch (FLSW) is shorted to Ground and the charge pump current (ICP) is changed temporarily until the Fast Lock mode is disabled.

The loop bandwidth needs to be increased temporarily in order to allow a faster lock time. By doing this, the loop filter needs to be initially designed so that it addresses the risk of instability of having the zero and the poles too close to the actual bandwidth knee, when the user switches to a fast lock mode.

The loop bandwidth is proportional to:

$$RS \text{ and } ICP \text{ (BW} \sim RS * ICP \text{)}$$

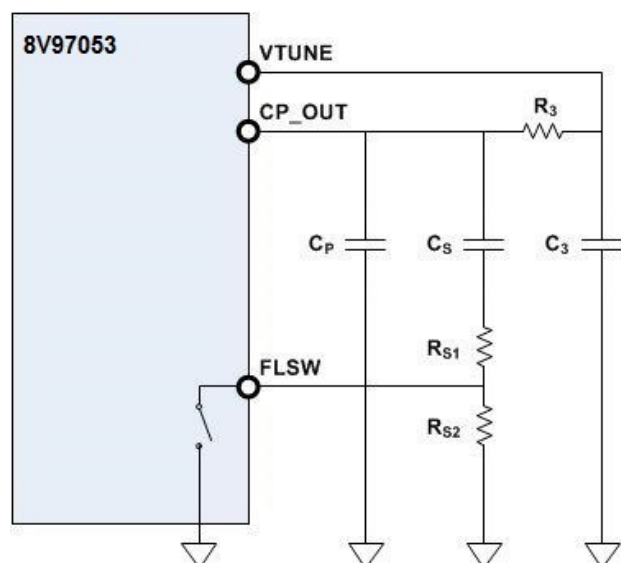
Where:

BW = The loop bandwidth

RS = The damping resistor

ICP = The programmable charge pump current

In order to enable the fast lock mode, the charge pump current is increased to the maximum value in order to increase the loop bandwidth. In parallel, the FLSW filter is set to ON so that the RS value is  $\frac{1}{4}$  of its initial value in order to maintain the loop stability. By doing so, the zero and the first pole are moved (by a factor of 4x in the example below), so that the zero and the pole are kept at a suitable distance around the loop bandwidth.

**Figure 9. Example of Fast Lock Mode Loop Filter Topology**


In the example of [Figure 9](#), the damping resistor RS is equal to:  
 $RS1 + RS2$  in normal mode (FSLW switch OFF), with  $RS2 = 3 * RS1$

When the FLSW switch is ON, the damping resistor value is reduced by  $\frac{1}{4}$  of its initial value ( $RS = RS1$ ).

The second pole defined by R3 and C3 need needs to be designed so that there is no risk of instability when widening the loop bandwidth.

## RF Output Power

For RF\_OUT<sub>A</sub> and RF\_OUT<sub>B</sub>, the output power can be programmed from -4dBm to +7dBm. Refer to [Table 50](#), [Table 52](#), [Table 61](#) and [Table 62](#) in the [Register Map](#) section for more information.

## MUX\_OUT

MUX\_OUT is a multipurpose output that can be programmed to provide the user with some internal status and values for test and debugging purpose. In addition, MUX\_OUT can also be programmed to provide an additional Serial Data Out Pin for a 4-wire SPI interface when needed. The MUX\_OUT function is described in the [Table 13](#) and can be programmed in Bits[D28:D26] in [Register 2](#).

**Table 13. MUX\_OUT Pin Configuration**

MUX_OUT Register Value	MUX_OUT Function
000	High-Impedance Output
001	V <sub>DDD</sub>
010	GNDD
011	R Counter Output
100	N counter Output
101	Reserved
110	Lock Detect
111	MUX_OUT configured as SDO

## Power-Down Mode

When power-down is activated, the following events occur:

1. Counters are forced to their load state conditions
2. VCO is powered down
3. Charge pump is forced into three-state mode
4. Digital lock detect circuitry is reset
5. RF\_OUT buffers are disabled
6. The input stage is powered down and set to High-Impedance
7. Input registers remain active and capable of loading and latching data

## Default Power-Up Conditions

All the RF outputs are muted at power up until the loop is locked. For default values in registers, see [the Register Map](#).

## Program Modes

Table 14 and the Register Map indicate how the program modes are set up in the 8V97053.

**Table 14. Control Bits Configuration**

Control Bits (CB)			Register
C3	C2	C1	
0	0	0	Register 0
0	0	1	Register 1
0	1	0	Register 2
0	1	1	Register 3
1	0	0	Register 4
1	0	1	Register 5
1	1	0	Register 6
1	1	1	Register 7

## Double Buffering

The following bits are Doubled Buffered:

1. PHASE (Bits[D26:D15] in Register 1)
2. MOD (Bits[D14:D3] in Register 1)
3. REF DOUBLER (Bit D25 in Register 2)
4. REF DIV2 (Bit D24 in Register 2)
5. R COUNTER (Bits[D23:D14] in Register 2)
6. ICP SETTING (Bits[D12:D9] in Register 2)

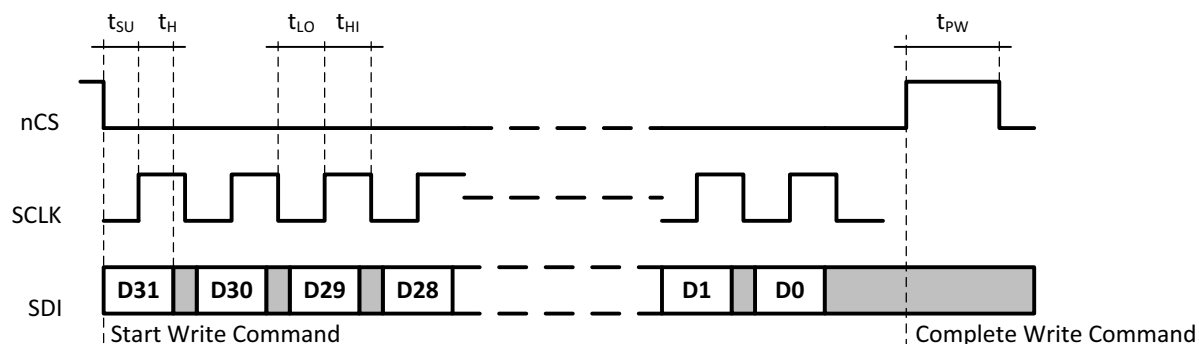
The user must proceed to the following steps before any value written in these bits are used.

1. The new values are written in the double buffered bits
2. A new Write is performed on Register 0

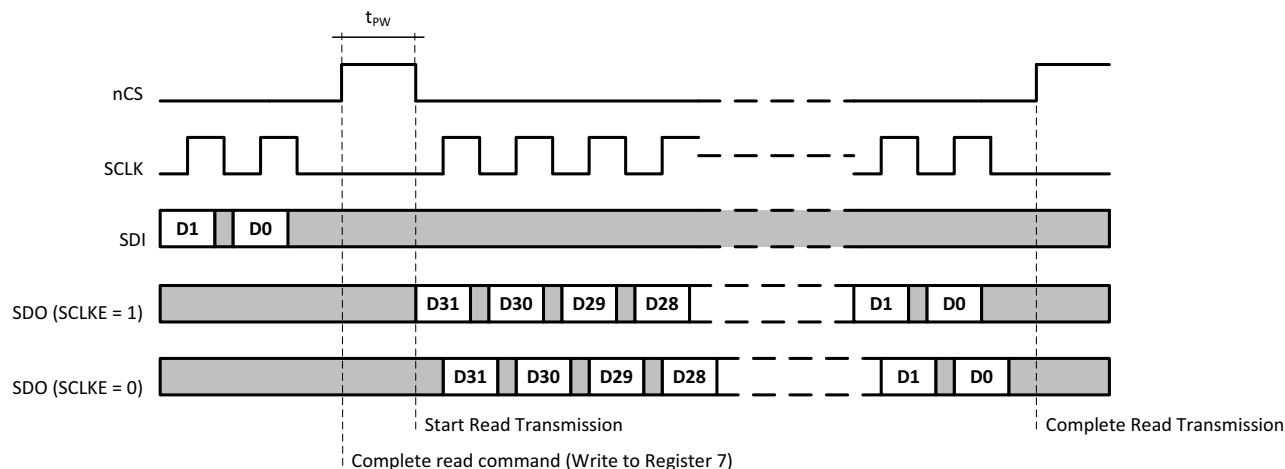
The RF DIVIDER value in Register 4 (Bits[D22:D20]) is also double buffered, but only if the DOUBLE BUFFER bit (Bit D13 in Register 2) is set to 1.

# Timing Characteristics

**Figure 10. SPI Write Cycle Timing Diagram**



**Figure 11. SPI Read Cycle Timing Diagram**



**Table 15. SPI Read / Write Cycle Timing Parameters**

Symbol	Parameter	Minimum	Maximum	Unit
$f_{CLK}$	SCLK Frequency		20	MHz
$t_{SU}$	nCS, SDI Setup Time to SCLK	10		ns
$t_H$	SCLK to nCS, SDI Hold Time	10		ns
$t_{LO}$	SCLK Low Pulse Width	25		ns
$t_{HI}$	SCLK High Pulse Width	25		ns
$t_{PW}$	nCS De-asserted Pulse Width	20		ns

### 3- or 4-Wire SPI Interface Description

The 8V97053 has a serial control port capable of responding as a slave in an SPI compatible configuration to allow access to any of the internal registers (see [Register Map](#)) for device programming or examination of internal status. See the specific sections for each register for details on meanings and default conditions.

SPI mode slave operation requires that a device external to the 8V97053 has performed any necessary serial bus arbitration and/or address decoding at the level of the board or system. The 8V97053 begins a cycle by detecting an asserted (low) state on the nCS input at a rising edge of SCLK. This is also coincident with the first bit of data being shifted into the device. In SPI mode, the first bit is the Most Significant Bit (MSB) of the data word being written. Data must be written in 32-bit words, with nCS remaining asserted and one data bit being shifted in to the 8V97053 on every rising edge of SCLK. If nCS is de-asserted (high) at any time except after the complete 32<sup>nd</sup> SCLK cycle, this is treated as an error and the shift register contents are discarded. No data is written to any internal registers. If nCS is de-asserted (high) as expected at a time at least  $t_{SU}$  after the 32<sup>nd</sup> falling edge of SCLK, then this will result in the shift register contents being acted on according to the control bit in it.

It is recommended to write the registers in reverse sequential order, starting with the highest register number first and ending with Register 0.

The word format of the 32-bit quantity in the shift register is shown in [Table 16](#). The register fields in the 8V97053 have been organized so that the three LSBs in each 32-bit register row are not used for data transfer. These bits will represent the base address for the 32-bit register row.

**Table 16. SPI Mode Serial Word Structure**

	MSB							LSB
Bit #	31	...	5	4	3	2	1	0
Meaning	D[31:3]						Control Bits	
Width	29						3	

To perform a register Read, the user needs set the MUX\_OUT bits (Bits[28:D26]) in Register 2 to 111 to configure the MUX\_OUT pin as SDO. Register 7 (Instruction register) needs to be set for Read operation. Bit D3 of Register 7 will set the Read or Write command, and Bits[D4:D6] determine the read back address.

If a read operation is requested, 32-bits of read data will be provided in the immediately subsequent access. nCS must be de-asserted (high) for at least  $t_{PW}$ , and then reasserted (low).

If SCLKE = 1 (default condition), one data bit will be transmitted on the SDO output at the falling edge of nCS and each falling edge of SCLK as long as nCS remains asserted (low), and the master device should capture data on the rising edge of SCLK. If SCLKE = 0, one data bit will be transmitted on the SDO output at each rising edge of SCLK as long as nCS remains asserted (low), and the master device should capture data on the falling edge of SCLK.

If nCS is de-asserted (high) before 32-bits of read data have been shifted out, the read cycle will be considered to be completed. If nCS remains asserted (low) longer than 32-bit times, then the data during those extra clock periods will be undefined. The MSB of the data will be presented first.

# Register Map

## Register 0

**Table 17. Register 0 Bit Allocation**

DESCRIPTION	NAME	BITS
	RESERVED	D31
FEEDBACK DIVIDER INTEGER VALUE (INT)	NDiv16	D30
	NDiv15	D29
	NDiv14	D28
	NDiv13	D27
	NDiv12	D26
	NDiv11	D25
	NDiv10	D24
	NDiv9	D23
	NDiv8	D22
	NDiv7	D21
	NDiv6	D20
	NDiv5	D19
	NDiv4	D18
	NDiv3	D17
	NDiv2	D16
	NDiv1	D15
FEEDBACK DIVIDER FRACTIONAL VALUE (FRAC)	FDiv12	D14
	FDiv11	D13
	FDiv10	D12
	FDiv9	D11
	FDiv8	D10
	FDiv7	D9
	FDiv6	D8
	FDiv5	D7
	FDiv4	D6
	FDiv3	D5
	FDiv2	D4
	FDiv1	D3
CONTROL BITS	CB3	D2
	CB2	D1
	CB1	D0

**Table 18. Register 0: 16-Bit Feedback Divider Integer Value (INT). Function Description**

Name	Description	Factory Default	Function
NDiv[16:1]	Feedback Divider Integer Value (INT)	0000 0000 0110 0100 (INT = 100)	0000 0000 0000 0000 = Not allowed 0000 0000 0000 0001 = Not allowed ... 0000 0000 0000 0111 = Not allowed 0000 0000 0000 1000 = 8 ... 0000 0000 0001 0111 = 23 0000 0000 0001 1000 = 24 ... 1111 1111 1111 1111 = 65,535

**Table 19. Register 0: 12-Bit Feedback Divider Fractional Value (FRAC). Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function
FDiv[12:1]	Feedback Divider Fractional Value (FRAC)	0000 0000 0000 (FRAC = 0)	0000 0000 0000 = 0 0000 0000 0001 = 1 ... 1111 1111 1111 = 4095

[a] This table is used when bit 16b\_12b\_sel is set to 0 (default). If the 16b\_12b\_sel is set to 1, refer to [Table 83](#).

**Table 20. Register 0: 3-Bit Control Bits. Function Description<sup>[a]</sup>**

Name	Description	Factory Default
CB[3:1]	Control Bits	000 = Register 0 is programmed

[a] The user has to set CB[3:1] to 000 in order to write to Register 0.

## Register 1

**Table 21. Register 1 Bit Allocation**

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Reserved	Reserved	Reserved	Band_Sel_Disable	Unused	Phase12	Phase11	Phase10	Phase9	Phase8	Phase7	Phase6	Phase5	Phase4	Phase3	Phase2	Phase1	Mod12	Mod11	Mod10	Mod9	Mod8	Mod7	Mod6	Mod5	Mod4	Mod3	Mod2	Mod1	CB3	CB2	CB1
DESCRIPTION	RESERVED			BAND_SEL_DISABLE	UNUSED	PHASE VALUE (PHASE)												MODULUS VALUE (MOD)												CONTROL BITS		

**Table 22. Register 1: 1-Bit BAND\_SEL\_DISABLE. Function Description**

Name	Description	Factory Default	Function
Band_Sel_Disable	BAND_SEL_DISABLE	0	0 = VCO Band Selection occurs after a Write to Register 0 1 = VCO Band selection is not active and hold to previous VCO band selection

**Table 23. Register 1: 12-Bit Phase Value (PHASE). Function Description**

Name	Description	16b_12b_sel (Bit D20, Register7)	Factory Default	Function
Phase [12:1]	PHASE	0	0000 0000 0001	0000 0000 0000 = 0
				0000 0000 0001 = 1
				.....
				1111 1111 1111 = 4095
		1	0000 0000 0001	0000 0000 0000 = 0
				0000 0000 0001 = 16
				.....
				1111 1111 1111 = 65520

**Table 24. Register 1: 12-Bit Modulus Value (MOD). Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function
Mod[12:1]	MOD	0000 0000 0010	0000 0000 0000 = Not Allowed 0000 0000 0001 = Not Allowed 0000 0000 0010 = 2 ... 1111 1111 1111 = 4095

[a] This table is used when bit D20 in Register 7 (16b\_12B\_sel) is set to 0 (default). If 16b\_12b\_sel is set to 1, refer to [Table 82](#).

**Table 25. Register 1: 3-Bit Control Bits. Function Description<sup>[a]</sup>**

Name	Description	Function
CB[3:1]	Control Bits	001 = Register 1 is programmed

[a] The user has to set CB[3:1] to 001 in order to write to Register 1.



## Register 2

**Table 26. Register 2 Bit Allocation**

DESCRIPTION	NAME	BITS	
RESERVED	RESERVED	D31	
NOISE MODE	ModeNoise1	D30	
	ModeNoise2	D29	
MUX_OUT	MUX_OUT3	D28	
	MUX_OUT2	D27	
	MUX_OUT1	D26	
	RefDoub	D25	
REF DOUBLER	RDiv2	D24	
R COUNTER	R10	D23	
	R9	D22	
	R8	D21	
	R7	D20	
	R6	D19	
	R5	D18	
	R4	D17	
	R3	D16	
	R2	D15	
	R1	D14	
	DOUBLE BUFFER	DoubBuff1	D13
	ICP SETTING	ChrgPmp4	D12
		ChrgPmp3	D11
		ChrgPmp2	D10
ChrgPmp1		D9	
LDF	LDF	D8	
LDP	LDP	D7	
PD POLARITY	PD_pol	D6	
POWER DOWN	PwrDwn	D5	
CP HIGHZ	CP_HIGHZ	D4	
UNUSED	Unused	D3	
CONTROL BITS	CB3	D2	
	CB2	D1	
	CB1	D0	

**Table 27. Register 2: 2-Bit NOISE MODE. Function Description**

Name	Description	Factory Default	Function
ModeNoise[2:1]	NOISE MODE	00	00 = Low Noise Mode (Dither OFF) 01 = Reserved 10 = Reserved 11 = Low Spur Mode (Dither Enabled)

**Table 28. Register 2: 3-Bit MUX\_OUT. Function Description**

Name	Description	Factory Default	Function
MUX_OUT[3:1]	MUX_OUT	000	000 = High-Impedance output 001 = V <sub>DD</sub> 010 = GNDD 011 = R counter output 100 = N counter output 101 = Reserved 110 = Lock Detect 111 = MUX_OUT configured as SDO

**Table 29. Register 2: 1-Bit REF DIV2. Function Description**

Name	Description	Factory Default	Function
RDiv2	REF DIV2	0	0 = Disabled 1 = Enabled

**Table 30. Register 2: 10-Bit R COUNTER (R). Function Description**

Name	Description	Factory Default	Function
R[10:1]	R	00 0000 0001	00 0000 0000 = Not Allowed 00 0000 0001 = 1 00 0000 0010 = 2 ... 11 1111 1111 = 1023

**Table 31. Register 2: 1-Bit DOUBLE BUFFER. Function Description**<sup>[a]</sup>

Name	Description	Factory Default	Function
DoubBuff1	DOUBLE BUFFER	0	0 = Disabled 1 = Enabled

[a] Bit D13 enables or disables Double Buffering of Bits[D22:D20] in Register 4. Refer to [Program Modes](#).

**Table 32. Register 2: 1-Bit Lock Detect Function (LDF). Function Description**<sup>[a]</sup>

Name	Description	Factory Default	Function
LDF	LDF	0	0 = 40 consecutive cycles (recommended for FRAC-N mode) 1 = 5 consecutive cycles (recommended for INT-N mode)

[a] LDF controls the number of PFD cycles that needs to be considered by the Lock Detect function to decide if the part has achieved lock.

**Table 33. Register 2: 1-Bit Lock Detect Precision. Function Description**

Name	Description	Factory Default	Function
LDP	LDP	0	0 = 10ns 1 = 6ns

**Table 34. Register 2: 1-Bit Phase Detector Polarity. Function Description**

Name	Description	Factory Default	Function
PD_Pol	PD POLARITY	1	0 = Negative 1 = Positive

**Table 35. Register 2: 1-Bit Charge Pump High-Impedance. Function Description**

Name	Description	Factory Default	Function
CP_HIGHZ	CP HIGHZ	0	0 = Disabled 1 = Enabled

**Table 36. Register 2: 3-Bit Control Bits. Function Description<sup>[a]</sup>**

Name	Description	Function
CB[3:1]	Control Bits	010 = Register 2 is programmed

[a] The user has to set CB[3:1] to 010 in order to write to Register 2.

## Register 3

**Table 37. Register 3 Bit Allocation**

DESCRIPTION	NAME	BITS	
RESERVED	RESERVED	D31	
	RESERVED	D30	
	RESERVED	D29	
	RESERVED	D28	
	RESERVED	D27	
	RESERVED	D26	
	RESERVED	D25	
	RESERVED	D24	
	BAND SELECT	BandSelCM	D23
UNUSED	Unused	D22	
UNUSED	Unused	D21	
RESERVED	RESERVED	D20	
	RESERVED	D19	
UNUSED	Unused	D18	
	RESERVED	D17	
CLK DIV MODE	ClkDivMode2	D16	
	ClkDivMode1	D15	
CLOCK COUNTER VALUE	ClkDiv12	D14	
	ClkDiv11	D13	
	ClkDiv10	D12	
	ClkDiv9	D11	
	ClkDiv8	D10	
	ClkDiv7	D9	
	ClkDiv6	D8	
	ClkDiv5	D7	
	ClkDiv4	D6	
	ClkDiv3	D5	
	ClkDiv2	D4	
	ClkDiv1	D3	
	CONTRO L BITS	CB3	D2
		CB2	D1
CB1		D0	

**Table 38. Register 3: 1-Bit Band Select Clock Mode. Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function
BandSelCM	BAND SELECT (CLOCK RATE)	0	0 = LOW (125kHz) 1 = HIGH (up to 500kHz logic sequence for Faster Lock applications)

[a] BAND SELECT (CLOCK RATE) selects the speed of the logic sequence for the band selection. BandSelCM = 1 sets the logic sequence rate faster, which is recommended for fast lock operation and when high PFD frequencies are used. BandSelCM = 0 is recommended when low PFD frequencies (125kHz) are used. When using BandSelCM = 1, the value of the BAND SELECT CLOCK COUNTER (BndSelDiv[8:1]) must be less than or equal to 254.

**Table 39. Register 3: 2-Bit Clock Divider Mode. Function Description**

Name	Description	Factory Default	Function
ClkDivMode[2:1]	CLK DIV MODE	00	00 = Clock Divider OFF 01 = Fast Lock Enabled 10 = Resync Enabled 11 = Reserved

**Table 40. Register 3: 12-Bit Clock Divider Value (CLKDIV). Function Description**

Name	Description	Factory Default	Function
ClkDiv[12:1]	CLKDIV	0000 0000 0001	0000 0000 0000 = Not allowed 0000 0000 0001 = 1 0000 0000 0010 = 2 ... 1111 1111 1111 = 4095

**Table 41. Register 3: 3-Bit Control Bits. Function Description**<sup>[a]</sup>

Name	Description	Function
CB[3:1]	CONTROL BITS	011 = Register 3 is programmed

[a] The user has to set CB[3:1] to 011 in order to write to Register 3.

## Register 4

**Table 42. Register 4 Bit Allocation**

DESCRIPTION	NAME	BITS
RESERVED	RESERVED	D31
	RESERVED	D30
	RESERVED	D29
	RESERVED	D28
	RESERVED	D27
	RESERVED	D26
	RESERVED	D25
	RESERVED	D24
FEEDBACK SELECT	FbkSel	D23
RF DIVIDER	RFDiv3	D22
	RFDiv2	D21
	RFDiv1	D20
	BndSelDiv8	D19
BAND SELECT CLOCK COUNTER	BndSelDiv7	D18
	BndSelDiv6	D17
	BndSelDiv5	D16
	BndSelDiv4	D15
	BndSelDiv3	D14
	BndSelDiv2	D13
	BndSelDiv1	D12
	VCO POWER DOWN	VCOPwrDwn
MTLD	MTLD	D10
RF_OUTB SELECT	RF_OUTB_Sel	D9
RF_OUTB ENABLE	RF_OUTB_En	D8
RF_OUTB OUTPUT POWER	RF_OUTB_Pwr2	D7
	RF_OUTB_Pwr1	D6
RF_OUTA ENABLE	RF_OutA_En	D5
RF_OUTA OUTPUT POWER	RF_OUTA_Pwr2	D4
	RF_OUTA_Pwr1	D3
CONTROL BITS	CB3	D2
	CB2	D1
	CB1	D0

**Table 43. Register 4: 1-Bit Feedback Select. Function Description**

Name	Description	Factory Default	Function
FbkSel	FEEDBACK SELECT	1	0 = Divided 1 = Fundamental

**Table 44. Register 4: 3-Bit RF Output Divider ( $\div$  MO) Select. Function Description**

Name	Description	Factory Default	Function
RFDiv[3:1]	RF OUTPUT DIVIDER	000	000 = Div by 1 001 = Div by 2 010 = Div by 4 011 = Div by 8 100 = Div by 16 101 = Div by 32 110 = Div by 64 111 = Reserved

**Table 45. Register 4: 8-Bit Band Select Clock Counter. Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function
BndSelDiv[8:1]	BAND SELECT CLOCK COUNTER	0000 0001	0000 0000 = Not Allowed 0000 0001 = 1 0000 0010 = 2 ... 1111 1111 = 255

[a] BAND SELECT CLOCK COUNTER sets the value of the divider for the band select logic clock input. By default, the output frequency of the R counter is used to clock the band select logic. If this frequency is larger than 125kHz, the Band Select Clock counter can be used to divide the R counter output to a smaller frequency suitable for the band selection logic.

**Table 46. Register 4: 1-Bit VCO Power Down. Function Description**

Name	Description	Factory Default	Function
VCOPwrDwn	VCO POWER DOWN	0	0 = VCO Powered Up 1 = VCO Powered Down

**Table 47. Register 4: 1-Bit Mute Till Lock Detect. Function Description**

Name	Description	Factory Default	Function
MTLD	MTLD	0	0 = Mute Disabled 1 = Mute Enabled

**Table 48. Register 4: 1-Bit RF\_OUTB Select. Function Description**

Name	Description	Factory Default	Function
RF_OUTB_Sel	RF_OUTB SELECT	0	0 = Divided Output 1 = Fundamental

**Table 49. Register 4: 1-Bit RF\_OUTB Enable. Function Description**

Name	Description	Factory Default	Function
RF_OUTB_En	RF_OUTB ENABLE	0	0 = Disabled (High-Impedance) 1 = Enabled <sup>[a]</sup>

[a] RF\_OUT<sub>A</sub> must also be enabled.

**Table 50. Register 4: 2-Bit RF\_OUTB Output Power. Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function
RF_OUTB_Pwr[2:1]	RF_OUTB OUTPUT POWER	10	00 = -4dBm 01 = -1dBm 10 = +2dBm 11 = +5dBm

[a]  $f_{RF\_OUT} = 34.375\text{MHz}$ .

**Table 51. Register 4: 1-Bit RF\_OUTA Enable. Function Description**

Name	Description	Factory Default	Function
RF_OUTA_En	RF_OUTA ENABLE	0	0 = Disabled <sup>[a]</sup> (High-Impedance) 1 = Enabled

[a] RF\_OUT<sub>B</sub> will also disable.

**Table 52. Register 4: 2-Bit RF\_OUTA Output Power. Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function
RF_OUTA_Pwr[2:1]	RF_OUTA OUTPUT POWER	10	00 = -4dBm 01 = -1dBm 10 = +2dBm 11 = +5dBm

[a]  $f_{RF\_OUT} = 34.375\text{MHz}$ .

**Table 53. Register 4: 3-Bit Control Bits. Function Description<sup>[a]</sup>**

Name	Description	Function
CB[3:1]	CONTROL BITS	100 = Register 4 is programmed

[a] The user has to set CB[3:1] to 100 in order to write to Register 4.

## Register 5

**Table 54. Register 5 Bit Allocation<sup>[a]</sup>**

DESCRIPTION	NAME	BITS
RESERVED	RESERVED	D31
	RESERVED	D30
	RESERVED	D29
	RESERVED	D28
	RESERVED	D27
	RESERVED	D26
	RESERVED	D25
	RESERVED	D24
	LD PIN MODE	LDPinMode2
LDPinMode1		D22
RESERVED	RESERVED	D21
	RESERVED	D20
	RESERVED	D19
	RESERVED	D18
	RESERVED	D17
	RESERVED	D16
	RESERVED	D15
	RESERVED	D14
	RESERVED	D13
	RESERVED	D12
	RESERVED	D11
	RESERVED	D10
	RESERVED	D9
	RESERVED	D8
	RESERVED	D7
	RESERVED	D6
	RESERVED	D5
	RESERVED	D4
CONTROL BITS	RESERVED	D3
	CB3	D2
	CB2	D1
	CB1	D0

[a] D19 and D20 must be set to 1.

**Table 55. Register 5: 2-Bit LD (Lock Detect) Pin Mode. Function Description**

Name	Description	Factory Default	Function
LDPinMode[2:1]	LD PIN MODE	01	00 = Low 01 = Digital Lock Detect 10 = Low 11 = High

**Table 56. Register 5: 3-Bit Control Bits. Function Description<sup>[a]</sup>**

Name	Description	Function
CB[3:1]	CONTROL BITS	101 = Register 5 is programmed

[a] The user has to set CB[3:1] to 101 in order to write to Register 5.

## Register 6

**Table 57. Register 6 Bit Allocation**<sup>[a] [b] [c]</sup>

DESCRIPTION	NAME	BITS
DIGITAL LOCK (RO)	DigLock	D31
BAND_SELECT_DONE (RO)	Band_select_done	D30
RESERVED (RO)	Reserved	D29
RESERVED (RO)	Reserved	D28
LDP_EXT	LDP_Ext2	D27
	LDP_Ext1	D26
RF_OUTB_HI_PWR	rfoutb_hi_pwr	D25
RF_OUTA_HI_PWR	rfouta_hi_pwr	D24
SDM_ORDER	SDMOrder2	D23
	SDMOrder1	D22
DITHER GAIN	DitherG	D21
SHAPE_DITHER_EN	ShapeDitherEn	D20
RESERVED	Reserved	D19
SDM_TYPE	SDMType	D18
BAND_SELECT_ACC	band_select_acc2	D17
	band_select_acc1	D16
RESERVED (RO)		
RESERVED	Reserved	D15
	Reserved	D14
	Reserved	D13
	Reserved	D12
	Reserved	D11
	Reserved	D10
	Reserved	D9
	Reserved	D8
	Reserved	D7
EXT_BND_SEL_DIV		
CONTROL BITS		

[a] It is recommended that the user writes to Register 0 after writing to Register 6.

[b] Bits D7 and D19 must be set to 0 for correct operation.

[c] RO Bits are Read Only Bits.

**Table 58. Register 6: 1-Bit Digital Lock Detect. Function Description**

Name	Description	Function
DigLock	DIGITAL LOCK	0 = PLL Not Locked 1 = PLL Locked (according LDF and LDP in Register 2)

**Table 59. Register 6: 1-Bit Band Select Status (Read Only). Function Description**

Name	Description	Function
Band_select_done	BAND_SELECT_DONE	0 = Band Selection Not Complete 1 = Band Selection Complete



**Table 60. Register 6: 2-Bit Extra Lock Detect Precision. Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function		
			Extra Bit	LDP Bits in Register 2	Value
LDP_Ext[2:1]	LDP_EXT Extra Lock Detect Precision	00	00	0	10ns
				1	6ns
			01	0	3ns
				1	3ns
			10	0	4ns
				1	4.5ns
			11	0	1.5ns
				1	1.5ns

[a] LDP\_Ext[2:1] are Extra Lock Detect Precision bits. When these bits are set to 00, then the precision of the Lock Detect precision only relies on the LDP bit in Register 2, so that the lock detect window is 10ns or 6ns, depending on the LDP bit in Register 2. For high PFD frequencies, the 6ns window may be larger than the entire ref/FB period. The LDP\_ext bits reduce the size of the lock detect window to the value described in Table 58, allowing an accurate lock detection with higher PFD frequencies.

**Table 61. Register 6: 1-Bit Extra Bit of RF\_OUTB Power. Function Description<sup>[a] [b]</sup>**

Name	Description	Factory Default	Function		
			Extra Bit	RF_OUTB OUTPUT POWER Bits in Register 4	Value (dBm)
rf_outb_hi_pwr	RF_OUTB_HI_PWR	0	0	00	-4
				01	-1
				10	+2
				11	+5
			1	00	+2
				01	+5
				10	+6
				11	+7

[a] RF\_OUTB\_HI\_PWR is an Extra Bit of RF\_OUTB Power that increases the output power to the RF\_OUT<sub>B</sub> output.

[b]  $f_{RF\_OUT} = 34.375\text{MHz}$ .

**Table 62. Register 6: 1-Bit Extra Bit of RF\_OUTA Power. Function Description**<sup>[a] [b]</sup>

Name	Description	Factory Default	Function		
			Extra Bit	RF_OUTA OUTPUT POWER Bits in Register 4	Value (dBm)
rf_outa_hi_pwr	RF_OUTA_HI_PWR	0	0	00	-4
				01	-1
				10	+2
				11	+5
			1	00	+2
				01	+5
				10	+6
				11	+7

[a] RF\_OUTA\_HI\_PWR is an Extra Bit of RF\_OUTA Power that increases the output power to the RF\_OUTA output.

[b]  $f_{RF\_OUT} = 34.375\text{MHz}$ .

**Table 63. Register 6: 2-Bit Sigma Delta Modulator Order Configuration. Function Description**

Name	Description	Factory Default	Function
SDMOrder[2:1]	SDM_ORDER	11	00 = OFF. The device operates in integer mode and the fractional part is ignored. 01 = 1 <sup>st</sup> order 10 = 2 <sup>nd</sup> order 11 = 3 <sup>rd</sup> order

**Table 64. Register 6: 2-Bit Dither Gain Configuration. Function Description**

Name	Description	Factory Default	Function
DitherG	DITHER_GAIN	0	0 = LSB Dither (Recommended) 1 = LSB x4 Dither

**Table 65. Register 6: 1-Bit Dither Noise Shaping Configuration. Function Description**

Name	Description	Factory Default	Function
ShapeDitherEn	SHAPE_DITHER_EN	1	0 = Dither Noise Shaping Disabled 1 = Dither Noise Shaping Enabled

**Table 68. Register 6: 1-Bit Sigma Delta Modulator Type Configuration. Function Description**

Name	Description	Factory Default	Function
SDMType	SDM_TYPE	1	0 = SSMF-B 1 = SSMF-II

**Table 69. Register 6: 2-Bit VCO Band Selection Accuracy Configuration. Function Description**

Name	Description	Factory Default	Function
band_select_acc[2:1]	BAND_SELECT_ACC	00	00 = 1 cycle of the band select clock (output of the Band Select Divider) 01 = 2 cycles 10 = 4 cycles 11 = Reserved

**Table 72. Register 6: 4-Bit Extra Most Significant Bits of Band Select Divider. Function Description** <sup>[a]</sup> <sup>[b]</sup>

Name	Description	Factory Default	Value	Function
ExtBndSelDiv[4:1]	EXT_BND_SEL_DIV	0000	BSCC_R4 + [EXT_BND_SEL_DIV]x256	0000 = [BSCC_R4]
				0001 = [BSCC_R4]+256
				0010 = [BSCC_R4] + 512
				.....
				1111 = [BSCC_R4]+3840

[a] EXT\_BND\_SEL\_DIV are Extra 4 MSBs that extend the Band Select Clock Counter in Register 4. These additional bits are necessary for band selection to divide down to <500kHz when high PFD frequencies are used.

[b] BSCC\_R4 is the BAND SELECT CLOCK COUNTER value in Register 4.

**Table 73. Register 6: 3-Bit Control Bits. Function Description** <sup>[a]</sup>

Name	Description	Function
CB[3:1]	CONTROL BITS	110 = Register 6 is programmed

[a] The user has to set CB[3:1] to 110 in order to write to Register 6.

## Register 7

**Table 74. Register 7 Bit Allocation**<sup>[a] [b] [c]</sup>

BITS	NAME	DESCRIPTION
D31	Loss_Dig_Lock	LOSS_DIG_LOCK (SB)
D30	Loss_Anlg_Lock	LOSS_ANLG_LOCK (SB)
D29	Spi_error	SPI_ERROR (SB)
D28	Reserved	RESERVED
D27	Rev_ID3	REV_ID (RO)
D26	Rev_ID2	
D25	Rev_ID1	
D24	Dev_ID4	DEV_ID (RO)
D23	Dev_ID3	
D22	Dev_ID2	
D21	Dev_ID1	
D20	16b_12b_sel	16b_12b_SEL
D19	1	1
D18	RESERVED	RESERVED
D17	RESERVED	RESERVED
D16	RESERVED	RESERVED
D15	ext_mod4	EXT_MOD
D14	ext_mod3	
D13	ext_mod2	
D12	ext_mod1	EXT_FRAC
D11	ext_fdiv4	
D10	ext_fdiv3	
D9	ext_fdiv2	
D8	ext_fdiv1	SCLKE
D7	sclke	
D6	Rd_Addr3	READBACK_ADDR
D5	Rd_Addr2	
D4	Rd_Addr1	
D3	SPI_R_WN	SPI_R_WN
D2	CB3	CONTROL BITS
D1	CB2	
D0	CB1	

[a] SB Bits are Sticky Bits and need to be cleared.

[b] RO Bits are Read Only Bits.

[c] Write 1 to Bit D19 for normal reliable operation.

**Table 75. Register 7: 1-Bit Loss of Digital Lock. Function Description**<sup>[a]</sup>

Name	Description	Function
Loss_Dig_Lock	LOSS_DIG_LOCK	0 = Locked since last time register was cleared 1 = Loss of Digital Lock since last time register was cleared

[a] This bit is a sticky bit and needs to be cleared with a SPI write of 1 to detect further Loss of Digital Lock occurrences.

**Table 76. Register 7: 1-Bit Loss of Analog Lock. Function Description**<sup>[a]</sup>

Name	Description	Function
Loss_Anlg_Lock	LOSS_ANLG_LOCK	0 = Band Selection remained the same since last time register was cleared 1 = Band selection occurred since last time register was cleared

[a] This bit is a sticky bit and needs to be cleared with a SPI write of 1 to detect further Band Selection occurrences.

**Table 77. Register 7: 1-Bit SPI Error. Function Description**<sup>[a]</sup>

Name	Description	Function
Spi_error	SPI_ERROR	0 = No SPI write error detection 1 = SPI Write error

[a] Spi\_error Bit goes high if the SPI interface detects a cycle with the incorrect number of SCLK cycles between nCS asserted Low and nCS asserted High. The SPI interface expects 32 clock cycles between nCS asserted Low and nCS asserted High. Any Read/Write via the SPI interface with more or less than 32 clock cycles will result in the Spi\_error Bit switched to 1. This bit is a sticky bit and needs to be cleared with a SPI write of 1 in order to detect further possible SPI Write/Read errors.

**Table 78. Register 7: 3-Bit Revision ID. Function Description**

Name	Description	Function
Rev_ID[3:1]	REV_ID	010

**Table 79. Register 7: 4-Bit Device ID. Function Description**

Name	Description	Function
Dev_ID[4:1]	DEV_ID	0110

**Table 80. Register 7: 1-Bit Resolution Select. Function Description**

Name	Description	Factory Default	Function
16b_12b_sel	16b_12b_SEL	0	0 = FRAC, PHASE and MOD set to 12-Bit resolution, Bit[D19:D8] set to 0 and unused
			1 = FRAC, PHASE and MOD set to 16-Bit resolution

**Table 82. Register 7: 4-Bit Extra Bits of MOD Value. Function Description**<sup>[a]</sup>

Name	Description	Factory Default	Function		
			MOD	EXT_MOD	Value
ext_mod[4:1]	EXT_MOD	0000	0000 0000 0000	0000	Not Allowed
				0001	Not Allowed
				0010	2
				...	...
				1111	15
			0000 0000 0001	0000	16
				...	...
				1111	31
			...		
			1111 1111 1111	0000	65520
				...	...
				1111	65535

[a] Bit D20 in Register 7 (16b\_12b\_SEL) is required to be set to 1 when using this table. If Bit D20 in Register 7 (16b\_12b\_SEL) is set to 0, see [Table 24](#).

**Table 83. Register 7: 4-Bit Extra Bits of FRAC Value. Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function		
			FRAC	EXT_FRAC	Value
ext_div[4:1]	EXT_FRAC	0000	0000 0000 0000	0000	0
				0001	1
				...	...
				1111	15
			0000 0000 0001	0000	16
				...	...
				1111	31
			...		
			1111 1111 1111	0000	65520
				...	...
				1111	65535

[a] Bit D20 in Register 7 (16b\_12b\_SEL) is required to be set to 1 when using this table. If Bit D20 in Register 7 (16b\_12b\_SEL) is set to 0, refer to Table 19.

**Table 84. Register 7: 1-Bit SCLKE. Function Description**

Name	Description	Factory Default	Function
Sclke	SCLKE	1	0 = Output Data in a Read Cycle on a Rising Edge of SCLK 1 = Output Data in a Read Cycle on a Falling Edge of SCLK

**Table 85. Register 7: 1-Bit READBACK\_ADDR. Function Description<sup>[a]</sup>**

Name	Description	Function
Rd_Addr[3:1]	READBACK_ADDR	000 = Register 0 001 = Register 1 010 = Register 2 011 = Register 3 100 = Register 4 101 = Register 5 110 = Register 6 111 = Register 7

[a] In order to Read a register, the user must write to Register 7 first and set the SPI\_R\_WN Bit to 1 (READ) and indicate the address of the register to read in the READBACK\_ADDR Bit (Bits[D6:D4]).

**Table 86. Register 7: 1-Bit SPI\_R\_WN. Function Description<sup>[a]</sup>**

Name	Description	Factory Default	Function
SPI_R_WN	SPI_R_WN	0	0 = WRITE 1 = READ

[a] Writing this bit to a 1 will allow the user to read back the register selected in READBACK\_ADDR on the next 32 SCLK cycle. This bit will revert back to 0 once it is written with 1 and will not retain the 1 value.

**Table 87. Register 7: 3-Bit Control Bits. Function Description<sup>[a]</sup>**

Name	Description	Function
CB[3:1]	CONTROL BITS	111 = Register 7 is programmed

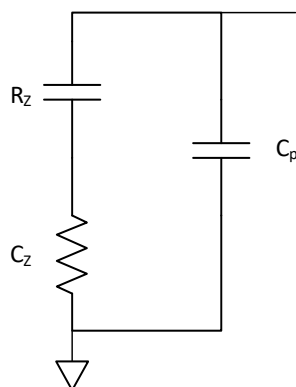
[a] The user has to set CB[3:1] to 111 in order to write to Register 7.

## Applications Information

### Loop Filter Calculations

#### 2<sup>nd</sup> Order Loop Filter

This section helps design a 2<sup>nd</sup> order loop filter for the 8V97053. A general 2<sup>nd</sup> order loop filter is shown in Figure 12. Step-by-step calculations to determine R<sub>z</sub>, C<sub>z</sub> and C<sub>p</sub> values for a desired loop bandwidth are described below. Required parameters are provided. A spreadsheet for calculating the loop filter values is also available.

**Figure 12. Typical 2<sup>nd</sup> Order Loop Filter**


1. Determine desired loop bandwidth  $f_c$ .
2. Calculate R<sub>z</sub>:

$$R_z = \frac{2 * \pi * f_c * N}{I_{cp} * K_{vco}}$$

Where,

**I<sub>cp</sub>** is charge pump current. I<sub>cp</sub> is programmable from 310μA to 5mA.

**N** is effective feedback divider. N must be programmed into the following value.

$$N = \frac{F_{VCO}}{F_{pd}}$$

**F<sub>VCO</sub>** is VCO frequency.

VCO frequency range: 2200MHz to 4400MHz

**F<sub>pd</sub>** is phase detector input frequency.

$$F_{pd} = \frac{F_{ref}}{P_v}$$

**F<sub>ref</sub>** is reference clock (REF\_IN) input frequency.

**P<sub>v</sub>** is overall pre-divider setting.

**K<sub>vco</sub>** is VCO gain. K<sub>vco</sub> = 60MHz/V

3. Calculate C<sub>z</sub>:

$$C_z = \frac{\alpha}{2 * \pi * f_c * R_z}$$

Where,

$\alpha$  = f<sub>c</sub>/ f<sub>z</sub>, user can determine an  $\alpha$  number.

$\alpha$  > 6 is recommended.

**f<sub>z</sub>** is frequency at zero.

4. Calculate C<sub>p</sub>:

$$C_p = \frac{C_z}{\alpha * \beta}$$

Where,

$\beta$  = f<sub>p</sub>/f<sub>c</sub>, user can determine  $\beta$  number.

$\beta$  > 4 is recommended.

**f<sub>p</sub>** is frequency at pole.

5. Verify Phase Margin (PM)

$$PM = \arctan \left( \frac{b - 1}{2 * \sqrt{b}} \right)$$

Where,

$$b = 1 + \frac{C_z}{C_p}$$

The phase margin (PM) should be greater than 50°.



A spreadsheet for calculating the loop filter component values is available at [www.IDT.com](http://www.IDT.com). To use the spreadsheet, the user simply enters the following parameters:

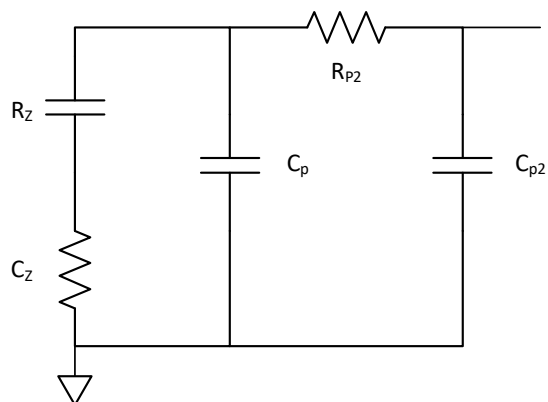
$f_c$ ,  $F_{ref}$ ,  $P_V$ ,  $I_{cp}$ ,  $F_{VCO}$ ,  $\alpha$  and  $\beta$ .

The spreadsheet will provide the component values,  $R_z$ ,  $C_z$  and  $C_p$  as the result. The spreadsheet also calculates the maximum phase margin for verification.

### 3<sup>rd</sup> Order Loop Filter

This section helps design a 3<sup>rd</sup> order loop filter for the 8V97053. A general 3<sup>rd</sup> order loop filter is shown in Figure 13.

**Figure 13. Typical 3<sup>rd</sup> Order Loop Filter**



The  $R_z$ ,  $C_z$  and  $C_p$  can be calculated as 2<sup>nd</sup> order loop filter.

The following equation help determine the 3<sup>rd</sup> order loop filter  $R_{p2}$  and  $C_{p2}$ .

Pick an  $R_{p2}$  value.  $R_{p2} \sim 1.5 \times R_z$  is suggested.

$$C_{p2} = \frac{R_z * C_p}{R_{p2} * \gamma}$$

Where,

$\gamma$  is ratio between the 1<sup>st</sup> pole frequency and the 2<sup>nd</sup> pole frequency.  $\gamma > 4$  is recommended.

## Recommendations for Unused Input and Output Pins

### Inputs

#### LVC MOS Control Pins

All control pins have internal pullup and pulldown resistors; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### Outputs

#### Output Pins

For any unused output, it can be left floating and disabled.

Figure 14 and Figure 15 show general application schematic examples for the 8V97053.

The 8V97053 input is high impedance. The input termination depends on the driver type termination requirements. In these examples, the 8V97053 REF\_IN input is terminated with a matched load termination. For transmission line with characteristic impedance  $Z_0 = 50\Omega$ , the termination resistor R8 is  $50\Omega$ . The input is self-biased to proper DC offset after the AC coupling.

### Figure 14. An 8V97053 General Application Schematic Example



The loop filter values can be calculated to meet the loop bandwidth requirement. Please refer to the [Loop Filter Calculations](#) for detailed calculations. For fast lock mode, the loop filter can be configured as Fast Lock Loop Filter Option 1 or Fast Lock Loop Filter Option 2 shown in [Figure 14](#).

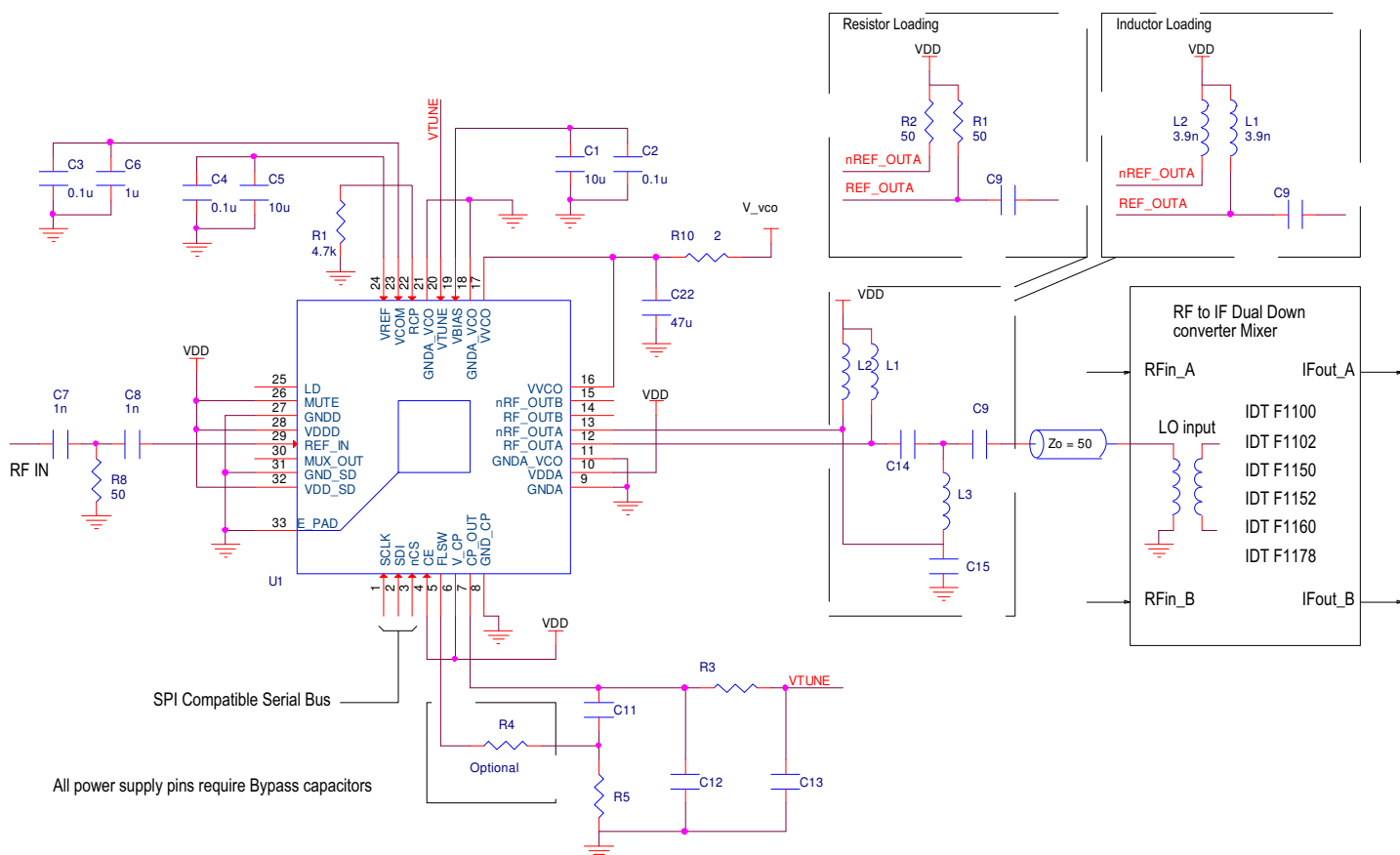
Fast Lock Loop Filter Option 1 is Parallel Resistor Configuration. For normal operating mode, only R5 is active and  $R5 = R_s$ , where  $R_s$  is the resistor value for normal operating mode loop bandwidth. In fast lock mode, the combination of R4 in parallel with R5 is active. For example, in normal operation mode, if the charge pump current is set at 0000 ( $ICP = 310\mu A$ ), then, in fast lock mode, the loop bandwidth is set larger by increasing the charge pump current to  $ICP \sim 5mA$  ( $ICP$  setting = 1111 or 16 times the normal charge pump current). The combination of the R4 and R5 in parallel is  $1/4 * R_s$ .

Fast Lock Loop Filter Option 2 is Series Resistor Configuration. For normal operating mode, both R6 and R7 are active and  $R6 + R7 = R_s$ . For fast lock mode, only R6 is active. For example, in normal operation mode, if the charge pump current is set at 0000 ( $ICP = 310\mu A$ ), then, in fast lock mode, the loop bandwidth is set larger by increasing the charge pump current to  $ICP \sim 5mA$  ( $ICP$  setting = 1111 or 16 times the normal charge pump current). The sum of R6 and R7 equals to  $R_s$ , i.e.  $R6 + R7 = R_s$ .

$R6 = 1/4 * R_s$  and  $R7 = 3/4 * R_s$ .

The 8V97053 output pull-up loading can be resistors or inductors. The pull up resistor value is typically  $50\Omega$ . Resistor pull up loading covers wide range of output frequencies. For inductor pull up loading, the inductor value is frequency dependent. One inductor value cannot cover all the output frequency range. This example shows the  $L = 3.9nH$  that is suitable for approximately 2GHz operating frequency. The output can also drive single ended LO input. [Figure 15](#) shows an example of the 8V97053 output driving single ended LO input of the mixer through an LC balun. The LC balun component values are frequency dependent. These values can be adjusted to optimize the performance. Single ended LO receiver input also can tap to one side of the differential driver using resistor loading or inductor loading. For single ended LO input, both sides of the differential driver still need to be loaded with pull up. The output power level can also be adjusted further through programming.

**Figure 15. Schematic Example for Driving Single Ended Mixer**



## Power Considerations

The 8V97053 device was designed and characterized to operate within the ambient industrial temperature range of -40°C to +85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature. The power calculation example below was generated using a typical configuration. For many applications, the power consumption can vary depending on configuration. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

**Example 1:** VCO Frequency Range = 1991MHz to 2846MHz

### 1. Power Dissipation.

The total power dissipation for the 8V97053 is the sum of the core power plus the power dissipation in the output driver. The following is the power dissipation for  $V_{DD} = 3.465V$ , which gives worse case results.

$$\text{Power (core)}_{MAX} = V_{DD\_MAX} * (I_{DDA} + I_{VCO} + I_{CP} + I_{DD\_SD} + I_{DD})_{MAX} = V_{DD\_MAX} * (I_{DDA} + I_{DDX})_{MAX} = 3.465V * (105mA + 145mA) = \mathbf{866.25mW}$$

**Total Power** (with two outputs active at 2dBm output power level) = **866.25mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 34.34°C/W per [Table 88](#).

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs active is:

$$85^\circ\text{C} + 0.866W * 34.34^\circ\text{C/W} = 114.74^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 88. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFPN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	34.34°C/W	30.7°C/W	29.12°C/W

## Example 2: VCO Frequency Range = 2590MHz to 3624MHz

### 1. Power Dissipation.

The total power dissipation for the 8V97053 is the sum of the core power plus the power dissipation in the output driver. The following is the power dissipation for  $V_{DD} = 3.465V$ , which gives worse case results.

$$\text{Power (core)}_{\text{MAX}} = V_{DD\_MAX} * (I_{DDA} + I_{VCO} + I_{CP} + I_{DD\_SD} + I_{DDD})_{\text{MAX}} = V_{DD\_MAX} * (I_{DDA} + I_{DDX})_{\text{MAX}} = 3.465V * (85mA + 146.4mA) = \mathbf{802mW}$$

**Total Power** (with two outputs active at 2dBm output power level) = **802mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 34.34°C/W per [Table 88](#).

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs active is:

$$85^\circ\text{C} + 0.802W * 34.34^\circ\text{C/W} = 113^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

## Reliability Information

**Table 89.  $\theta_{JA}$  vs. Air Flow for a 32-VFQFPN**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	34.34°C/W	30.7°C/W	29.12°C/W

**Table 90.  $\theta_{JB}$  vs. Air Flow for a 32-VFQFPN**

$\theta_{JB}$ vs. Air Flow <sup>[a]</sup>	
Meters per Second	0
Multi-Layer PCB, JEDEC Standard Test Boards	0.472°C/W

[a] Note:  $\theta_{JB}$  is independent of airflow.

## Transistor Count

The 8V97053 transistor count is: 338,270

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

[www.renesas.com/us/en/document/psc/package-outline-drawing-package-code-nlg32p1-32-vfqfn-50-x-50-x-09-mm-body-05-mm-pitch](http://www.renesas.com/us/en/document/psc/package-outline-drawing-package-code-nlg32p1-32-vfqfn-50-x-50-x-09-mm-body-05-mm-pitch)

## Marking Diagram



- Lines 1 and 2 indicate the part number.
- Line 3:
  - "#" denotes stepping.
  - "YY" is the last two digits of the year; "WW" is the work week number that the part was assembled.
  - "\$" denotes the mark code.

## Ordering Information

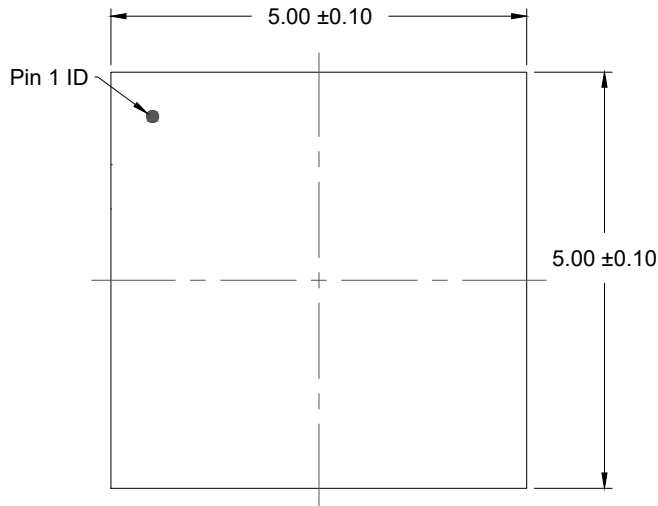
Part/Order Number	Marking	Package	Shipping Packaging	Temperature Range
8V97053NLGI	IDT8V97053NLGI	Lead-free (RoHS 6), 32-VFQFPN, 5 × 5 mm	Tray	-40°C to +85°C
8V97053NLGI8	IDT8V97053NLGI		Tape and Reel	-40°C to +85°C
8V97053NLGI/W	IDT8V97053NLGI		Tape and Reel	-40°C to +85°C

**Table 91. Pin 1 Orientation in Tape and Reel Packaging**

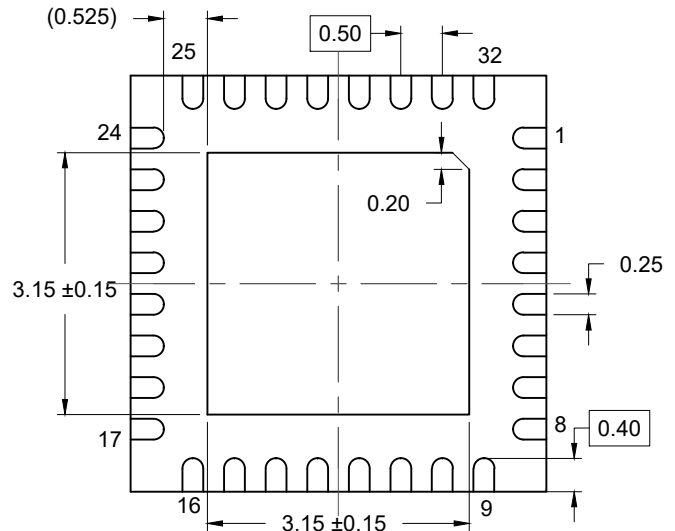
Part Number Suffix	Pin 1 Orientation	Illustration
NLGI8	Quadrant 1 (EIA-481-C)	<p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p>
NLGI/W	Quadrant 2 (EIA-481-D)	<p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p>

## Revision History

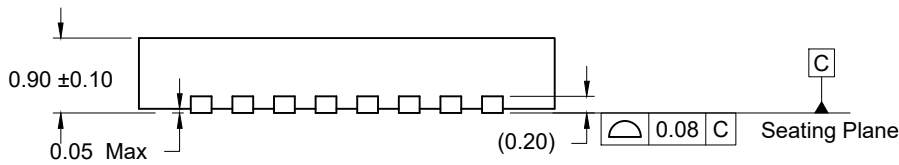
Revision Date	Description of Change
February 2, 2023	Updated POD link in <a href="#">Package Outline Drawings</a> .
September 22, 2018	Changed the functional value of REV_ID in <a href="#">Table 78</a>
August 7, 2018	Changed incorrect measurement unit nF to nH in <a href="#">Output Matching</a> and <a href="#">Schematic Example</a>
April 23, 2018	Initial release.



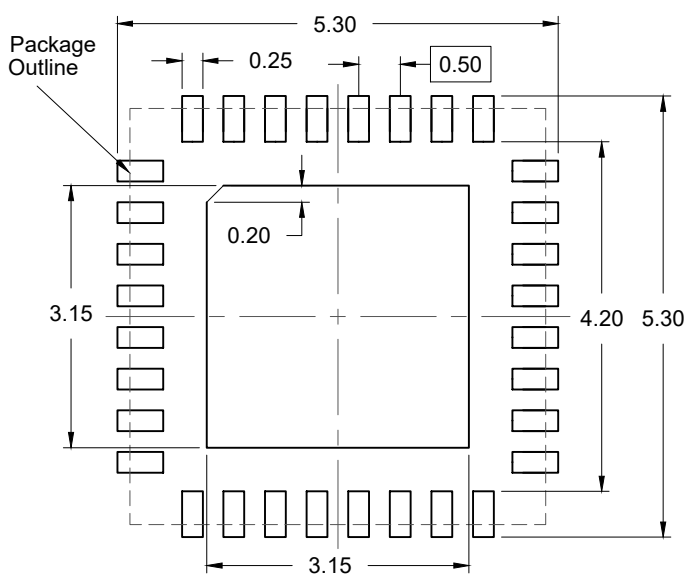
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

## NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



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