Ultralow, I_Q, anyCAP® Low Dropout Regulator

ADP3342

FEATURES

- **Accuracy over line and load: ±4.0% @ 25°C, ±5% over temperature**
- **Ultralow dropout voltage: 190 mV (typ) @ 300 mA**
- **Requires only C_O = 1.0 µF for stability**
- **anyCAP architecture stable with any type of capacitor (including MLCC)**
- **Current and thermal limiting**
- **Low shutdown current: < 2 µA**
- **1.7 V ≤ V_{IN} ≤ 6 V**
- **2.8 V ≤ V_{CC} ≤ 6 V**
- **V_{OUT} = 1.2 V ±5%**
- **0°C to +100°C ambient temperature range**
- **Ultrasmall thermally enhanced 8-lead MSOP package**

APPLICATIONS

- **Notebook PCs**
- **Desktop PCs**

GENERAL DESCRIPTION

The ADP3342 is a unique member of the ADP33xx family of precision low dropout anyCAP voltage regulators. The ADP3342 operates with an input voltage range of 1.7 V to 6 V and delivers a continuous load current up to 300 mA. In order to support the ability to regulate from such a low input voltage, the power rail to the IC, VCC, has been split off from the main power rail, IN, from which the output is powered.

The ADP3342 stands out from the conventional LDOs because it has the lowest thermal resistance of any MSOP-8 package and an enhanced process that enables it to offer performance advantages beyond its competition. Its patented design requires only a 1.0 µF output capacitor for stability. This device is insensitive to output capacitor equivalent series resistance (ESR) and is stable with any good quality capacitor, including ceramic (MLCC) types for space-restricted applications. The dropout voltage of the ADP3342 is only 190 mV (typical) at 300 mA. This device also includes a safety current limit, thermal overload protection, and a shutdown control pin.

FUNCTIONAL BLOCK DIAGRAM

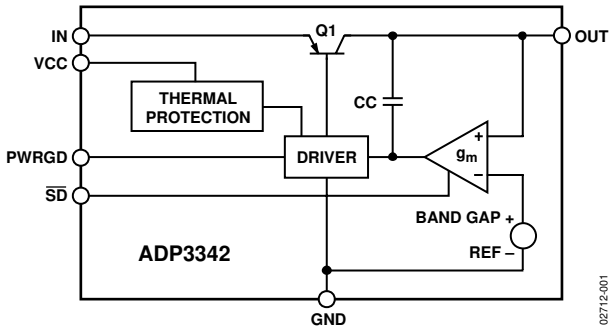

Figure 1.

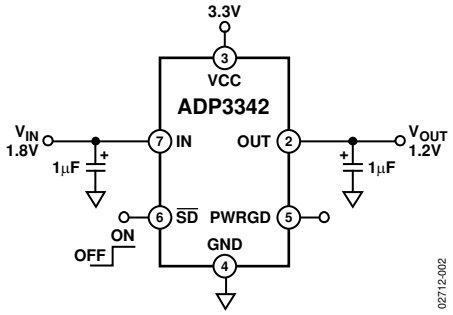

Figure 2. Typical Application Circuit

Rev. D

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SPECIFICATIONS

V_{CC} = 3.0 V, V_{IN} = 1.8 V, C_{IN} = C_{OUT} = 1 µF, T_A = 0°C to 100°C, unless otherwise noted.[1, 2]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy	V_{OUT}	V_{CC} = 2.8 V to 6 V, V_{IN} = 1.7 V to 6 V	−4.0		+4.0	%
		I_L = 0.1 mA to 300 mA				
		T_A = 25°C				
		V_{CC} = 2.8 V to 6 V, V_{IN} = 1.7 V to 6 V	−5.0		+5.0	%
		I_L = 0.1 mA to 300 mA				
		T_A = −40°C to +100°C				
Line Regulation		V_{CC} = 2.8 V to 6 V, V_{IN} = 1.7 V to 6 V		0.04		mV/V
		T_A = 25°C				
Load Regulation		I_L = 0.1 mA to 300 mA		0.12		mV/mA
		T_A = 25°C				
Dropout Voltage	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 300 mA		190	450	mV
		I_L = 200 mA		125		mV
		I_L = 100 mA		70		mV
Current Limiting	I_{LIM}	V_{CC} = 3 V, V_{IN} = 1.8 V		450		mA
Output Noise	V_{NOISE}	f = 10 Hz to 100 kHz, C_L = 1 µF		60		µV rms
		I_L = 300 mA				
OPERATING CURRENTS						
Ground Current in Regulation	I_{GND}	I_L = 300 mA, T_A = −40°C to +100°C		3.0	8.5	mA
		I_L = 300 mA, T_A = 0°C to 100°C		3.0	6.0	mA
		I_L = 300 mA, T_A = 25°C		3.0	4.0	mA
		I_L = 200 mA		2.0		mA
		I_L = 0.1 mA		100	175	µA
VCC Current in Regulation	I_{VCC}	I_L = 300 mA		100	170	µA
Ground Current in Shutdown	I_{GNDSD}	SD = 0 V, V_{CC} = 6 V, V_{IN} = 1.8 V		0.01	2	µA
SHUTDOWN						
Threshold Voltage	V_{THSD}	On	VCC − 0.9			V
		Off			0.6	V
$\overline{SD}$ Input Current	$I_{\overline{SD}}$	$0 \le \overline{SD} \le 6$ V		1.4	7	µA
Output Current in Shutdown	I_{OSD}	T_A = 25°C, V_{CC} = 6 V, V_{IN} = 6 V		0.01	1	µA
		T_A = 100°C, V_{CC} = 6 V, V_{IN} = 6 V		0.01	2	µA
PWRGD						
Output Current	I_{PWRGDL}	V_{PWRGD} = 1.2 V, V_{CC} = 3.0 V	0.85	1.5		mA
Output Low Voltage	V_{PWRGDL}[3]	I_{PWRGD} = 300 µA			0.4	V
Output High Voltage	V_{PWRGDH}[3]	I_{PWRGD} = 300 µA	VCC − 0.4			V
On-Time Delay	TD1[4]	I_L = 3 mA to 300 mA, C_{OUT} = 1 µF to 10 µF	5		300	µs
	TD2[5]	I_L = 3 mA to 300 mA, C_{OUT} = 1 µF to 10 µF	50		300	µs
Off-Time Delay	TD3[6]	I_L = 3 mA to 300 mA, C_{OUT} = 1 µF to 10 µF	0.05		1	µs
THERMAL PROTECTION						
Shutdown Temperature	TH_{PROT}	I_L = 100 mA		165		°C

[1] All limits at temperature extremes are guaranteed via a correlation using standard statistical quality control (SQC) methods.
[2] Ambient temperature of 100°C corresponds to a junction temperature of 125°C under typical full load test conditions.
[3] V_{PWRGDL}, V_{PWRGDH}: Power good output voltages. Guaranteed by design and characterization.
[4] TD1: Delay time from V_{OUT} crossing 1 V to PWRGD high. Guaranteed by design.
[5] TD2: Delay time from $\overline{SD}$ high to PWRGD high. Guaranteed by design.
[6] TD3: Delay time between $\overline{SD}$ low and PWRGD low. Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Supply Voltage	−0.3 V to +13 V
Shutdown Input Voltage	−0.3 V to +13 V
Power Dissipation	Internally Limited
Operating Ambient Temperature Range	−40°C to +100°C
Operating Junction Temperature Range	−40°C to +150°C
θ_{JA} (2-Layer Board)	205°C/W
θ_{JA} (4-Layer Board)	142°C/W
θ_{JC}	56°C/W
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

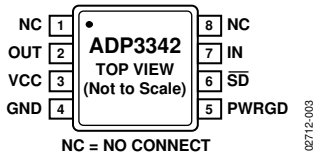

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 8	NC	No Connection.
2	OUT	Output of the Regulator. Bypass to ground with a 1.0 µF or larger capacitor.
3	VCC	Supply Voltage.
4	GND	Ground Pin.
5	PWRGD	Power Good. Used to indicate that output is in regulation.
6	$\overline{SD}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the VCC pin.
7	IN	Regulator Input.

TYPICAL PERFORMANCE CHARACTERISTICS

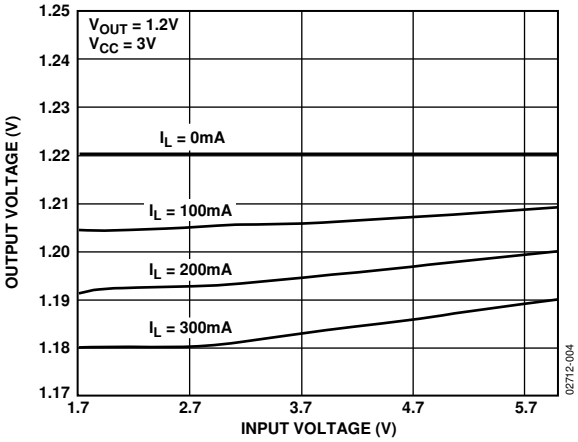

Figure 4. Line Regulation Output Voltage vs. Supply Voltage

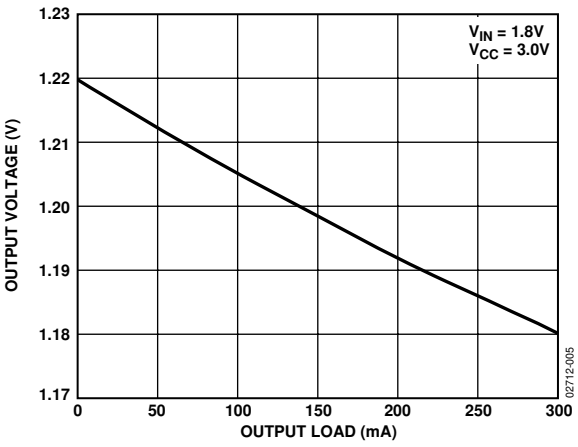

Figure 5. Output Voltage vs. Load Current

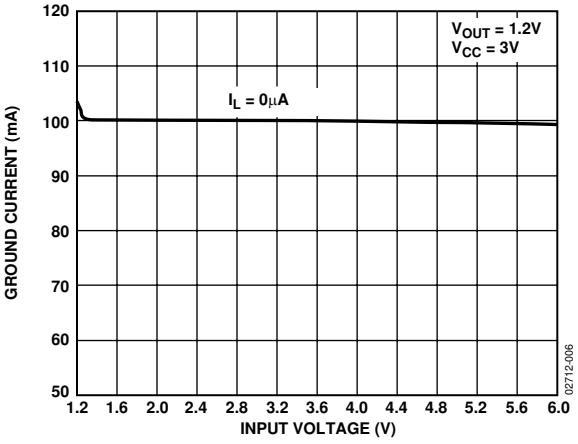

Figure 6. Ground Current vs. Supply Voltage

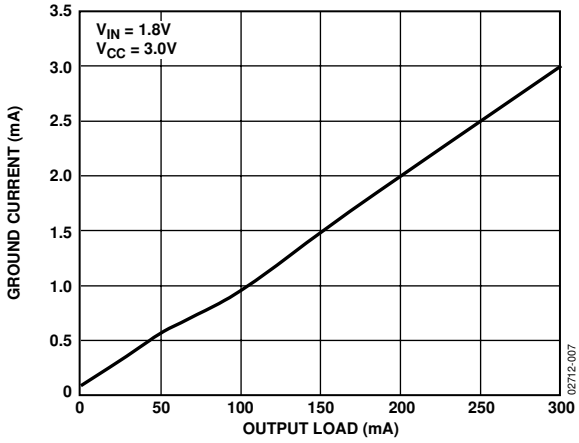

Figure 7. Ground Current vs. Load Current

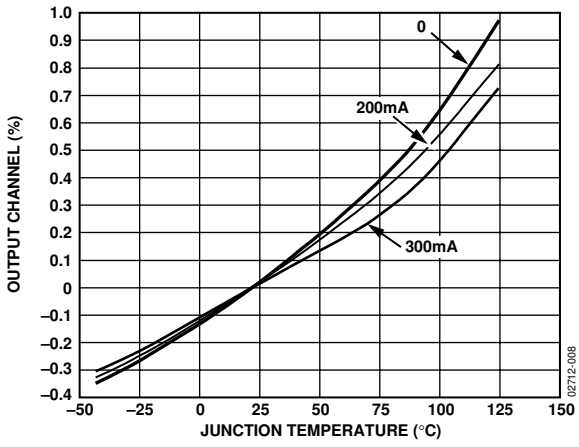

Figure 8. Output Voltage Variation vs. Junction Temperature

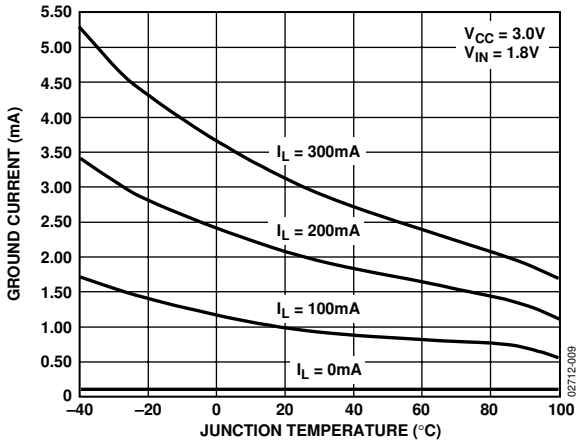

Figure 9. Ground Current vs. Junction Temperature

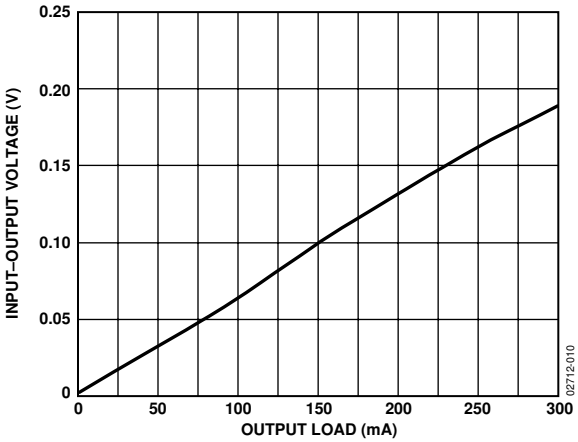

Figure 10. Dropout Voltage vs. Output Current

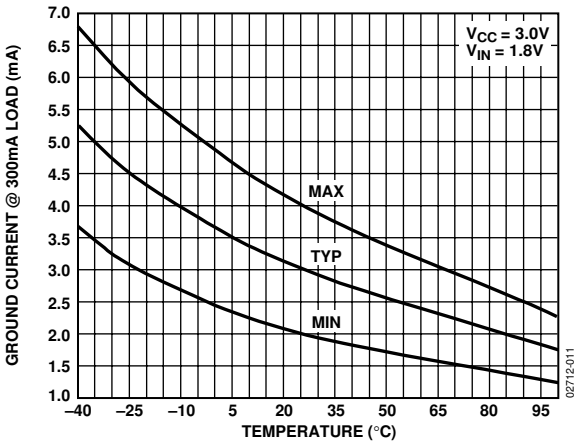

Figure 11. Ground Current @ 300 mA Load vs. Ambient Temperature

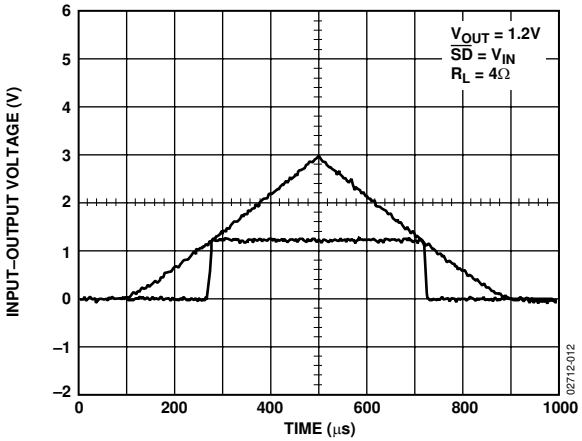

Figure 12. Power-Up/Power-Down

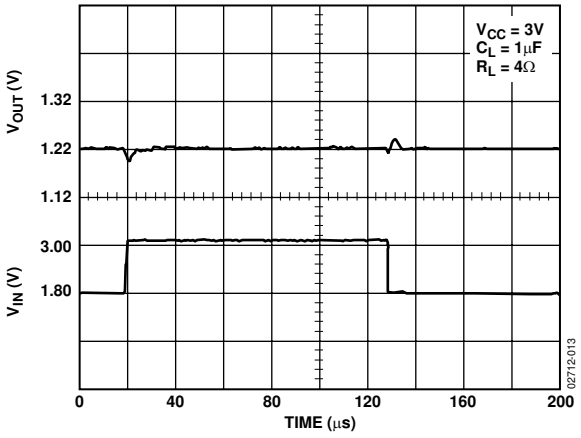

Figure 13. Line Transient Response

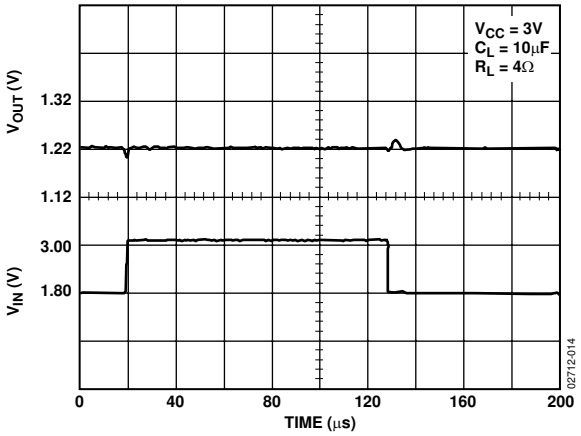

Figure 14. Line Transient Response

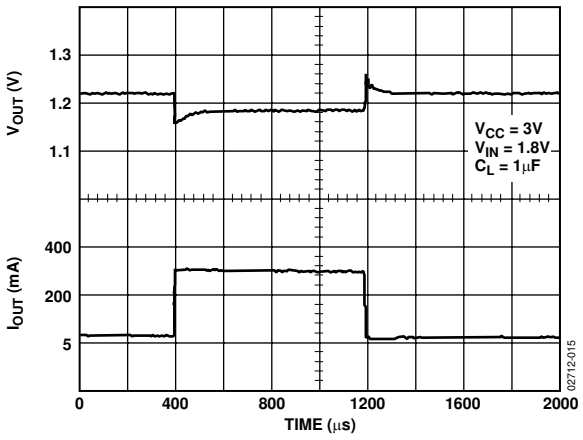

Figure 15. Load Transient Response

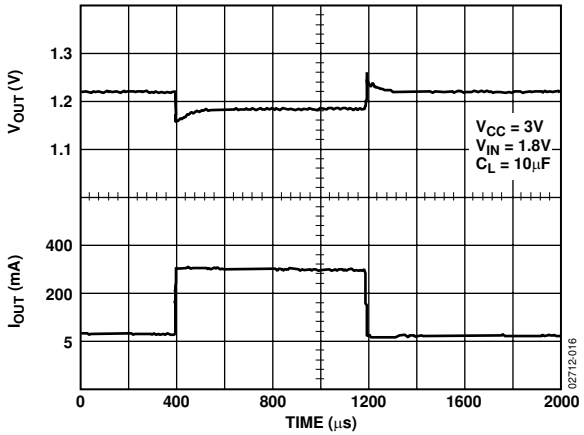

Figure 16. Load Transient Response

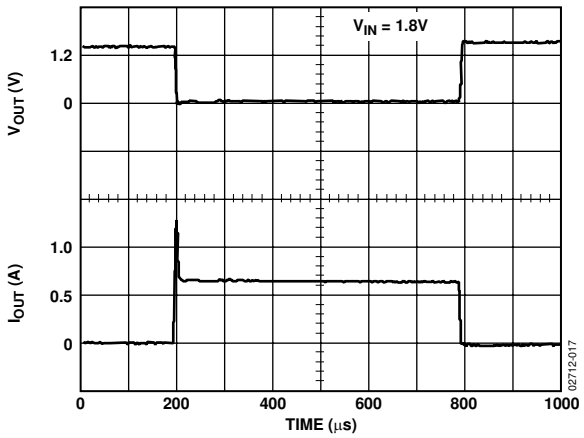

Figure 17. Short-Circuit Current

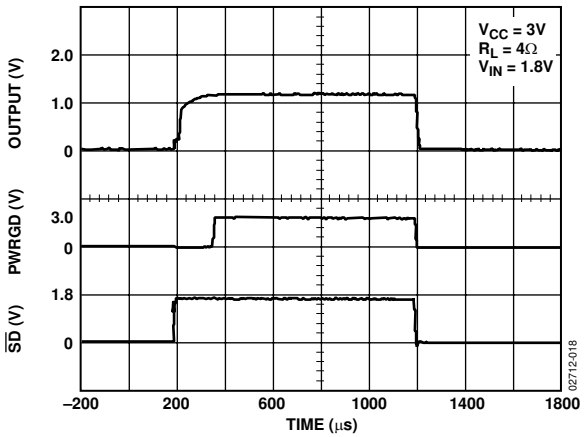

Figure 18. Power-On/Power-Off Response from Shutdown

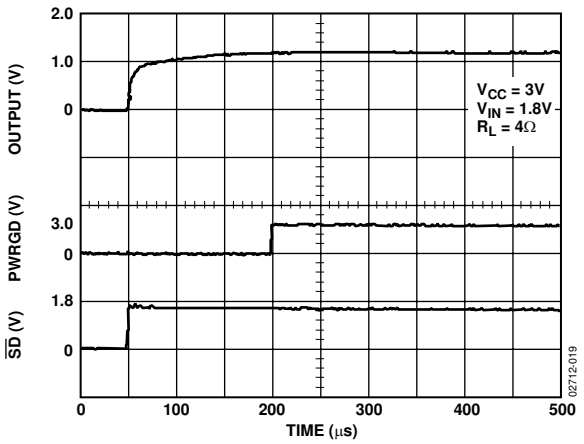

Figure 19. Turn-On Delay

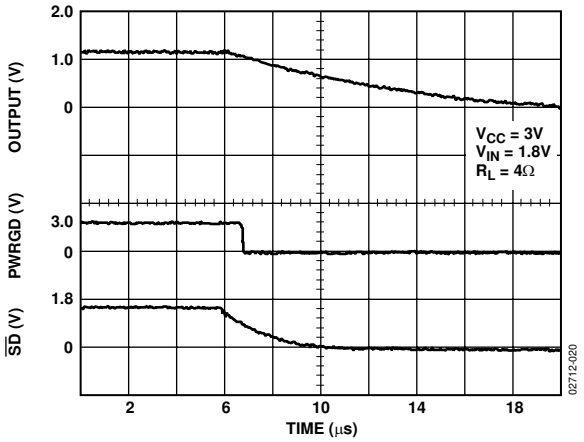

Figure 20. Turn-Off Delay

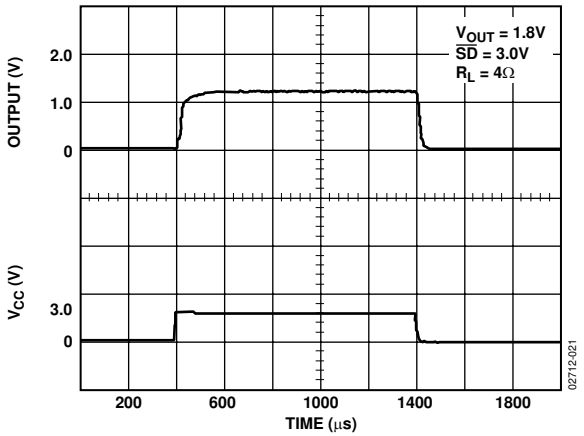

Figure 21. Power-On/Power-Off Response from V_{CC}

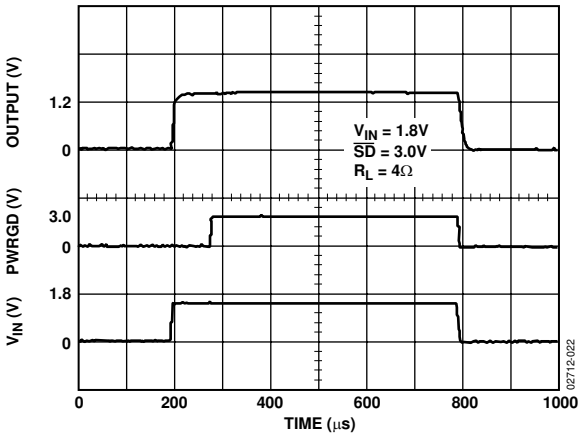

Figure 22. Power-On/Power-Off Response from V_{IN}

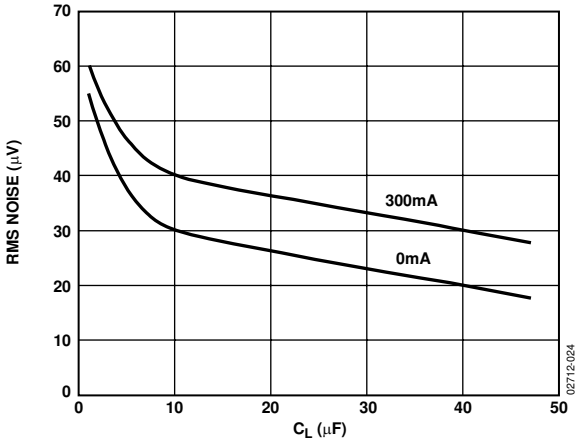

Figure 24. RMS Noise vs. C_L (10 Hz to 100 Hz)

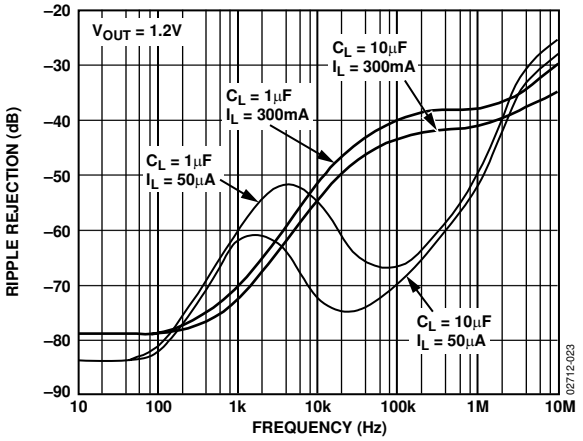

Figure 23. Power Supply Ripple Rejection

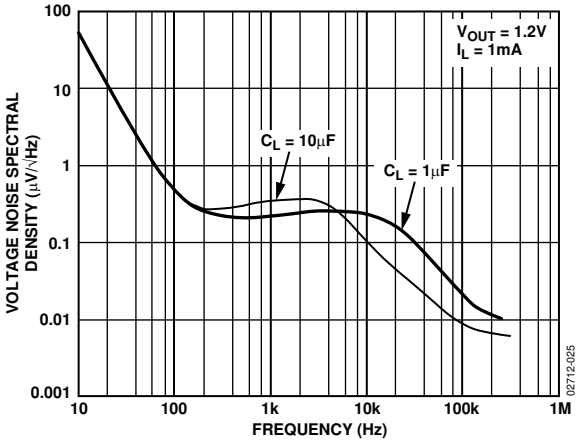

Figure 25. Output Noise Density

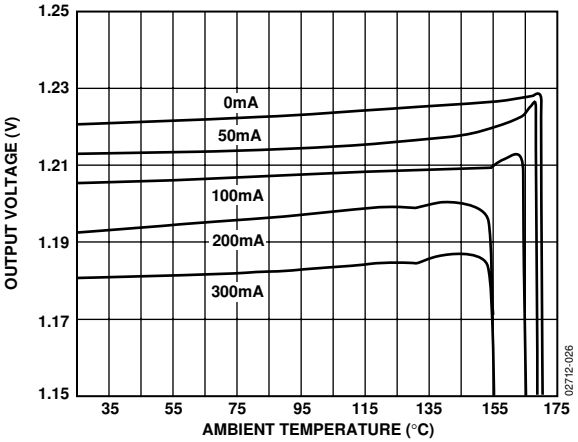

Figure 26. Thermal Protection

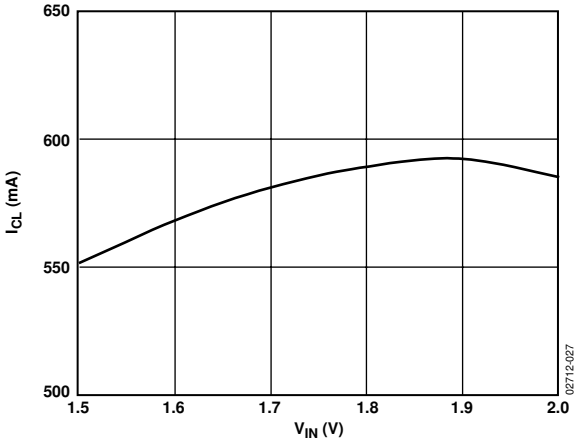

Figure 27. Current Limit vs. V_{IN}

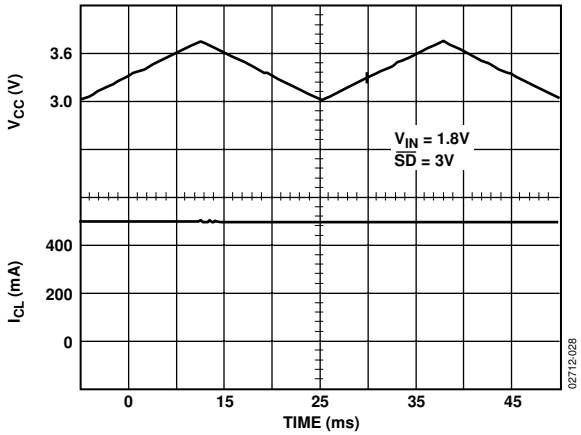

Figure 28. Current Limit vs. VCC

THEORY OF OPERATION

The anyCAP LDO ADP3342 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

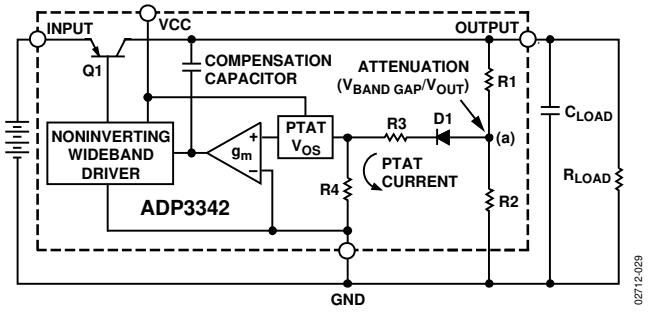

Figure 29. Control Loop Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that, at equilibrium, it produces a large, temperature proportional input offset voltage that is repeatable and very well controlled. The temperature proportional offset voltage is combined with the complementary diode voltage to form a virtual band gap voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that lead to a low noise design.

The R1, R2 divider is chosen in the same ratio as the band gap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by Diode D1 and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3342 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1 µF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain, resulting in excellent line and load regulation. Additional features of the circuit include current limit, thermal shutdown, and noise reduction.

APPLICATION INFORMATION

PC APPLICATION—VCCVID

The ADP3342 has been optimized for PC applications that require a 1.2 V output for powering the voltage identification rail, V_{CCVID}. The rail from which the output draws current, the IN pin, is separated from the rail that powers the IC, the VCC pin. This allows a higher efficiency design when, as recommended for IMVP-3/5 applications, the VCC pin is connected to a 3.3 V supply to power the IC adequately, and the IN pin is connected to a 1.8 V supply. The efficiency is nearly 60% in this case.

CAPACITOR SELECTION

As with any voltage regulator, output transient response is a function of the output capacitance. The ADP3342 is stable with a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 1 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3342 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON. The effective capacitance of some capacitor types may fall below the minimum at cold temperature. Ensure that the capacitor provides more than 1 µF at minimum temperature.

INPUT BYPASS CAPACITOR

An input bypass capacitor is not strictly required but is advisable in any application involving long input wires or high source impedance. Connecting a 1 µF capacitor from IN to ground reduces the circuit's sensitivity to PC board layout. If a larger value output capacitor is used, a larger value input capacitor is also recommended.

POWER GOOD MONITORING FUNCTION

The PWRGD pin does not monitor the output voltage directly but rather detects whether the internal PNP pass transistor is being modulated by the regulation loop. This method of detecting PWRGD, rather than using a voltage threshold detection, provides an inherent and desirable delay in asserting the PWRGD signal. During startup or overload, the regulation loop is not in control, so the PWRGD pin is low.

SHUTDOWN MODE

Applying a TTL high signal to the shutdown ($\overline{SD}$) pin, or tying it to the VCC input pin, turns on the output. Pulling $\overline{SD}$ down to 0.4 V or below, or tying it to ground, turns off the output. In shutdown mode, quiescent current is reduced.

THERMAL OVERLOAD PROTECTION

The ADP3342 is protected against damage due to excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions, that is, high ambient temperature and power dissipation where die temperature starts to rise above 165°C, the output current is reduced until the die temperature drops to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be limited by operating conditions so that the junction temperature does not exceed 150°C.

CALCULATING JUNCTION TEMPERATURE

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + V_{IN} \times I_{GND}$$

where I_{LOAD} and I_{GND} are load current and ground current, and V_{IN} and V_{OUT} are input and output voltages, respectively.

Assuming that I_{LOAD} = 300 mA, I_{GND} = 4 mA, V_{IN} = 1.8 V, and V_{OUT} = 1.2 V, device power dissipation is

$$P_D = (1.8\text{ V} - 1.2\text{ V}) \times 300\text{ mA} + (1.8\text{ V}) \times 4\text{ mA} = 187\text{ mW}$$

The ADP3342 is capable of supplying 300 mA @ V_{IN} = 1.8 V in a typical notebook PC application. If a higher input voltage, such as 3.3 V, is used, the power dissipation of the ADP3342 is limited by the thermal overload protection. Assuming a 4-layer board, the junction temperature rise above ambient temperature is approximately equal to

$$\Delta T_{JA} = 193\text{ mW} \times 142°\text{C/W} = 27.4°\text{C}$$

OUTLINE DIMENSIONS

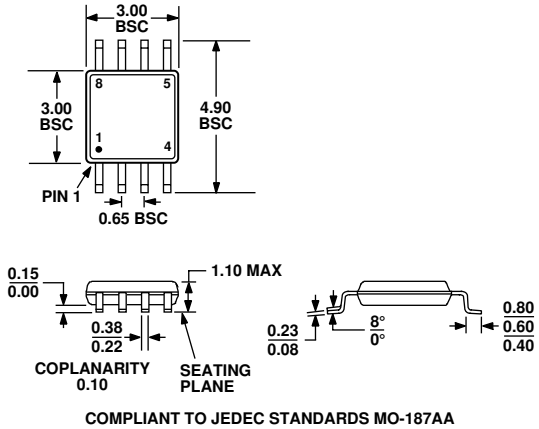

Figure 30. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Output Voltage	Temperature Range	Package Description	Package Option	Branding
ADP3342JRM-REEL	1.2 V	0°C to 100°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	LJA
ADP3342JRM-REEL7	1.2 V	0°C to 100°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	LJA
ADP3342JRMZ-REEL7[1]	1.2 V	0°C to 100°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	LJA

[1] Z = Pb-free part.

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