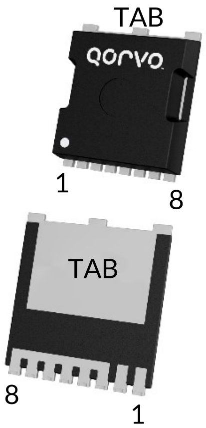
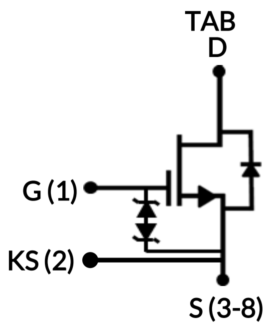
DATASHEET

UJ4SC075018L8S

750V-18mΩ SiC FET

Rev A, February 2023





Part Number	Package	Marking
UJ4SC075018L8S	MO-229	UJ4SC075018

RoHS COMPLIANT · Pb LEAD FREE · HF HALOGEN FREE

Description

The UJ4SC075018L8S is a 750V, 18mΩ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving MO-229 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: 18mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 128nC
- Low body diode V_{FSD}: 1.14V
- Low gate charge: Q_G = 37.8nC
- Threshold voltage $V_{G(th)}$: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected, HBM class 2
- MO-229 package for faster switching, clean gate waveforms

Typical applications

- Solid state relays and circuit-breakers
- Line rectification and active-bridge rectification circuits in AC/DC front-ends
- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current [1]	I_D	T_C < 118°C	53	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	208	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =3.6A	97.2	mJ
SiC FET dv/dt Ruggedness	dv/dt_{rug}	V_{DS}<500V	200	V/ns
Power dissipation	P_{tot}	T_C = 25°C	349	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	260	°C

1. Limited by bondwires
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.33	0.43	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	750			V
Total drain leakage current	I_{DSS}	V_{DS}=750V, V_{GS}=0V, T_J=25°C		1.3	45	μA
		V_{DS}=750V, V_{GS}=0V, T_J=175°C		20		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		4.7	20	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=50A, T_J=25°C		18	23	mΩ
		V_{GS}=12V, I_D=50A, T_J=125°C		29		
		V_{GS}=12V, I_D=50A, T_J=175°C		37		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	4.8	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C< 118°C			53	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			208	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_S=20A, T_J=25°C		1.14	1.46	V
		V_{GS}=0V, I_S=20A, T_J=175°C		1.35		
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=50A, V_{GS}=-0V, R_G=50Ω di/dt=1500A/μs, T_J=25°C		128		nC
Reverse recovery time	t_{rr}			26.4		ns
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=50A, V_{GS}=-0V, R_G=50Ω di/dt=1500A/μs, T_J=150°C		138		nC
Reverse recovery time	t_{rr}			28		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=400V, V_{GS}=0V f=100kHz		1414		pF
Output capacitance	C_{oss}			118		
Reverse transfer capacitance	C_{rss}			2		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V		150		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 400V, V_{GS}=0V		280		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V		12		μJ
Total gate charge	Q_G	V_{DS}=400V, I_D=50A, V_{GS} = 0V to15V		37.8		nC
Gate-drain charge	Q_{GD}			8		
Gate-source charge	Q_{GS}			11.8		
Turn-on delay time	$t_{d(on)}$	Note 4, V_{DS}=400V, I_D=50A, Gate Driver = 0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=50Ω Inductive Load, FWD: same device with V_{GS} = 0V, R_G = 50Ω, T_J=25°C		13.6		ns
Rise time	t_r			26.4		
Turn-off delay time	$t_{d(off)}$			134		
Fall time	t_f			18.4		
Turn-on energy	E_{ON}			234		μJ
Turn-off energy	E_{OFF}			216		
Total switching energy	E_{TOTAL}			450		
Turn-on delay time	$t_{d(on)}$	Note 4, V_{DS}=400V, I_D=50A, Gate Driver = 0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=50Ω Inductive Load, FWD: same device with V_{GS} = 0V, R_G = 50Ω, T_J=150°C		13		ns
Rise time	t_r			31		
Turn-off delay time	$t_{d(off)}$			136		
Fall time	t_f			18.4		
Turn-on energy	E_{ON}			272		μJ
Turn-off energy	E_{OFF}			258		
Total switching energy	E_{TOTAL}			530		

4. Measured with the half-bridge mode switching test circuit in Figure 23.

Typical Performance Diagrams

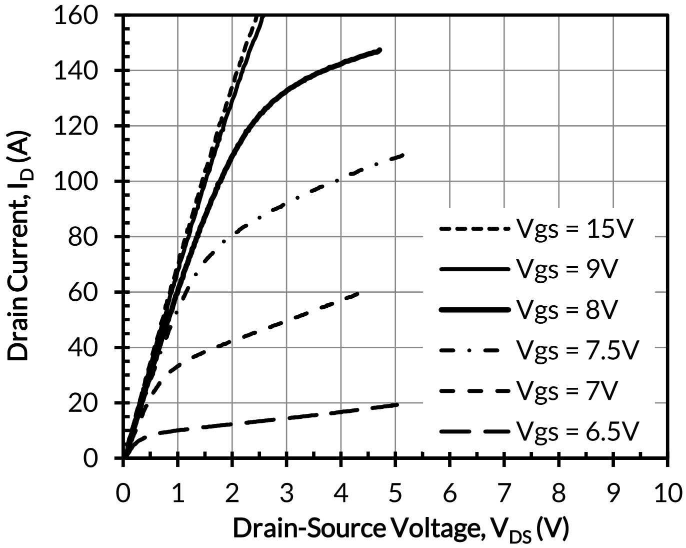


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

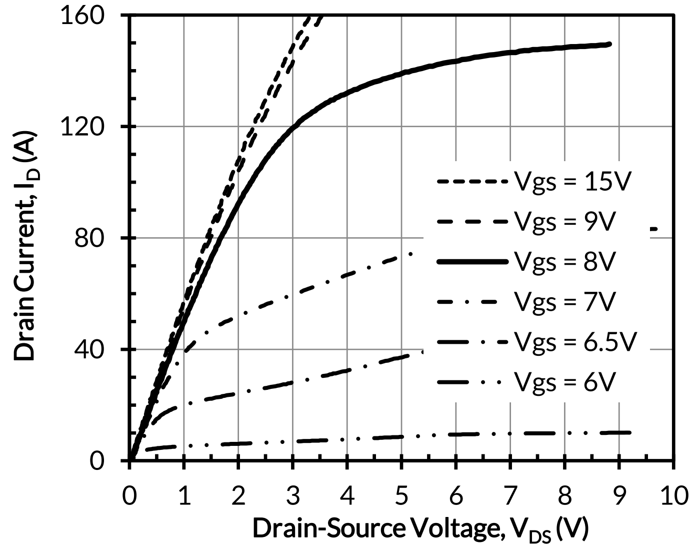


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

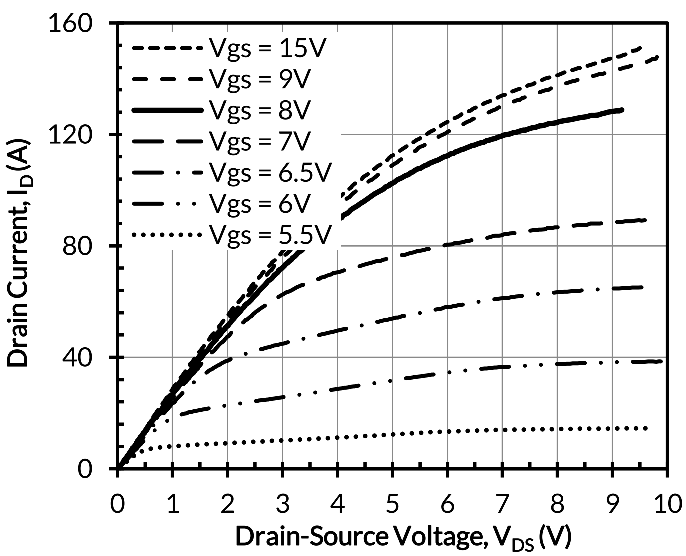


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

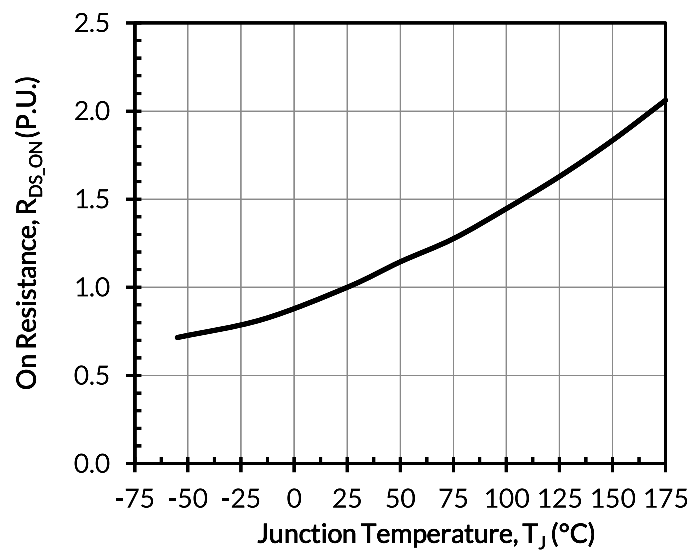


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 50A

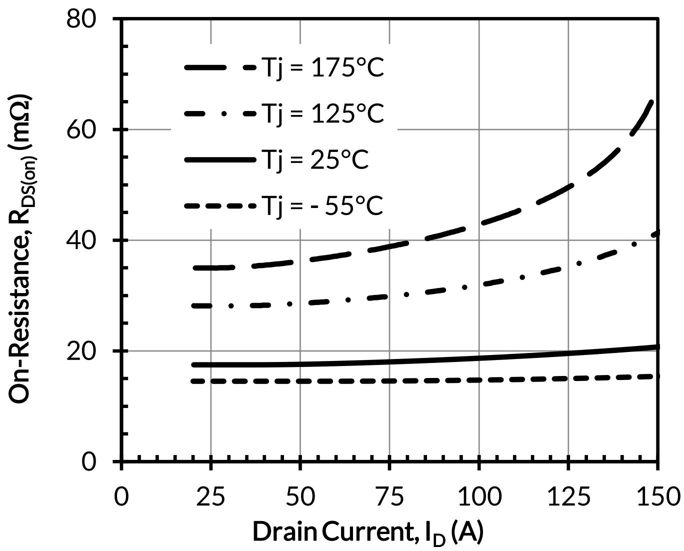


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

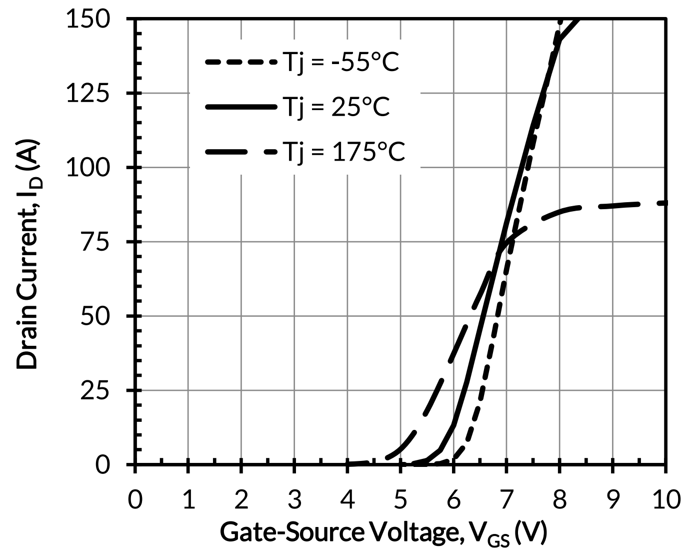


Figure 6. Typical transfer characteristics at V_{DS} = 5V

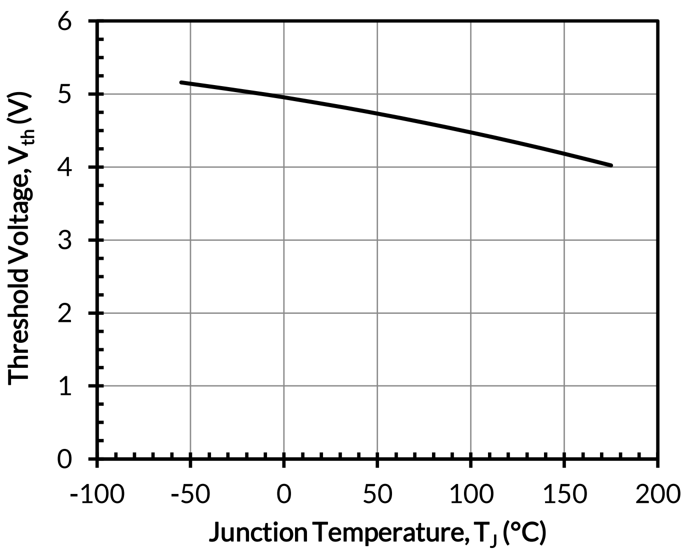


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

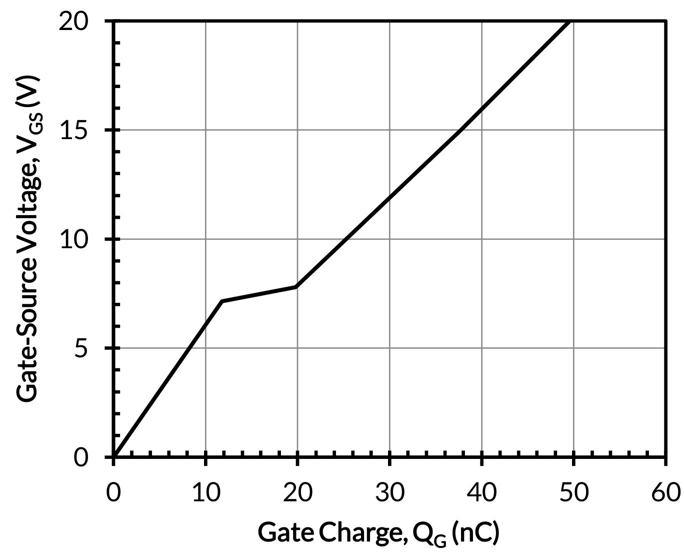


Figure 8. Typical gate charge at V_{DS} = 400V and I_D = 50A

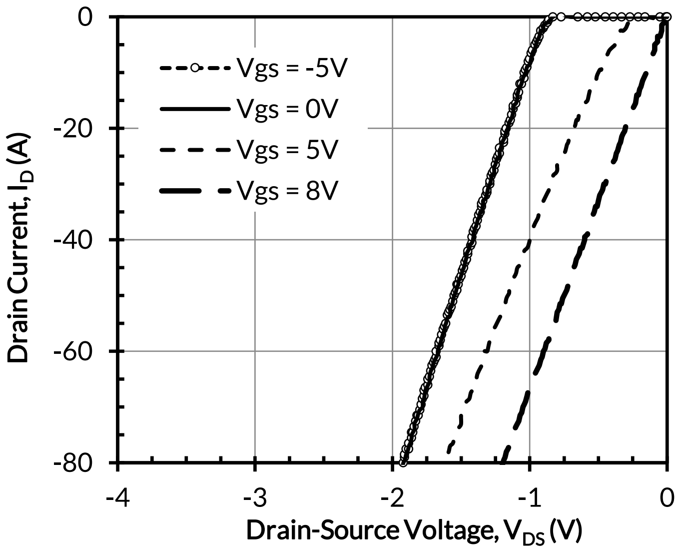


Figure 9. 3rd quadrant characteristics at T_J = -55°C

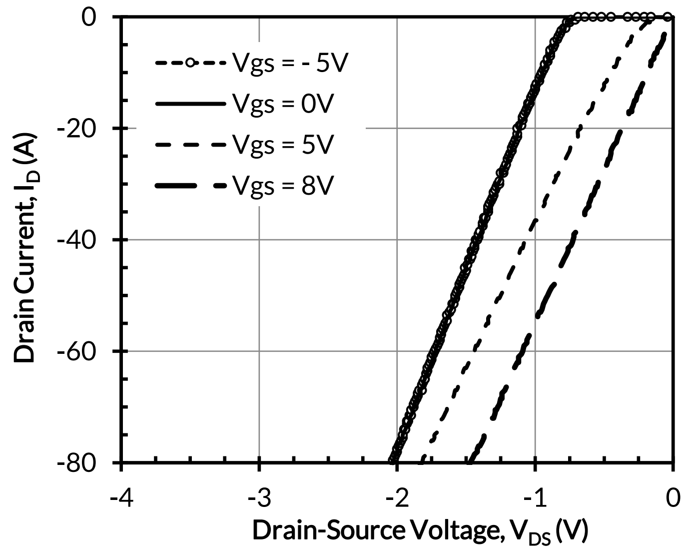


Figure 10. 3rd quadrant characteristics at T_J = 25°C

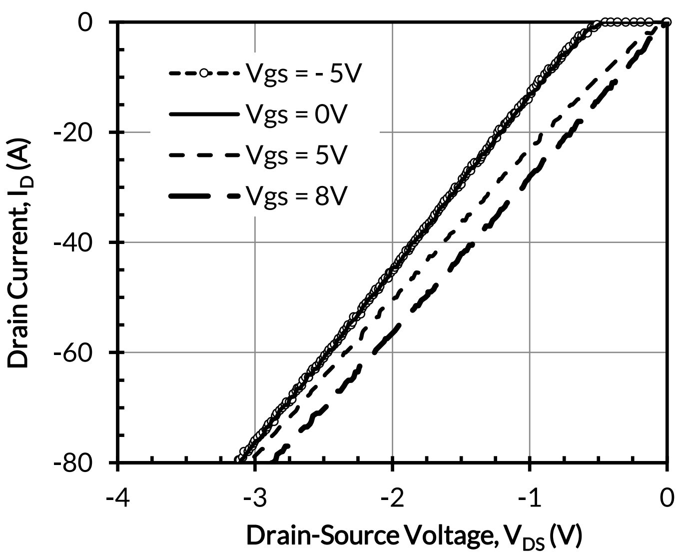


Figure 11. 3rd quadrant characteristics at T_J = 175°C

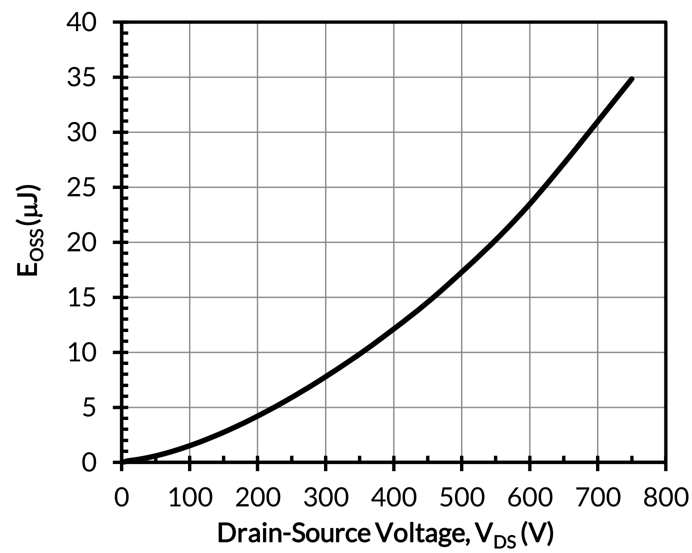


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

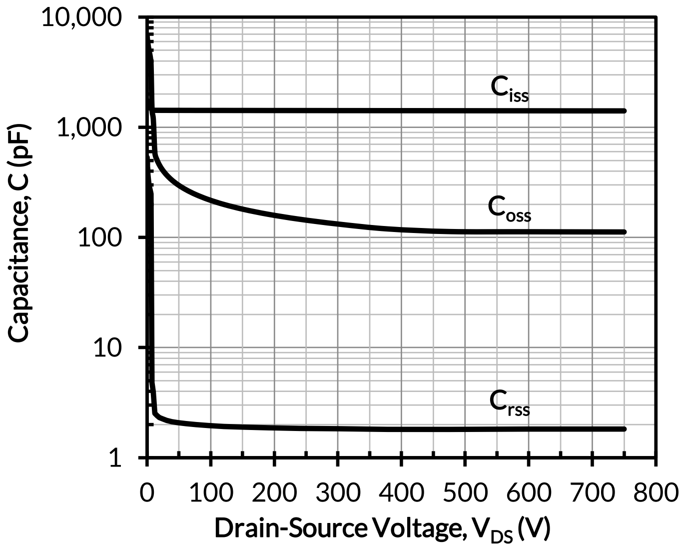


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

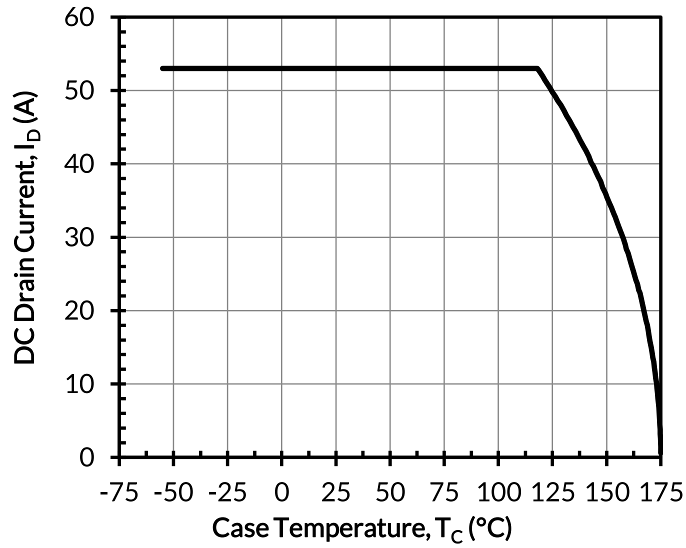


Figure 14. DC drain current derating

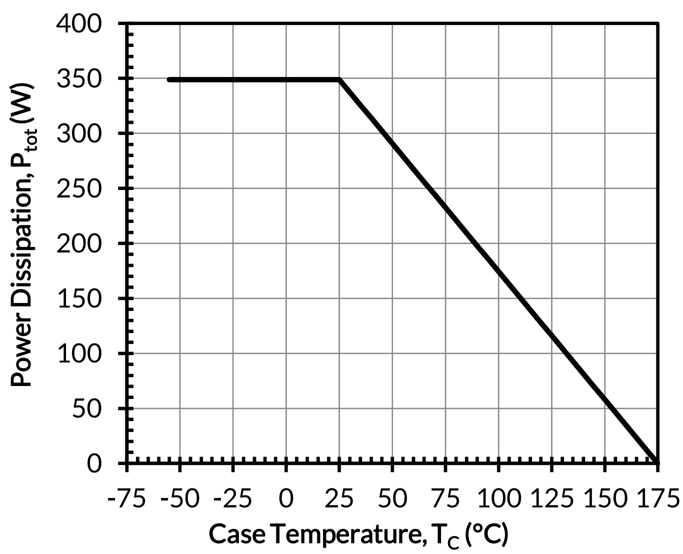


Figure 15. Total power dissipation

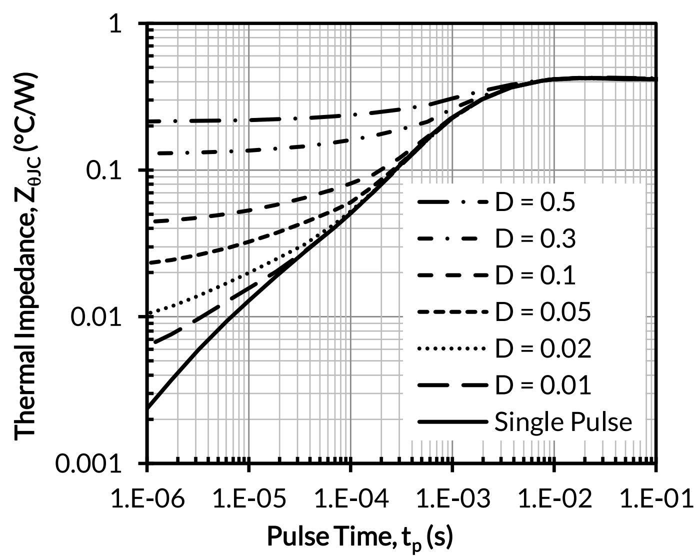


Figure 16. Maximum transient thermal impedance

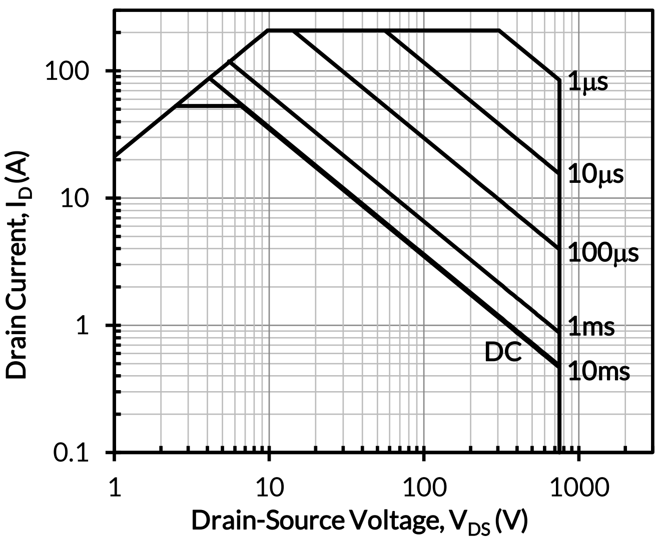


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

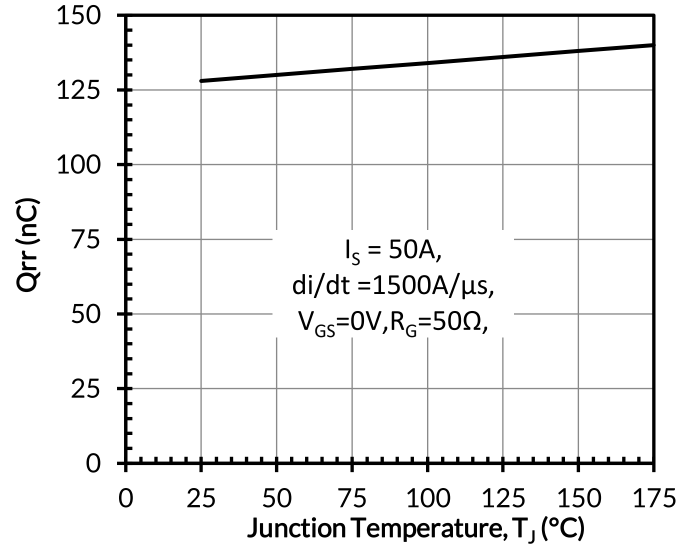


Figure 18. Reverse recovery charge Qrr vs. junction temperature at Vds = 400V

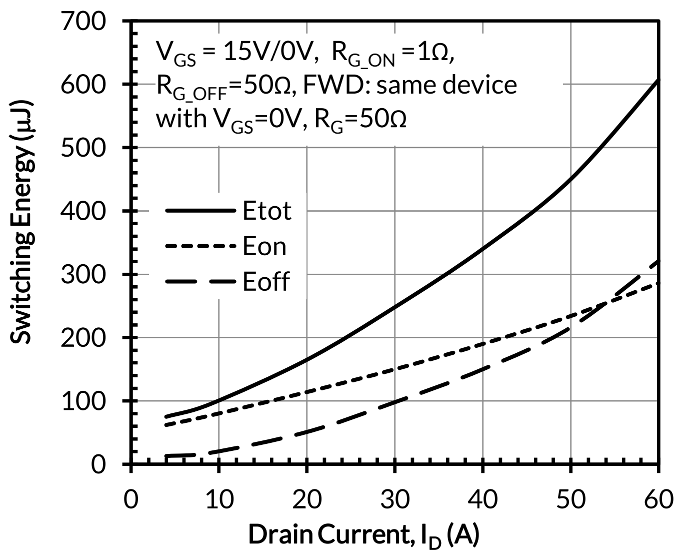


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

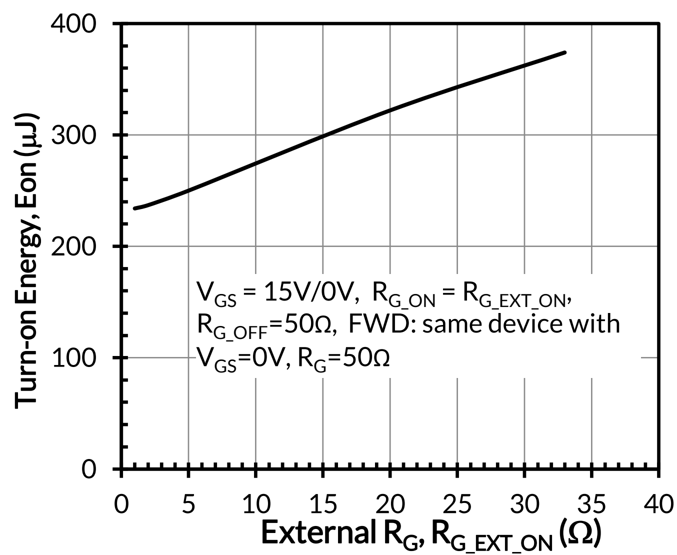


Figure 20. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON} at V_{DS} = 400V and I_D = 50A

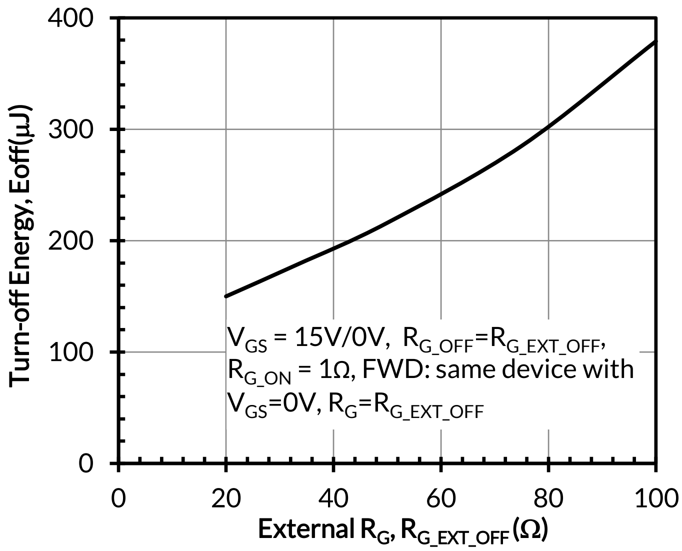


Figure 21. Clamped inductive switching turn-off energy vs. $R_{G\_EXT\_OFF}$ at V_{DS} = 400V and I_D = 50A

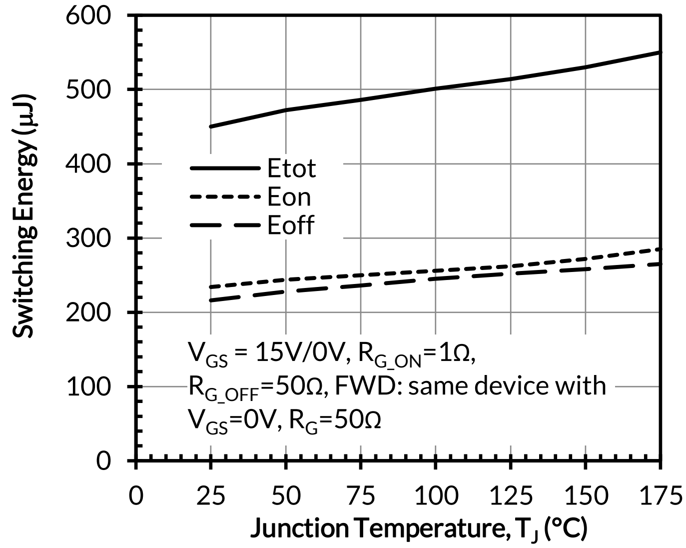


Figure 22. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 50A

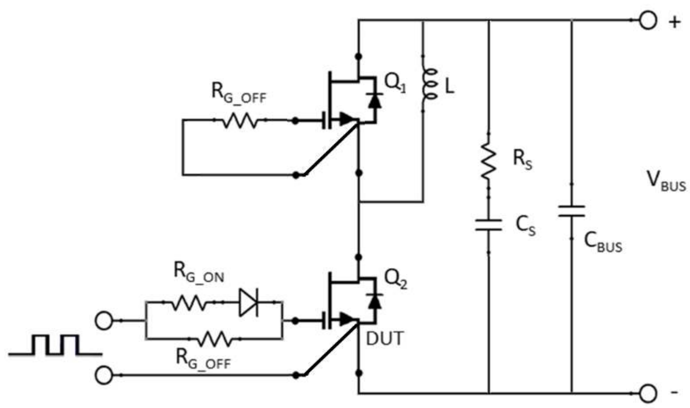


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_S = 2.5Ω, C_S=100nF) is used to reduce the power loop high frequency oscillations.

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

Important notice