

# **BUK961R6-40E**

# N-channel TrenchMOS logic level FET

28 July 2016

**Product data sheet** 

### 1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

#### 2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with Vgst(th) rating of greater than 0.5V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- · Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

#### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	40	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	-	120	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	349	W
Static characte	eristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	1.35	1.6	mΩ
Dynamic characteristics							
$Q_{GD}$	gate-drain charge	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; Fig. 13; Fig. 14		-	40.9	-	nC

[1] Continuous current is limited by package.



## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D I
2	D	drain		
3	S	source		G—VIII
mb	D	mounting base; connected to drain	1 3	mbb076 S
			D2PAK (SOT404)	

## 6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK961R6-40E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404		

## 7. Marking

Table 4. Marking codes

Ту	pe number	Marking code
ВІ	UK961R6-40E	BUK961R6-40E

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS}$ = 20 k $\Omega$		-	40	V
$V_{GS}$	gate-source voltage	T <sub>j</sub> ≤ 175 °C; DC		-10	10	V
		T <sub>j</sub> ≤ 175 °C; Pulsed	[1][2]	-15	15	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	349	W
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; <u>Fig. 2</u>	[3]	-	120	Α
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; <u>Fig. 2</u>	[3]	-	120	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; Fig. 3		-	1348	Α
T <sub>stg</sub>	storage temperature			-55	175	°C
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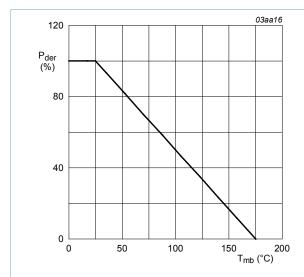
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#### N-channel TrenchMOS logic level FET

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain diode						
Is	source current	T <sub>mb</sub> = 25 °C	[3]	-	120	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	1348	Α
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 120 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[4][5]	-	1008	mJ

- Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering  $T_i$  and or  $V_{GS}$
- [3] Continuous current is limited by package.
- Single-pulse avalanche rating limited by maximum junction temperature of 175 °C. Refer to application note AN10273 for further information.



Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

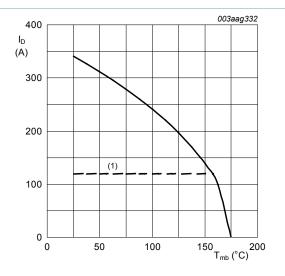


Fig. 2. Continuous drain current as a function of mounting base temperature

 $V_{GS} \ge 5V$ 

(1) Capped at 120 A due to package.

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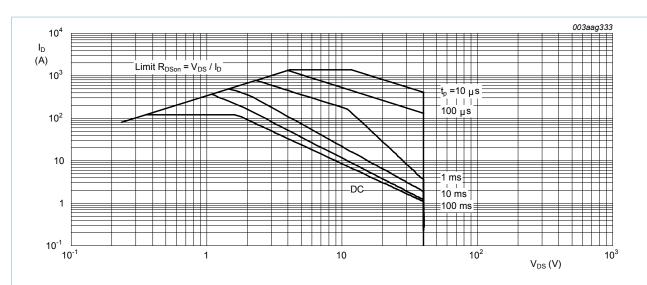
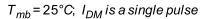


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



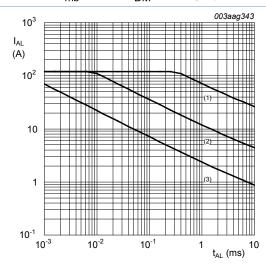


Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

(1) 
$$T_{j(init)} = 25$$
°C; (2)  $T_{j(init)} = 150$ °C; (3) Repetitive Avalanche

#### 9. Thermal characteristics

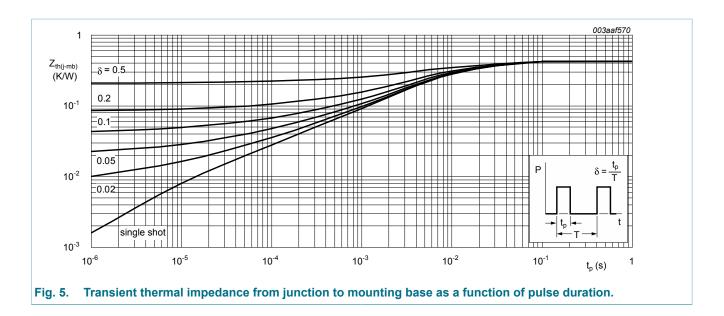
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	-	0.43	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

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## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		,			
$V_{(BR)DSS}$	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	40	-		V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^{\circ}C$	36	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.13	1	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	1.35	1.6	mΩ
	resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; Fig. 11	-	1.17	1.4	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 12; Fig. 11	-	-	3.1	mΩ
Dynamic ch	naracteristics		1			
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 5 V;	-	120	-	nC
Q <sub>GS</sub>	gate-source charge	Fig. 13; Fig. 14	-	26.9	-	nC

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$Q_{GD}$	gate-drain charge		-	40.9	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz;	-	12300	16400	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	1530	1840	pF
C <sub>rss</sub>	reverse transfer capacitance		-	740	1020	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	95	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$	-	118	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	195	-	ns
t <sub>f</sub>	fall time		-	119	-	ns
L <sub>D</sub>	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L <sub>S</sub>	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-dra	in diode					
$V_{SD}$	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <u>Fig. 16</u>	-	0.77	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S$ = 20 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V;	-	57	-	ns
Qr	recovered charge	V <sub>DS</sub> = 25 V	-	97	-	nC

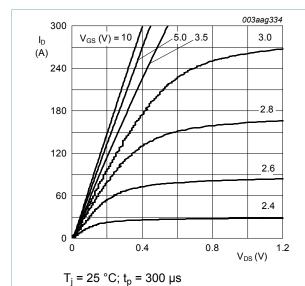


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

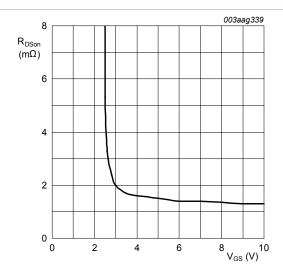


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values  $T_j = 25 \,^{\circ}C; I_D = 25A$ 

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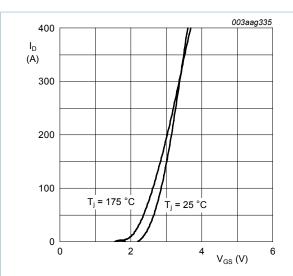


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



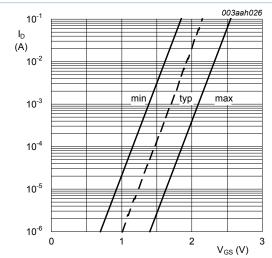


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

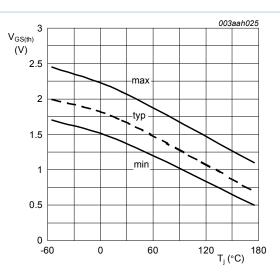
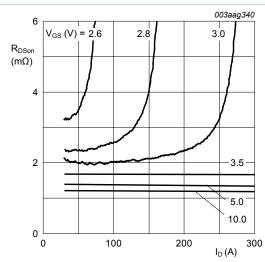


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA;  $V_{DS}$  =  $V_{GS}$ 



 $T_i$  = 25 °C;  $t_p$  = 300  $\mu s$ 

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

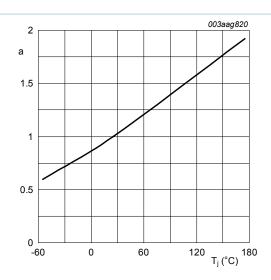


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25 \, ^{\circ}\text{C})}$$

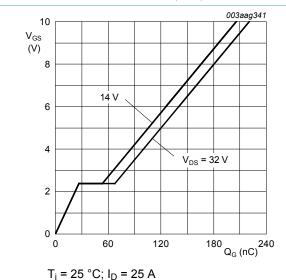


Fig. 14. Gate-source voltage as a function of gate charge; typical values

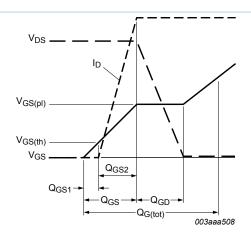


Fig. 13. Gate charge waveform definitions

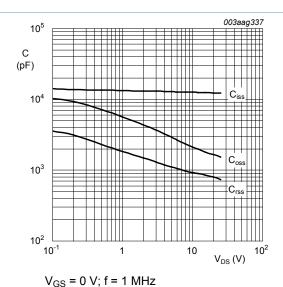
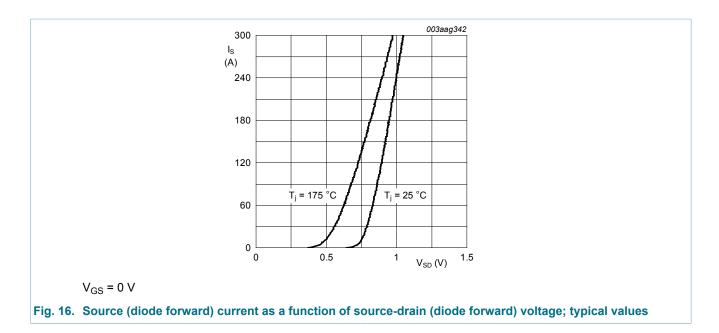
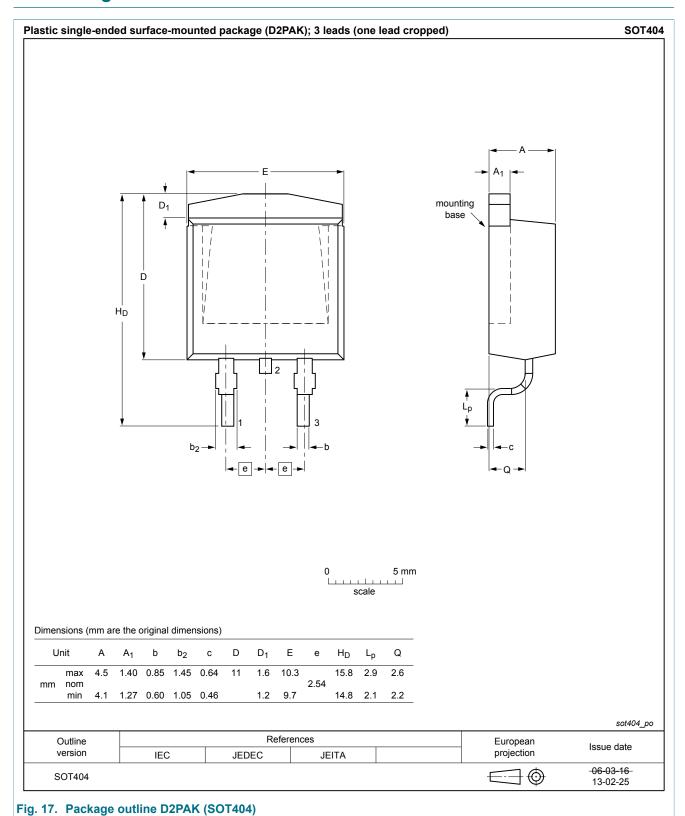


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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## 11. Package outline



### 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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