TPS78101EVM-339

This user's guide describes the characteristics, operation, and use of the TPS78101EVM-339 evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS78101 and TPS781330220 ultra low-power, low dropout (LDO) regulator with pin-selectable, dual-output voltage levels. The TPS78101 and TPS781330220 supply up to 150 mA of output current. The TPS78101 has an adjustable output voltage that can be changed with external feedback resistors. The TPS781330220 has a selectable dual level output voltage of 3.3 V (V_{SET}= low) or 2.2 V (V_{SET}=high) that can be changed with a digital input signal. The IC operates from a 2.2 V to 5.5 V input source. See the TPS781 data sheet (SBVS102) for definitive device specifications. This EVM user's guide includes setup instructions, schematic diagram, bill of materials (BOM), and PCB layout drawings.

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1 Introduction

The TPS78101EVM-339 evaluation module (EVM) assists designers in evaluating the operation and performance of the adjustable TPS78101 and the fixed TPS781330220 low dropout regulator (LDO). This LDO provides up to 150 mA of output current at a pin-programmable output while maintaining ultra-low quiescent current (I_Q=1000 nA). The board features the small 2 mm × 2 mm six-lead SON package (DRV) and the TSOT23-5 (DDC) package for small solution size.

Related Documentation from Texas Instruments

TPS781, Ultra Low-Power, 150mA Low Dropout Regulator, IQ 1000nA with Pin-Selectable, Dual Output Voltage Levels, data sheet (SBVS102)

2 Setup

Table 1 describes the jumpers and connectors on the EVM, as well as how to properly connect, set up, and use the TPS78101EVM-339.

Table 1. TPS78101EVM-339 Jumpers and Connections

Jumper	Connection Description	Connection Instructions
J1	U1 Input - VIN	Connect the positive lead of the input source to this input.
J2	U1 Input - GND	Connect the return lead of the input source to this input.
J3	U1 Output - VOUT	Connect the positive side of the load to this output.
J4	U1 Output - GND	Connect the ground side of the load to this output.
J5	U2 Input - VIN	Connect the positive lead of the input source to this input.
J6	U2 Input - GND	Connect the return lead of the input source to this input.
J7	U2 Output - VOUT	Connect the positive side of the load to this output.
J8	U2 Output - GND	Connect the ground side of the load to this output.
JP1	U1 EN	Enable input for the U1 device. Place a shunt across the H and EN pins of JP1 to enable U1. Place a shunt across the L and EN pins of JP1 to disable U1. A shunt must be installed on JP1 in either H or L positions and EN must not be left unconnected.
JP2	U1 V_{SET}/FB	This jumper is not used with this EVM in its default configuration. If the user modifies the EVM and replaces U1 with a fixed output voltage option, JP2 is used to change the output voltage between the two fixed output voltages.
JP3	U2 EN	Enable input for the U2 device. Place a shunt across the H and EN pins of JP3 to enable U2. Place a shunt across the L and EN pins of JP3 to disable U2. A shunt must be installed on JP1 in either H or L positions and EN should not be left unconnected.
JP4	U2 V_{SET}/FB	This jumper is used to program the output voltage. Place a shunt across the H and V_{SET} pins of JP4 to set the output of U2 to the default value of 2.2 V. Place a shunt across the L and V_{SET} pins of JP4 to the output of U2 to the default value of 3.3 V.

3 Operation

To setup the EVM Board operation

1. Connect the positive input power supply to the VIN pins on J1/J5.
2. Connect the input power return (ground) to the GND pins on J2/J6. The TPS78101EVM-339 has a maximum input voltage of 6 V. The recommended maximum operating input voltage is 5.5 V.
3. Connect the desired load between the VOUT (J3/J7) and GND (J4/J8). Each TPS781xxx supplies up to 150 mA of output current.
4. Configure jumpers JP1/JP3 and JP2/JP4 according to Table 1 and as required for your application. Additional versions of the TPS781xxx can be tested on this EVM by replacing U1 or U2 with the IC to be tested and appropriately configuring the resistors and jumpers on the PCB.

4 Test Results

This section provides typical performance waveforms (Figure 1 through Figure 4) using the TPS78101EVM-339 printed circuit board.

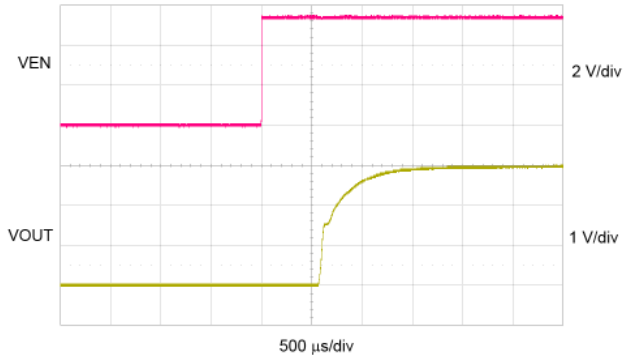

Figure 1. Startup from Enable, TPS78101, V_I=5.5 V, VOUT=3.0 V, R_{LOAD} = 22 Ω

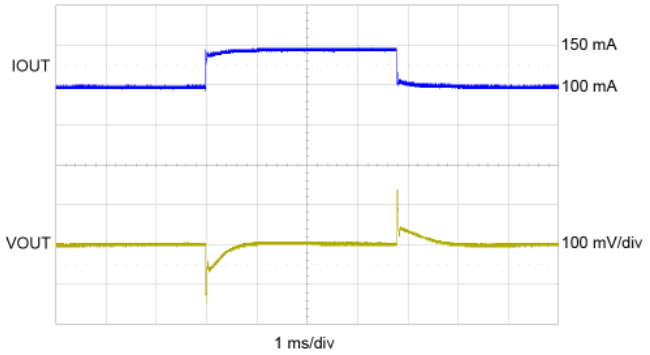

Figure 2. Load Transient, TPS78101, V_I = 3.6 V, VOUT = 3.0 V, IOUT = 100 mA to 150 mA to 100 mA

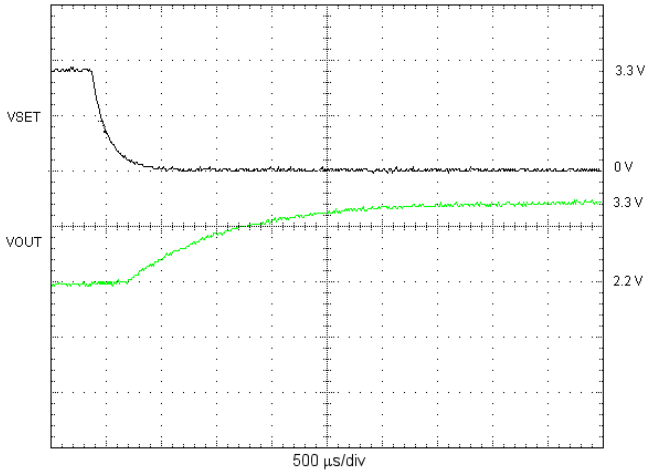

Figure 3. Low to High Output Transient, TPS781330220 (VOUT = 2.2 V to 3.3 V, R_{LOAD} = 22 Ω)

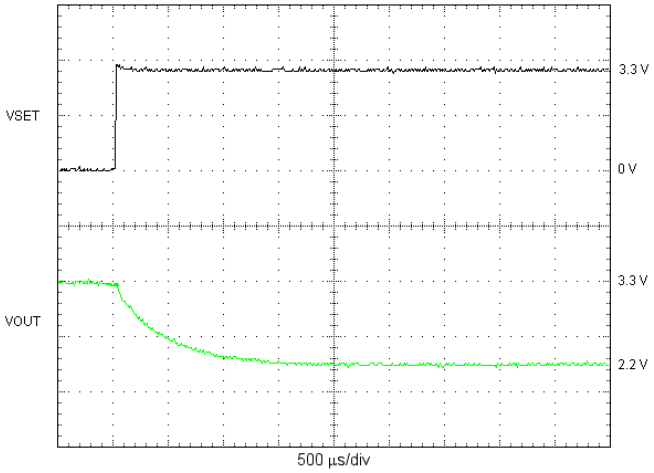

Figure 4. High to Low Output Transient, TPS781330220 (VOUT = 3.3 V to 2.2 V, R_{LOAD}= 22 Ω)

5 Board Layout, Schematic, and Bill of Materials

This section provides the TPS78101EVM-339 board layout, schematic, and bill of materials.

5.1 Board Layout

Board layout is critical for all power supplies. Without a carefully planned layout, the regulator could show poor performance or stability problems caused by incorrect routing of the PWB traces. All main current and return paths should use wide and short traces. The input and output capacitor should be placed as close as possible to the IC. Use a common ground node for power ground to minimize the effects of ground noise. Figure 5 through Figure 8 show the board layout for the TPS78101EVM PCB.

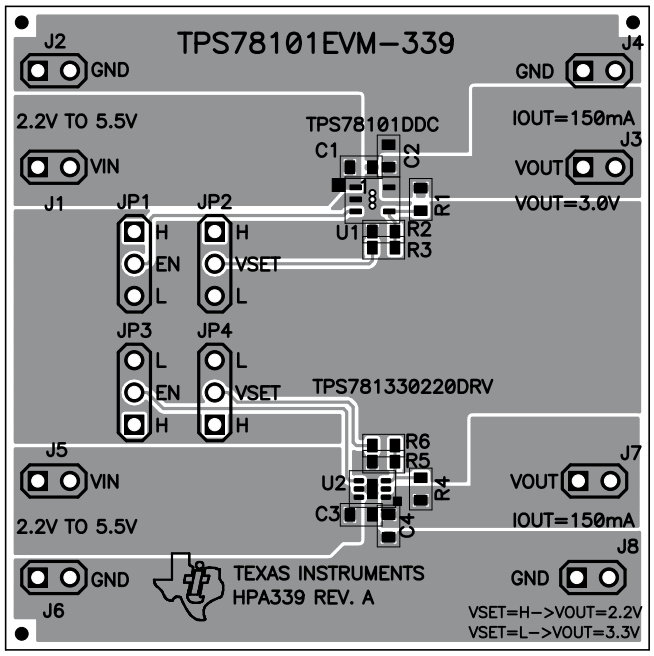

Figure 5. Top Assembly Layer

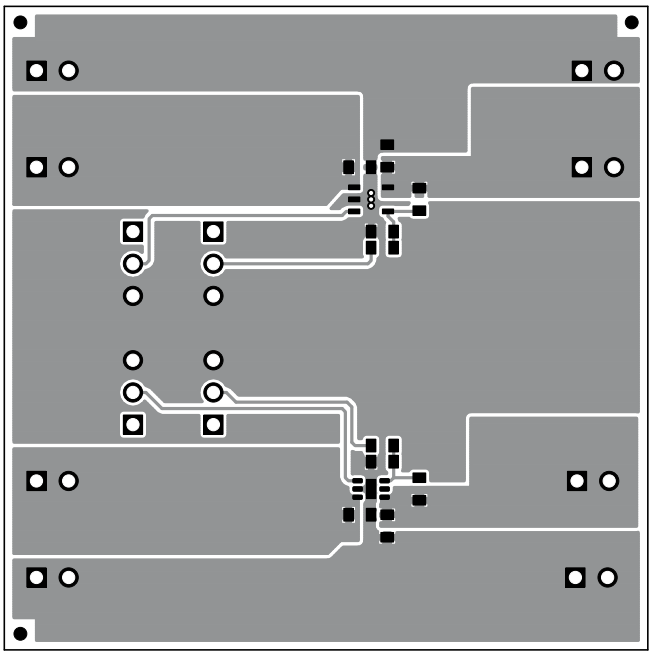

Figure 6. Top Layer

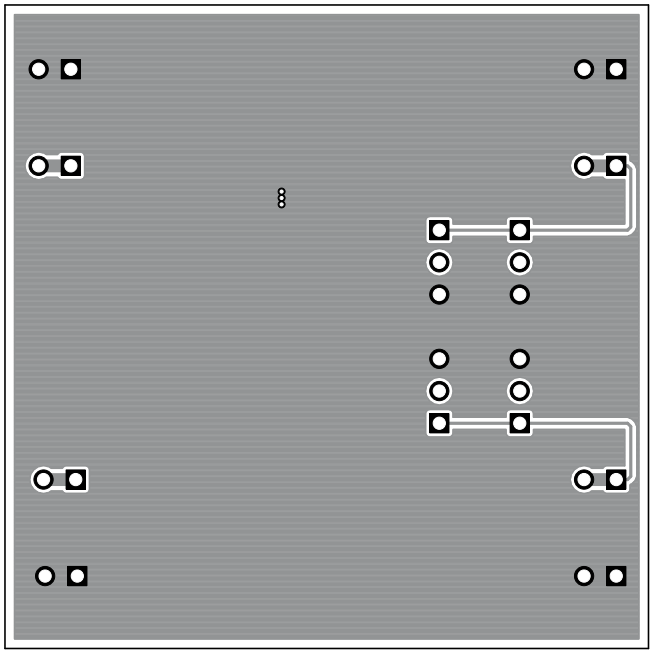

Figure 8. Bottom Layer

5.2 Schematic

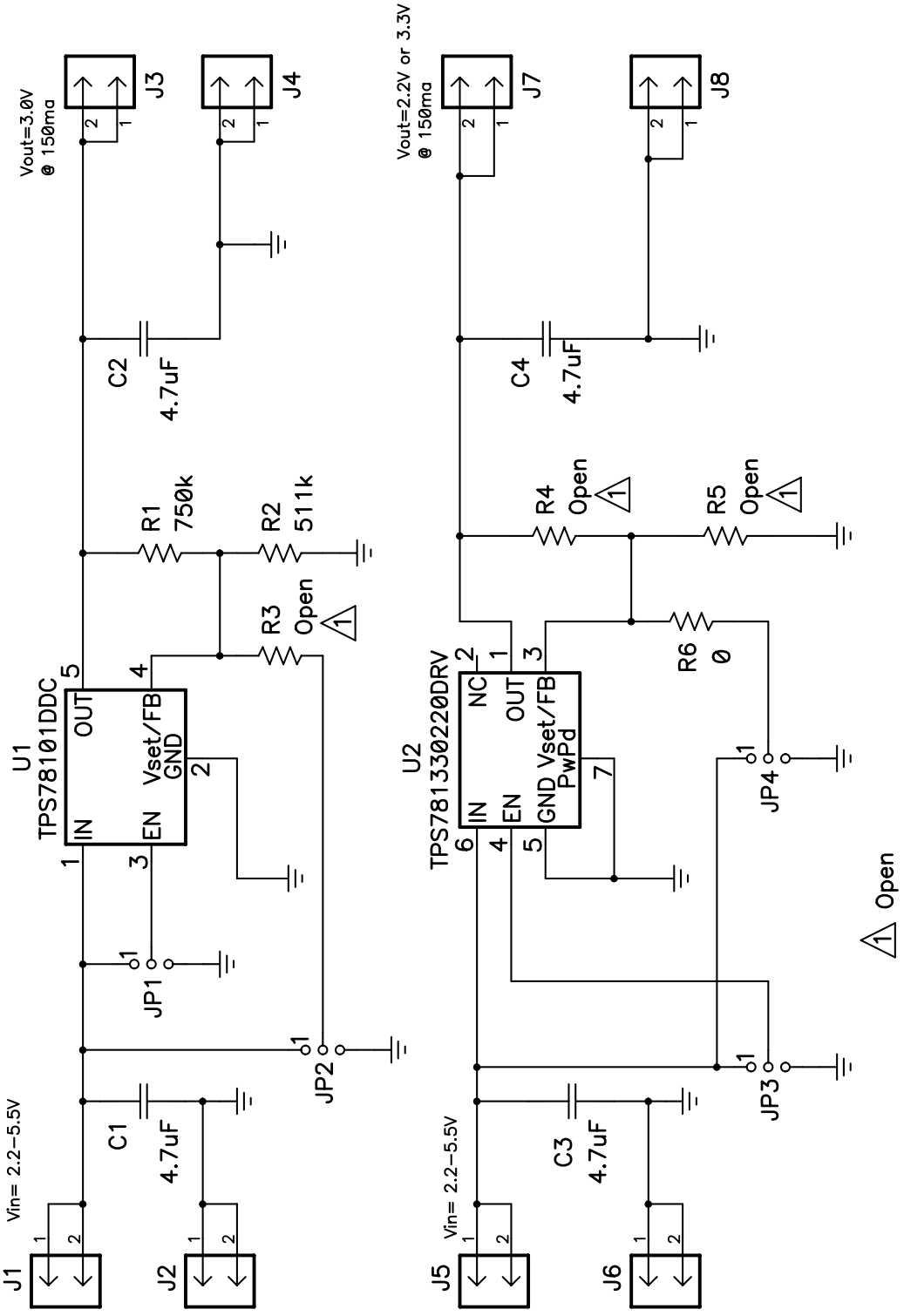

Figure 9. TPS78101EVM Schematic

5.3 Bill of Materials

Table 2. TPS78101EVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	Manufacturer
4	C1,C2, C3, C4	4.7 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	0603	GRM188R60J475KE19B	muRata
8	J1, J2, J3, J4, J5, J6, J7, J8	PTC36SAAN	Header, Male 2-pin, 100 mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins
4	JP1, JP2, JP3, JP4		Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 inch x 3	PTC36SAAN	Sullins
1	R1	750kohm	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	511kohm	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R4, R5	Open	Resistor, Chip, 1/16W, 1%	0603	N/A	Std
0	R6	0	Resistor, Chip, 1/16W	0603	Std	Std
4	–		Shunt, 100 mil, Black	0.1	929950-00	3M
1	U1	TPS78101DDC	IC, Dual OutPut LDO Linear Regulator Iq 500 nA With Pin-Selectable	TSOT23-5	TPS78101DDC	TI
1	U2	TPS781330220DRV	IC, Dual OutPut LDO Linear Regulator Iq 500 nA With Pin-Selectable	SON-6 (2mm x 2mm)	TPS781330220DRV	TI
1	–		PCB, 2 In x 2 In x 0.0062 In		HPA339	Any

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.2 V to 5.5 V and the output voltage range of 0.8 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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