8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

High−Performance Silicon−Gate CMOS

MC74HC595A

The MC74HC595A consists of an 8−bit shift register and an 8−bit D−type latch with three−state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8−bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The HC595A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - Improved Propagation Delays
  - 50% Lower Quiescent Power
  - Improved Input Noise and Latchup Immunity
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

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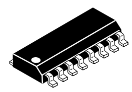
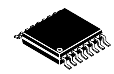
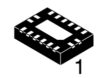


SOIC−16
D SUFFIX
CASE 751B

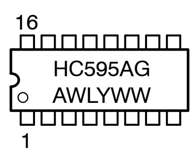


TSSOP−16
DT SUFFIX
CASE 948F

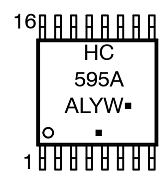


QFN16
MN SUFFIX
CASE 485AW

MARKING DIAGRAMS



SOIC−16



TSSOP−16

QFN16*

*V595A marking used for NLV74HC595AMN1TWG

A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G, ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

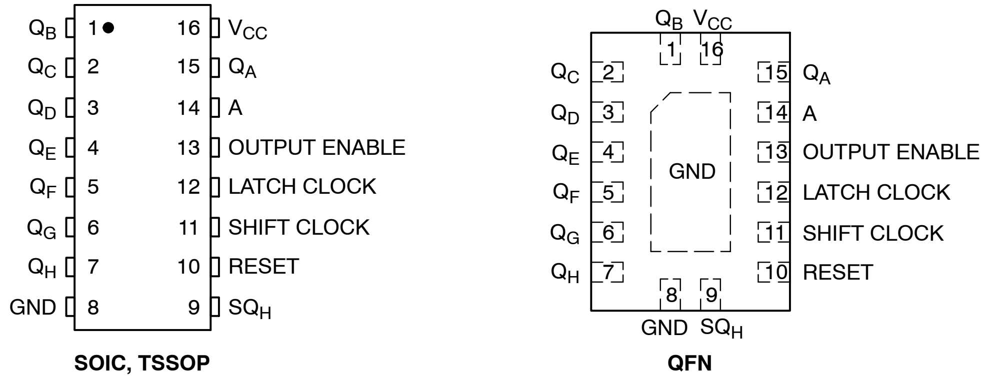
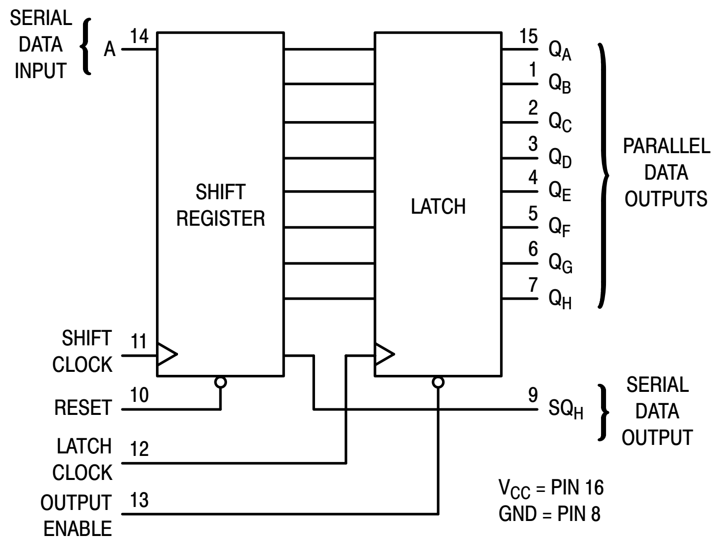


Figure 1. Pin Assignments

LOGIC DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC}+0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	 260	°C
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 3000 > 400 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: –6.1 mW/°C from 65° to 125°C

1. Tested to EIA/JESD22–A114–A.
2. Tested to EIA/JESD22–A115–A.
3. Tested to JESD22–C101–A.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit –55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert \le 20\ \mu A$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert \le 20\ \mu A$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage, Q_A – Q_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 2.4$ mA $\lvert I_{out} \rvert \le 6.0$ mA $\lvert I_{out} \rvert \le 7.8$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low−Level Output Voltage, Q_A – Q_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 2.4$ mA $\lvert I_{out} \rvert \le 6.0$ mA $\lvert I_{out} \rvert \le 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
V_{OH}	Minimum High−Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 2.4$ mA $\lvert I_{out} \rvert \le 4.0$ mA $\lvert i_{out} \rvert \le 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low−Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \le 2.4$ mA $\lvert I_{out} \rvert \le 4.0$ mA $\lvert i_{out} \rvert \le 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current, Q_A – Q_H	Output in High−Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	2.0 3.0 4.5 6.0	145 100 29 25	180 125 36 31	220 150 44 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to Q_A – Q_H (Figures 3 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q_A – Q_H (Figures 4 and 8)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q_A – Q_H (Figures 4 and 8)	2.0 3.0 4.5 6.0	135 90 27 23	170 110 34 29	205 130 41 35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Q_A – Q_H (Figures 3 and 7)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State), Q_A – Q_H	–	15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	300	pF

TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25°C to –55°C	≤ 85°C	≤ 125°C	Unit
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	75 60 15 13	95 70 19 16	110 80 22 19	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	60 45 12 10	75 60 15 13	90 70 18 15	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ_H	Parallel Outputs $Q_A - Q_H$
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	$D \rightarrow SR_A$; $SR_N \rightarrow SR_{N+1}$	U	$SR_G \rightarrow SR_H$	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	$SR_N \rightarrow LR_N$	U	SR_N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents   D = data (L, H) logic level   ↑ = Low–to–High   * = depends on Reset and Shift Clock inputs
LR = latch register contents   U = remains unchanged   ↓ = High–to–Low   ** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS

A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8–bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11)

Shift Register Clock Input. A low– to–high transition on this input causes the data at the Serial Input pin to be shifted into the 8–bit shift register.

Reset (Pin 10)

Active–low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8–bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low–to–high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active–low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A–Q_H) into the high–impedance state. The serial output is not affected by this control unit.

OUTPUTS

Q_A – Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3–state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8–bit shift register. This output does not have three–state capability.

SWITCHING WAVEFORMS

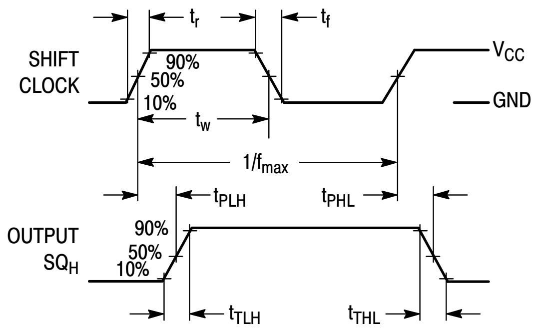


Figure 1.

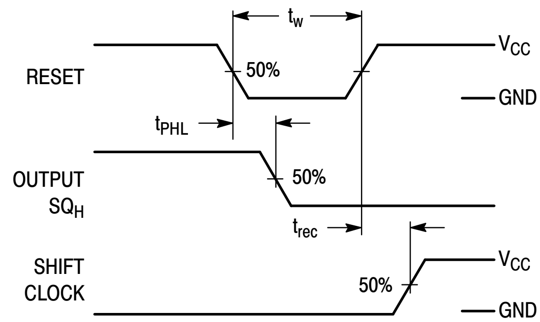


Figure 2.

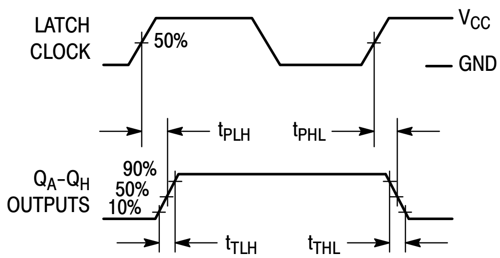


Figure 3.

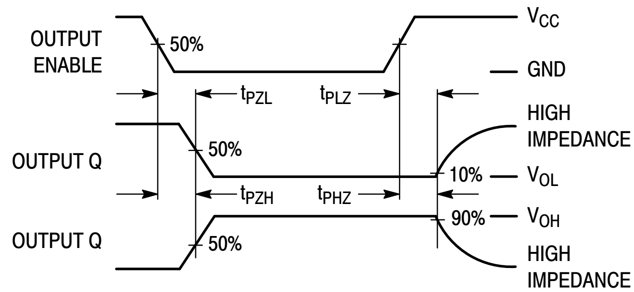


Figure 4.

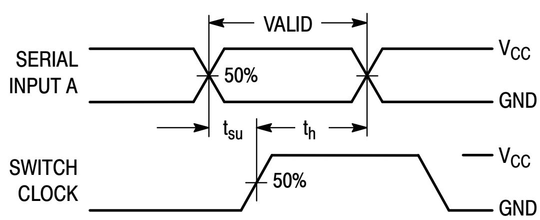


Figure 5.

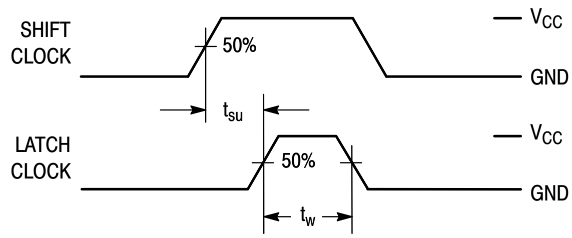
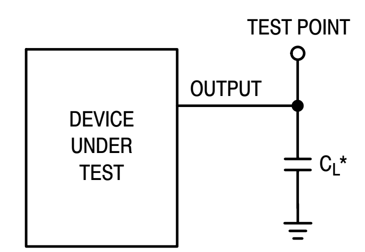


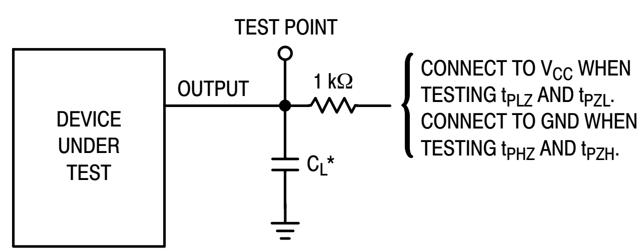
Figure 6.

TEST CIRCUITS



*Includes all probe and jig capacitance

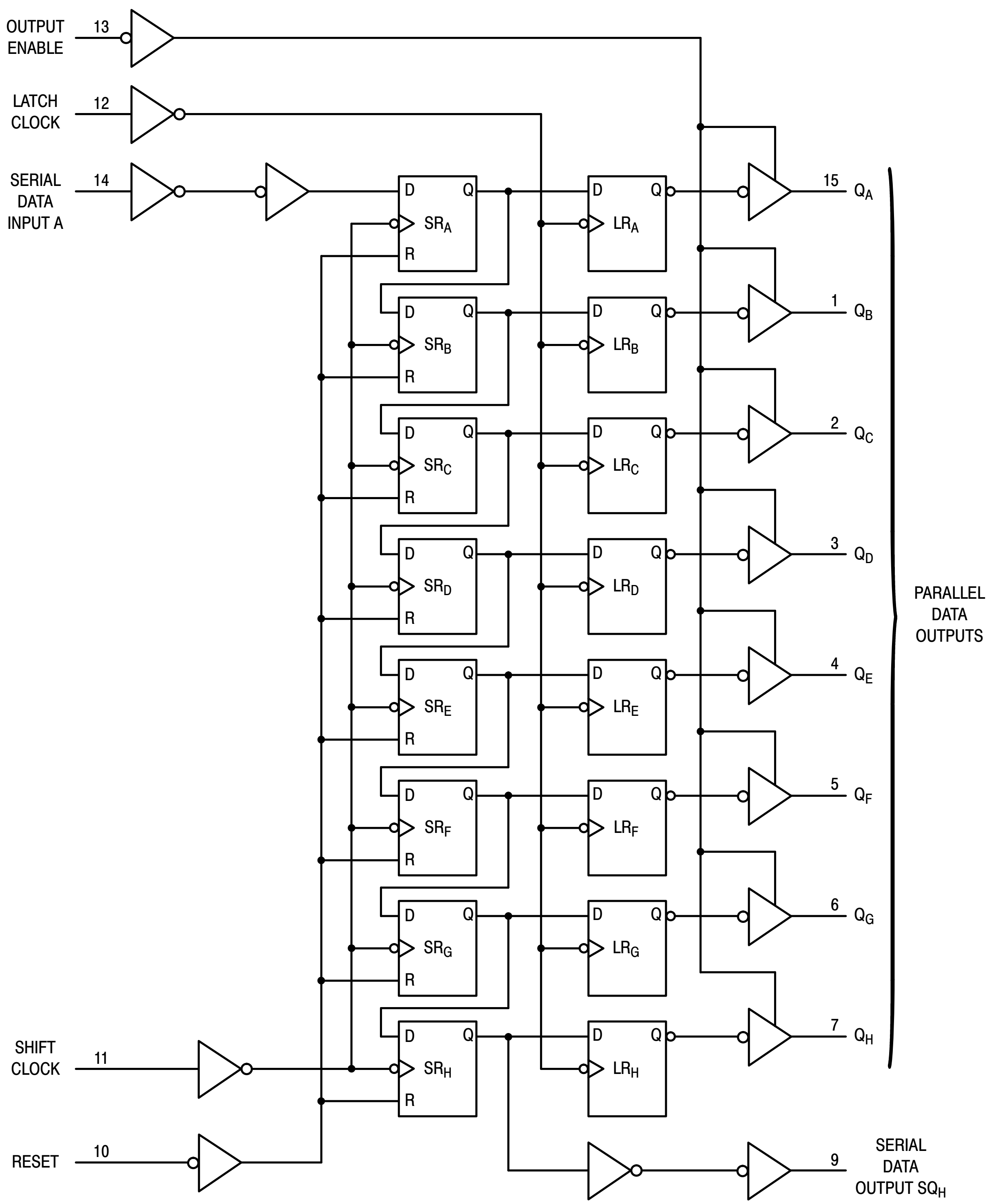
Figure 7.



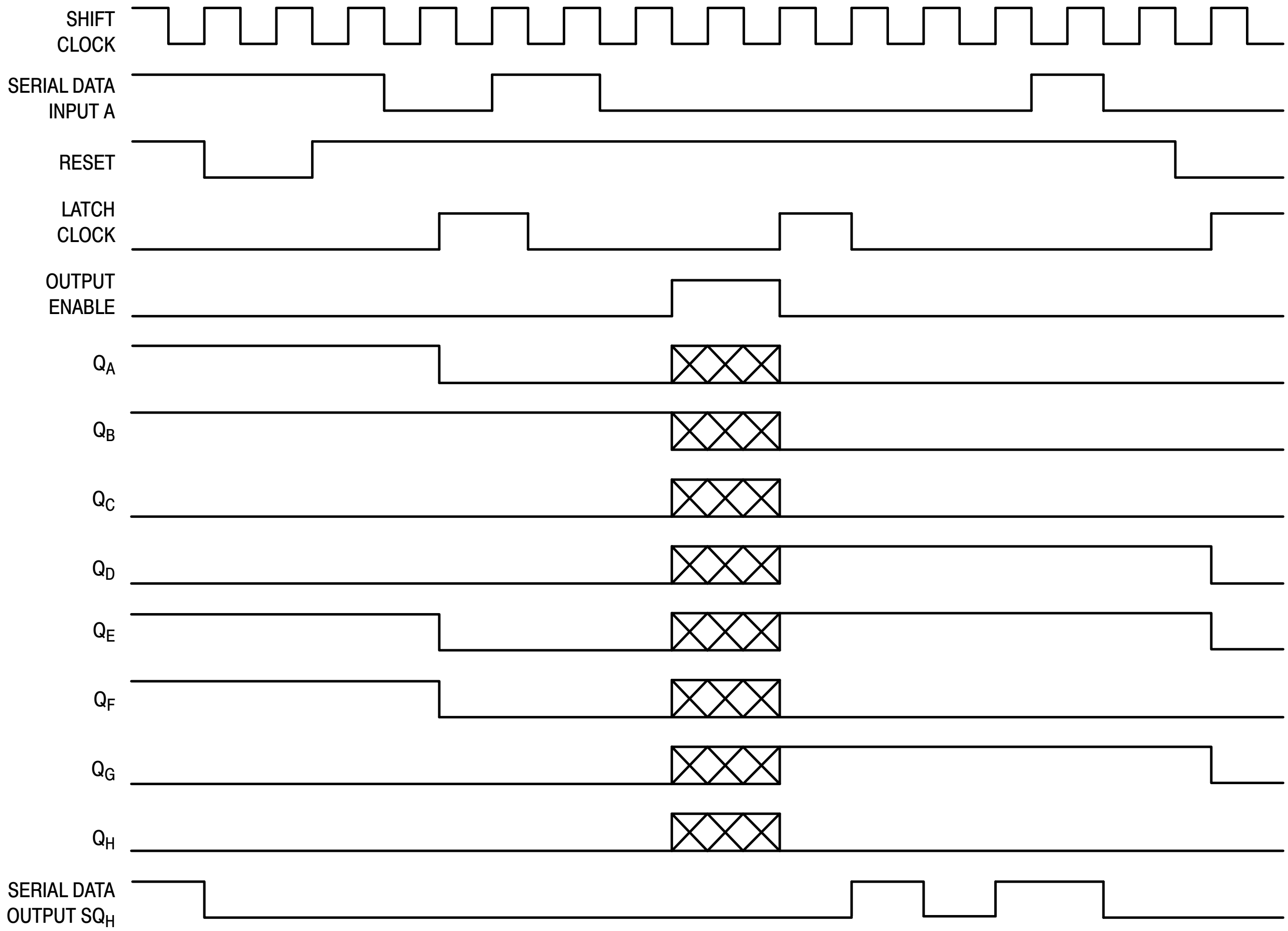
*Includes all probe and jig capacitance

Figure 8.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM

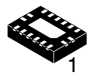


NOTE: [hatched box] implies that the output is in a high−impedance state.

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC595ADG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV74HC595ADG*		48 Units / Rail
MC74HC595ADR2G		2500 / Tape & Reel
NLV74HC595ADR2G*		2500 / Tape & Reel
MC74HC595AADR2G		2500 / Tape & Reel
NLV74HC595AADR2G* (Contact ON Semiconductor)		2500 / Tape & Reel
MC74HC595ADTG	TSSOP−16 (Pb−Free)	96 Units / Tube
NLV74HC595ADTG*		96 Units / Tube
MC74HC595ADTR2G		2500 / Tape & Reel
NLV74HC595ADTR2G*		2500 / Tape & Reel
NLV74HC595AADTR2G*		2500 / Tape & Reel
MC74HC595AMNTWG#	QFN16 (Pb−Free)	3000 / Tape & Reel
NLV74HC595AMNTWG*#		3000 / Tape & Reel
NLV74HC595AMN1TWG*#		3000 / Tape & Reel

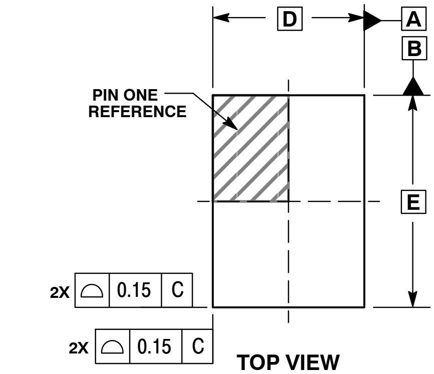
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
#MN suffix is with pull−back lead, MN1 is without pull−back lead. Refer to 'Detail A' of case outline on page 13.



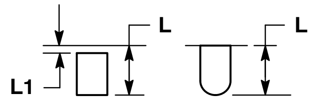
SCALE 2:1

QFN16, 2.5x3.5, 0.5P
CASE 485AW−01
ISSUE O

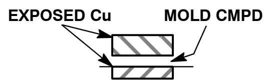
DATE 11 DEC 2008



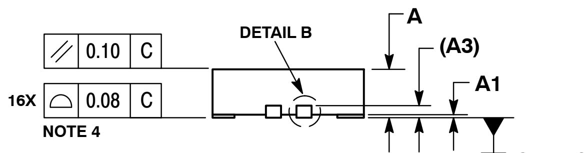
TOP VIEW



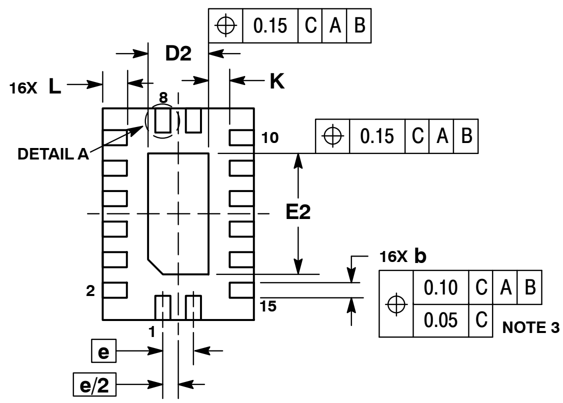
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS



SIDE VIEW

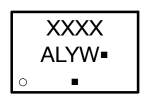


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*

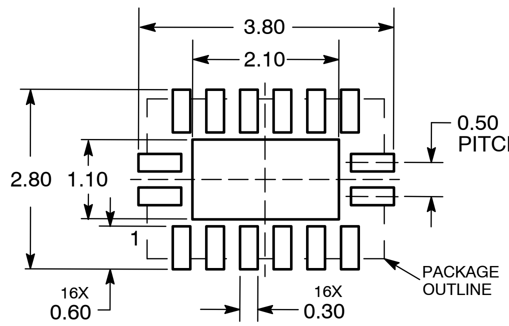


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

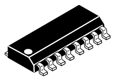
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

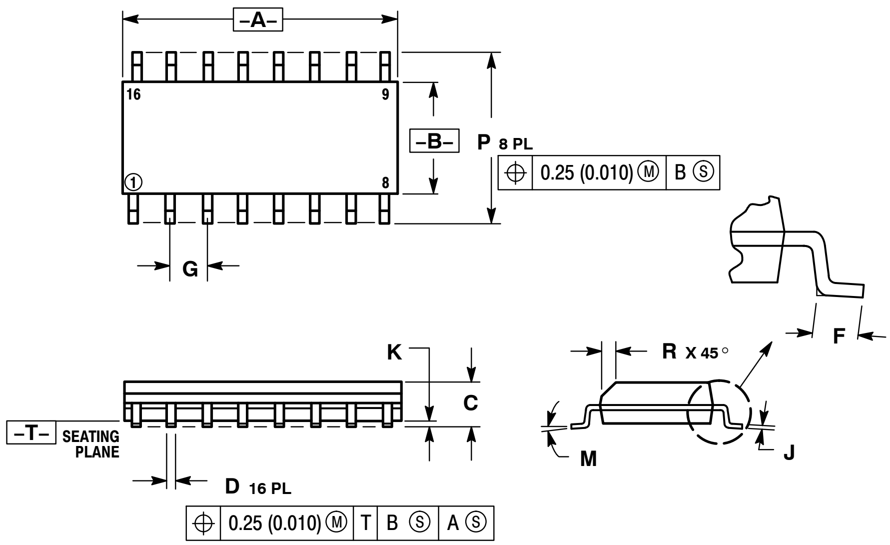
DOCUMENT NUMBER:	**98AON36347E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN16, 2.5X3.5, 0.5P**	**PAGE 1 OF 1**



SCALE 1:1

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

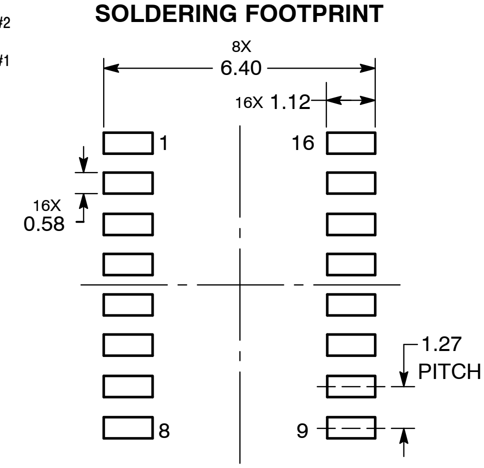
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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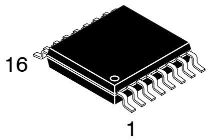
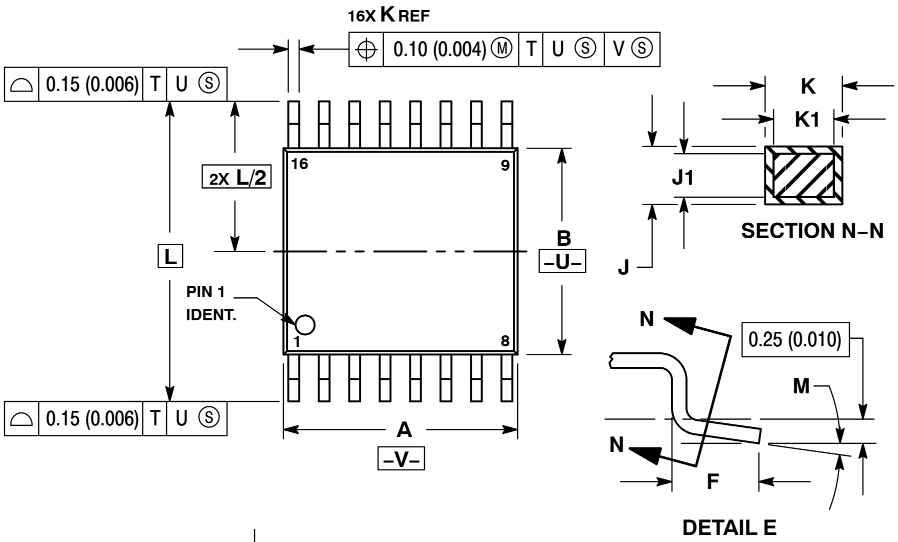
DESCRIPTION:	SOIC−16	PAGE 1 OF 1

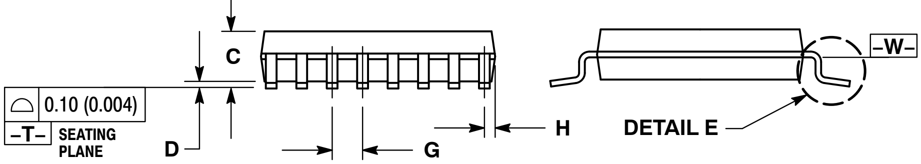


SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

DATE 19 OCT 2006

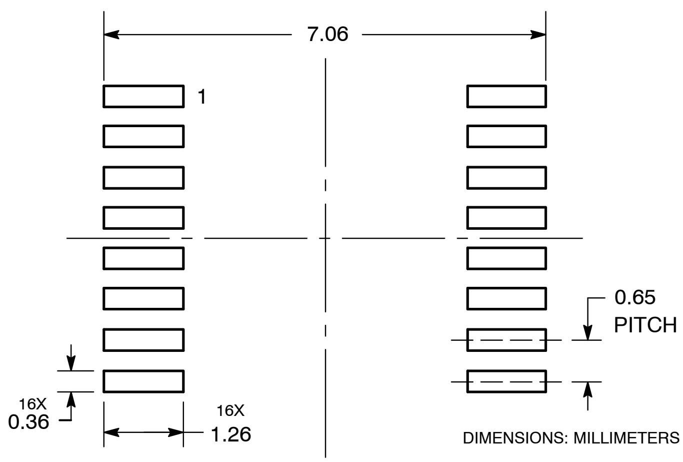




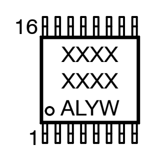
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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