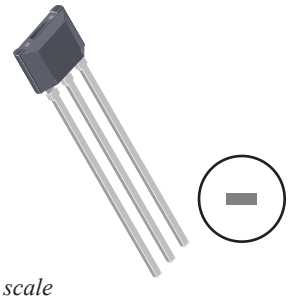
Chopper-Stabilized, Two-Wire Hall-Effect Latch

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- High-speed, 4-phase chopper stabilization
  - Low switchpoint drift throughout temperature range
  - Low sensitivity to thermal and mechanical stresses
- On-chip protection
  - Supply transient protection
  - Reverse-battery protection
- On-board voltage regulator
  - 3 to 24 V operation
- Solid-state reliability
- Robust EMC and ESD performance
- Industry-leading ISO 7637-2 performance through use of proprietary, 40 V clamping structures

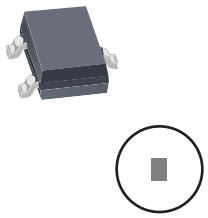
PACKAGES:

3-pin ultra-mini SIP
1.5 mm × 4 mm × 3 mm
(suffix UA)



Not to scale

3-pin SOT23-W
2 mm × 3 mm × 1 mm
(suffix LH)



Approximate footprint

DESCRIPTION

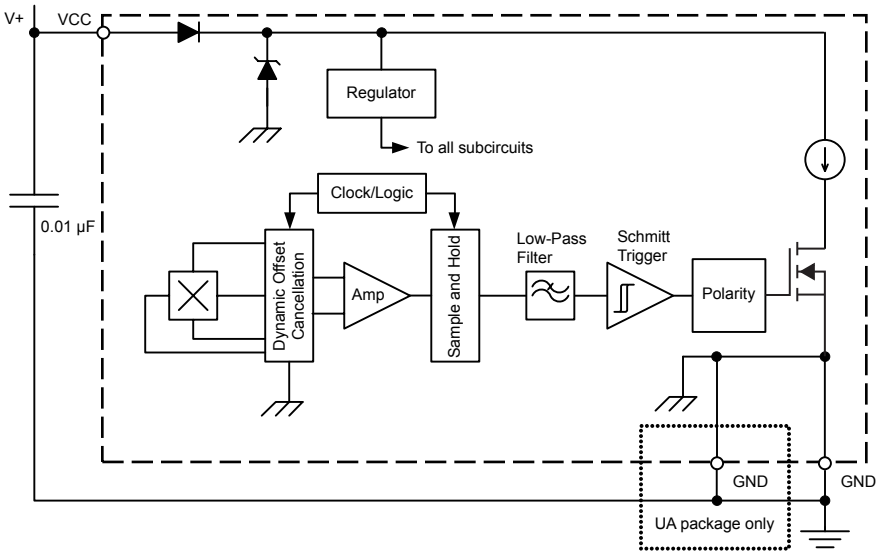
The A1244 is a two-wire Hall-effect latch. The devices are produced on the Allegro™ advanced BiCMOS wafer fabrication process, which implements a high-frequency, 4-phase, chopper stabilization technique. This technique achieves magnetic stability over the full operating temperature range, and eliminates offsets inherent in devices with a single Hall element that are exposed to harsh application environments.

Two-wire latches are particularly advantageous in cost-sensitive applications because they require one less wire for operation versus the more traditional open-collector output switches. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges. Any current level not within these ranges indicates a fault condition.

The Hall-effect latch will be in the high output current state in the presence of a magnetic south polarity field of sufficient magnitude and will remain in this state until a sufficient north polarity field is present.

The device is offered in two package styles. The LH is a SOT-23W style, miniature low-profile package for surface-mount applications. The UA is a 3-pin ultra-mini single inline package (SIP) for through-hole mounting. Both packages are lead (Pb) free, with 100% matte-tin leadframe plating.

Functional Block Diagram



SELECTION GUIDE

Part Number	Packing [1]	Package	Operating Ambient Temperature, T_A (°C)	Supply Current at $I_{CC(L)}$ (mA)
A1244LLHLT-I1-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40 to 150	5 to 6.9
A1244LLHLX-I1-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	–40 to 150	5 to 6.9
A1244LLHLT-I2-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40 to 150	2 to 5
A1244LLHLX-I2-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	–40 to 150	2 to 5
A1244LUA-I1-T	Bulk, 500 pieces/bag	3-pin SIP through hole	–40 to 150	5 to 6.9
A1244LUA-I2-T	Bulk, 500 pieces/bag	3-pin SIP through hole	–40 to 150	2 to 5

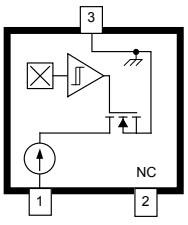
[1] Contact Allegro™ for additional packing options.

ABSOLUTE MAXIMUM RATINGS

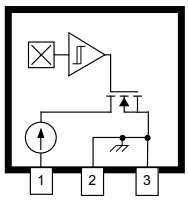
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage [2]	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[2] This rating does not apply to extremely short voltage transients such as Load Dump and/or ESD. Those events have individual ratings, specific to the respective transient voltage event.

Pinout Diagrams



LH Package
3-pin SOT23W



UA Package
3-pin SIP

Terminal List Table

Name	Number		Function
	LH	UA	
VCC	1	1	Connects power supply to chip
NC	2	–	No connection
GND	3	2, 3	Ground

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ELECTRICAL CHARACTERISTICS: Valid at T_A = –40°C to 150°C, $T_J < T_J$(max), C_{BYP} = 0.01 µF, through operating supply voltage range, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage [1][2]	V_{CC}	Operating, $T_J \le$ 165°C	3.0	–	24	V
Supply Current	$I_{CC(L)}$	-I1 $B < B_{RP}$	5	–	6.9	mA
		-I2 $B < B_{RP}$	2	–	5	mA
	$I_{CC(H)}$	$B > B_{OP}$	12	–	17	mA
Supply Zener Clamp Voltage	$V_{Z(sup)}$	$I_{CC(L)}$(max) + 3 mA, T_A = 25°C	28	–	–	V
Supply Zener Clamp Current	$I_{Z(sup)}$	$V_{Z(sup)}$ = 28 V	–	–	$I_{CC(L)}$(max) + 3 mA	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –18 V	–	–	–1.6	mA
Output Slew Rate [3]	di/dt	No bypass capacitor, capacitance of probe C_S = 20 pF	–	90	–	mA/µs
Chopping Frequency	f_c		–	700	–	kHz
Power-Up Time [2][4][5]	t_{on}		–	–	25	µs
Power-Up State [4][6][7]	POS	$t_{on} < t_{on}$(max), V_{CC} slew rate > 25 mV/µs	–	$I_{CC(H)}$	–	–

[1] V_{CC} represents the generated voltage between the VCC pin and the GND pin.
[2] The V_{CC} slew rate must exceed 600 mV/ms from 0 to 3 V. A slower slew rate through this range can affect device performance.
[3] Measured without bypass capacitor between VCC and GND. Use of a bypass capacitor results in slower current change.
[4] Power-Up Time is measured without and with bypass capacitor of 0.01 µF, $B < B_{RP}$ – 10 G. Adding a larger bypass capacitor would cause longer Power-Up Time.
[5] Guaranteed by characterization and design.
[6] Power-Up State as defined is true only with a V_{CC} slew rate of 25 mV/µs or greater.
[7] For $t > t_{on}$ and $B_{RP} < B < B_{OP}$, Power-Up State is not defined.

MAGNETIC CHARACTERISTICS [8]: Valid at T_A = –40°C to 150°C, $T_J < T_J$ (max), unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [9]
Magnetic Operating Point	B_{OP}		5	–	80	G
Magnetic Release Point	B_{RP}		–80	–	–5	G
Hysteresis	B_{HYS}	$B_{OP} - B_{RP}$	40	–	110	G

[8] Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).
[9] 1 G (gauss) = 0.1 mT (millitesla).

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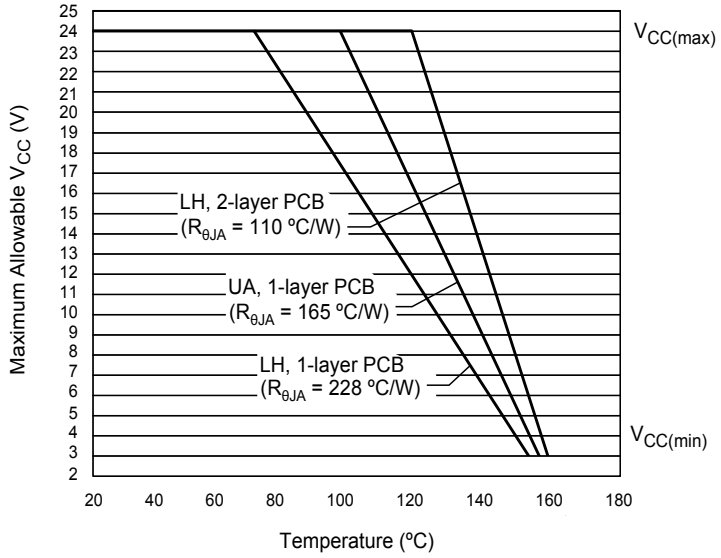
THERMAL CHARACTERISTICS

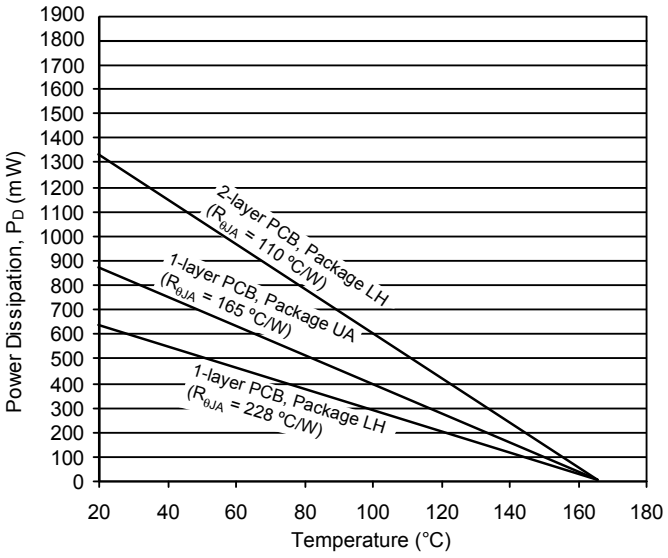
Characteristic	Symbol	Test Conditions [1]	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

[1] Additional thermal information available on Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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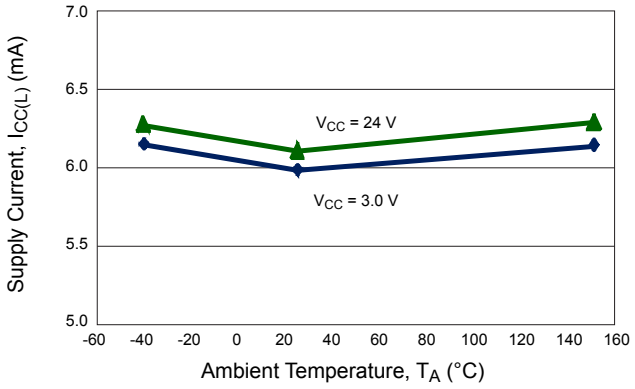
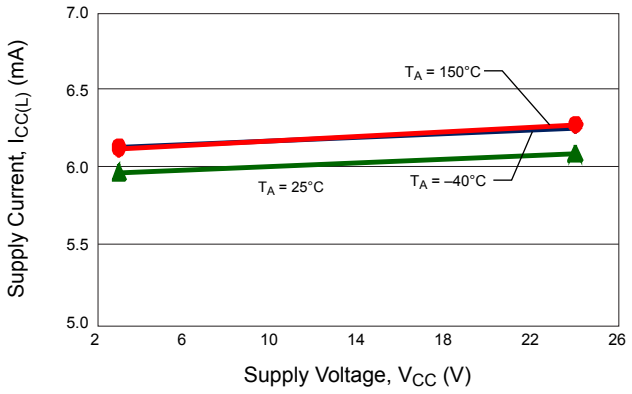
CHARACTERISTIC PERFORMANCE

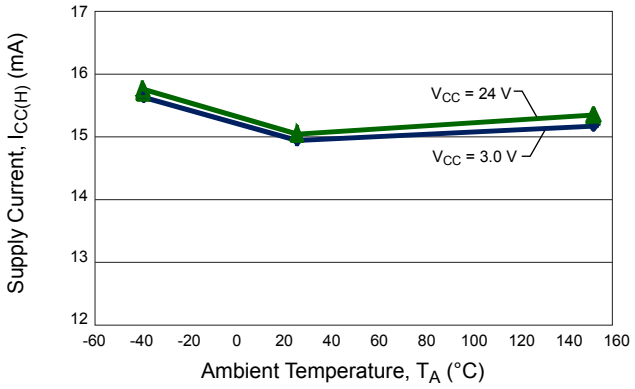
A1244-I1
Average Supply Current (Low) versus Temperature



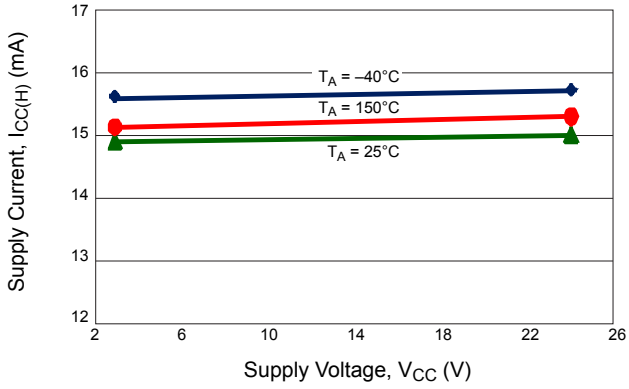
A1244-I1
Average Supply Current (Low) versus Supply Voltage



A1244-I1,I2
Average Supply Current (High) versus Temperature



A1244-I1,I2
Average Supply Current (High) versus Supply Voltage



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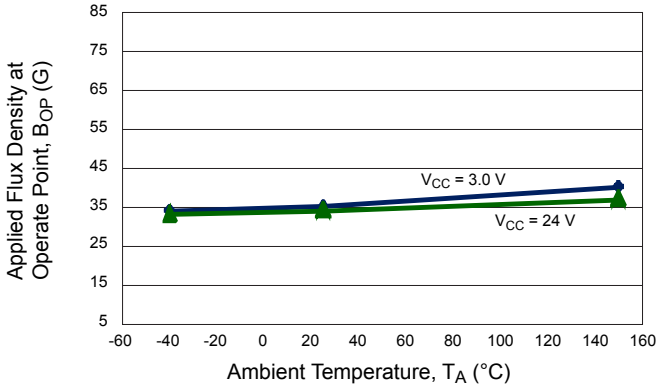
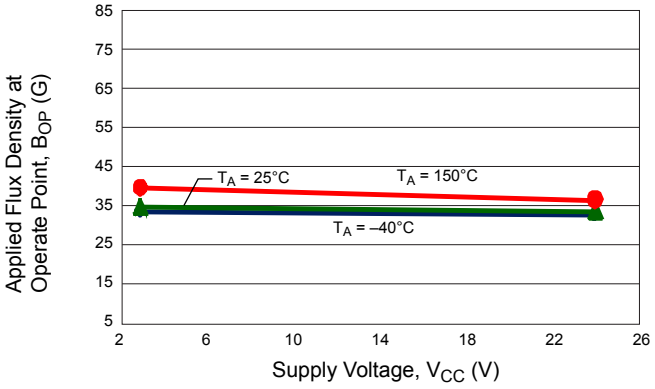
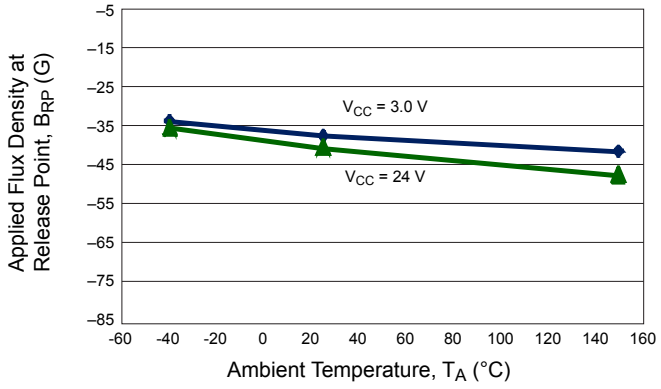
A1244-I1,I2
Average Operate Point versus Temperature



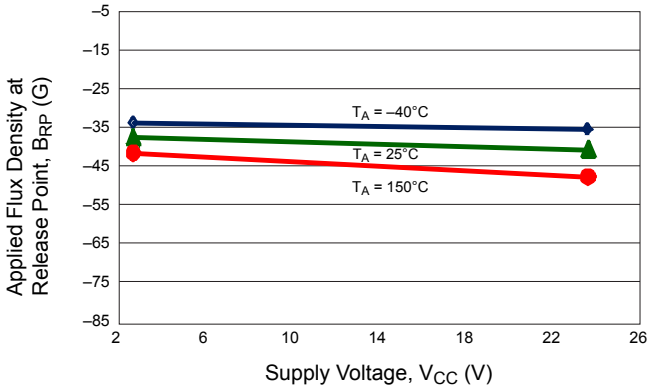
A1244-I1,I2
Average Operate Point versus Supply Voltage



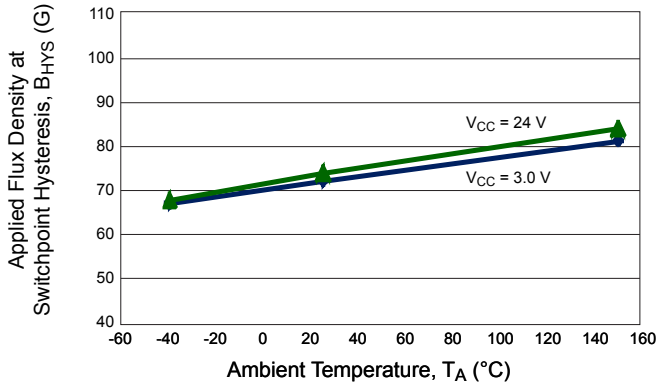
A1244-I1,I2
Average Release Point versus Temperature



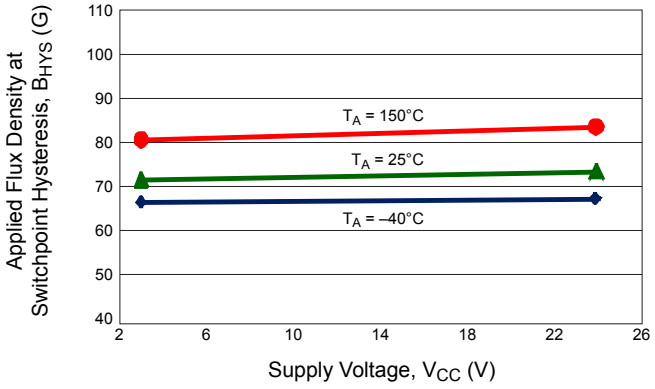
A1244-I1,I2
Average Release Point versus Supply Voltage



A1244-I1,I2
Average Switchpoint Hysteresis versus Temperature



A1244-I1,I2
Average Switchpoint Hysteresis versus Supply Voltage



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FUNCTIONAL DESCRIPTION

The A1244 output, I_{CC}, switches high after the magnetic field at the Hall sensor IC exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output goes low. This is shown in figure 1.

The difference between the magnetic operate and release points is called the hysteresis of the device, B_{HYS}. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

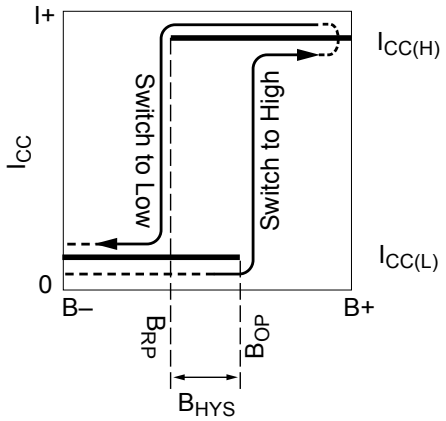
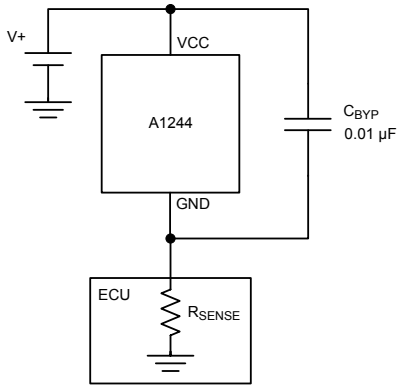


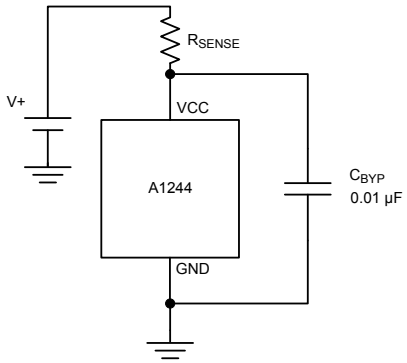
Figure 1. Hysteresis for the A1244. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

APPLICATION INFORMATION

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to guarantee correct performance under harsh environmental conditions and to reduce noise from internal circuitry.



(A) Low-side sensing



(B) High-side sensing

Figure 2. Typical application circuits

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 350 kHz high-frequency clock. For demodulation process, a sample-and-hold technique is used, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

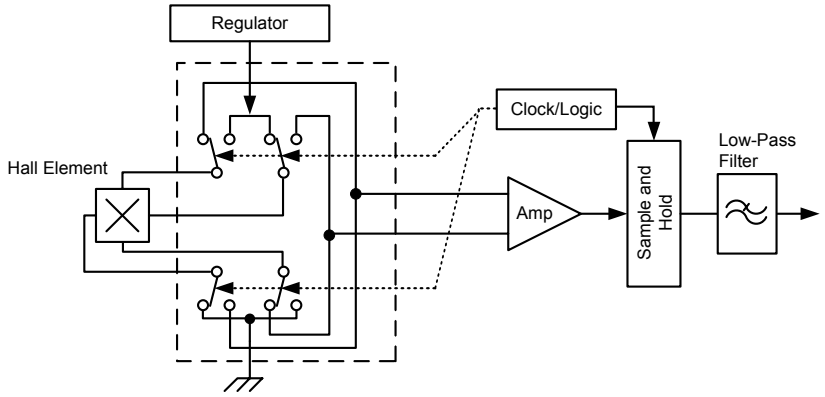

Figure 3. Chopper stabilization circuit (Dynamic Quadrature Offset Cancellation)

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Power Derating

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 140°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140°C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level (V_{CC}(max), I_{CC}(max)), without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package LH, using a low-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=110°C/W, T_J(max) = 165°C, V_{CC}(max) = 24 V, and I_{CC}(max) = 17 mA.

Calculate the maximum allowable power level, P_D(max). First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 110°C/W = 136\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_D(max) \div I_{CC}(max) = 136\ mW \div 17\ mA = 8\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to V_{CC}(max). If $V_{CC(est)} \leq V_{CC}$(max), then reliable operation between $V_{CC(est)}$ and V_{CC}(max) requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC}$(max), then operation between $V_{CC(est)}$ and V_{CC}(max) is reliable under these conditions.

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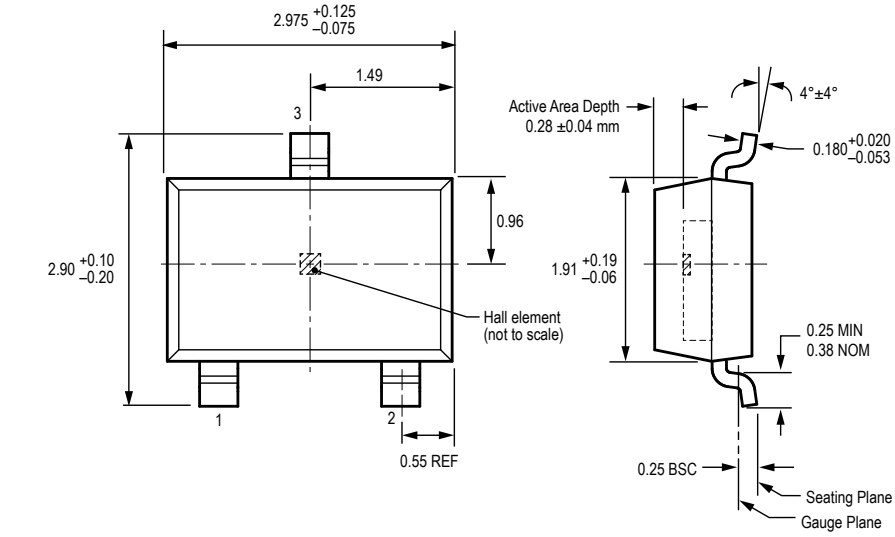
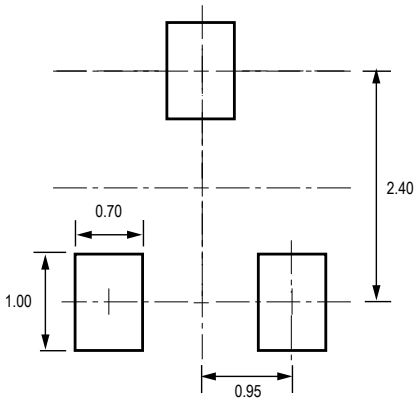
Package LH, 3-Pin SOT23W

For Reference Only – Not for Tooling Use

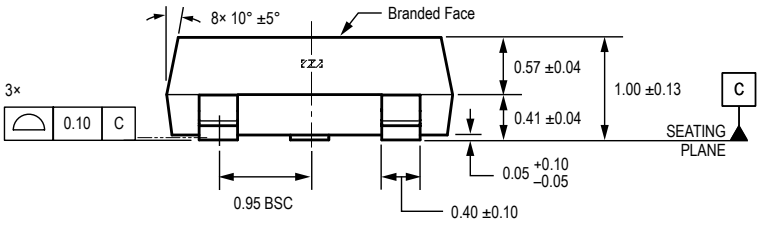
(Reference Allegro DWG-0000628, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

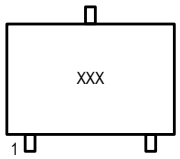




PCB Layout Reference View

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances





Standard Branding Reference View 1

Line 1: Last three digits of device part number

Branding scale and appearance at supplier discretion

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Package UA, 3-Pin SIP

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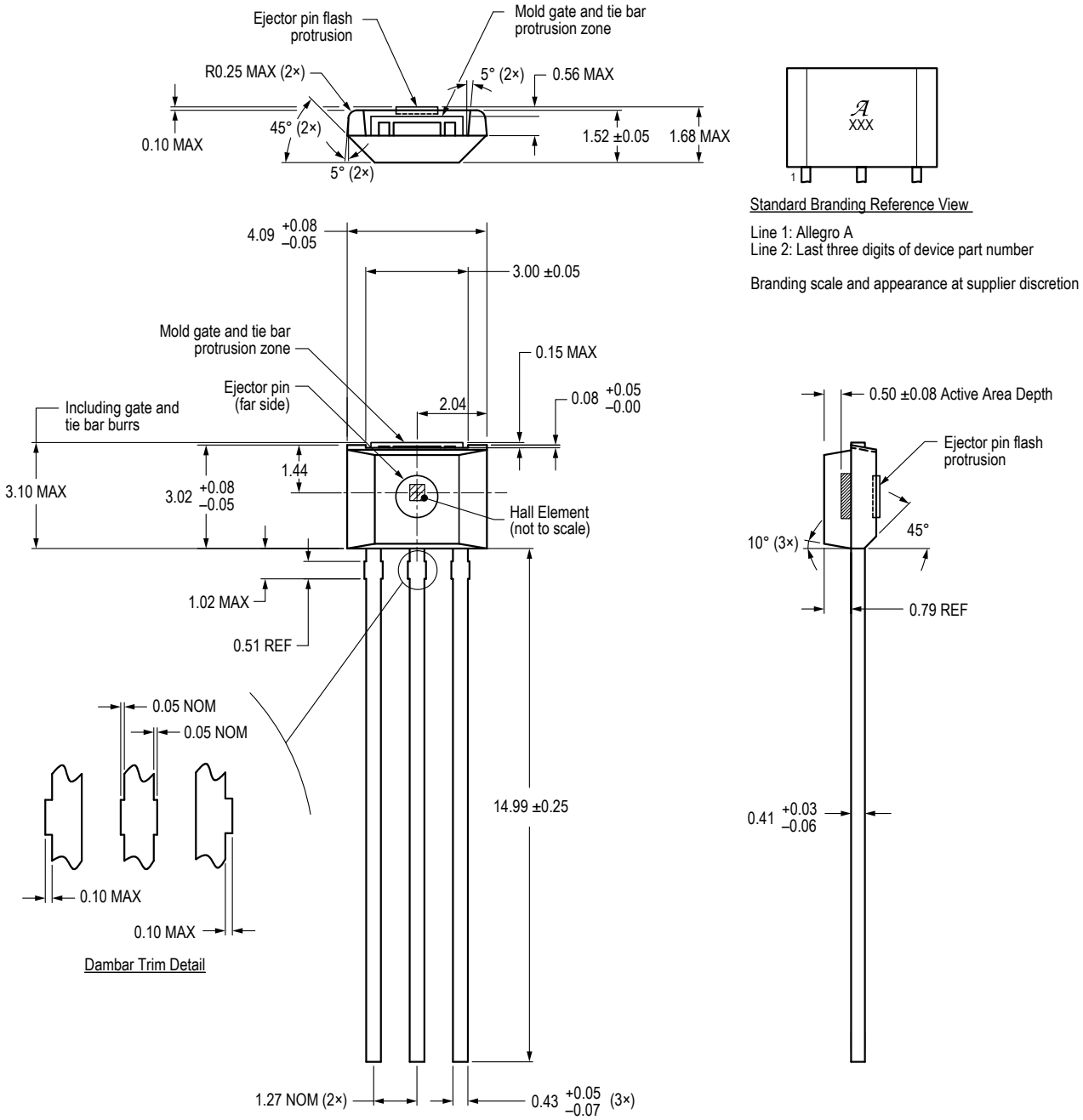
(Reference DWG-0000404, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



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REVISION HISTORY

Number	Date	Description
1	July 12, 2012	Update package drawing
2	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
3	May 19, 2017	Added “LT” tape and reel packing option
4	May 19, 2018	Minor editorial updates
5	July 2, 2019	Minor editorial updates
6	July 21, 2022	Updated package drawings (pages 10-11)

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