CIPOS™ Micro IPM 600 V, 4 A

IM241 Series

Description

IM241-M6 is a 3-phase Intelligent Power Module (IPM) designed for high-efficiency appliance motor drives such as fans and pumps. This IPM is available in both fast and slow speeds for low loss and low EMI operation respectively.

Features

- 600V 3-phase inverter including gate drivers & bootstrap function
- Reverse Conducting IGBT Gen 2 (RCD2) optimized for motor drives
- Temperature monitor
- Accurate overcurrent shutdown (±5%)
- Fault reporting and programmable fault clear
- Advanced input filter with shoot-through protection
- Optimized dV/dt for loss and EMI trade offs
- Open-emitter for single and leg-shunt current sensing
- 3.3V logic compatible
- Isolation 2000VRMS, 1min

SOP 29x12 DIP 29x12

Potential Applications

- Fans
- Pumps

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product Information

Base Part Number	Package Type	Standard Pack	
		Form	**Quantity**
IM241-M6T2*y*	DIP 29x12	Tube	240
IM241-M6S1*y*	SOP 29x12	Tube	240
		Tape & Reel	500

y = B (fast speed for low losses; for x = S, M, L) or J (slow speed for low EMI; for *x* = S, M)

Table of contents

1 Internal Electrical Schematic

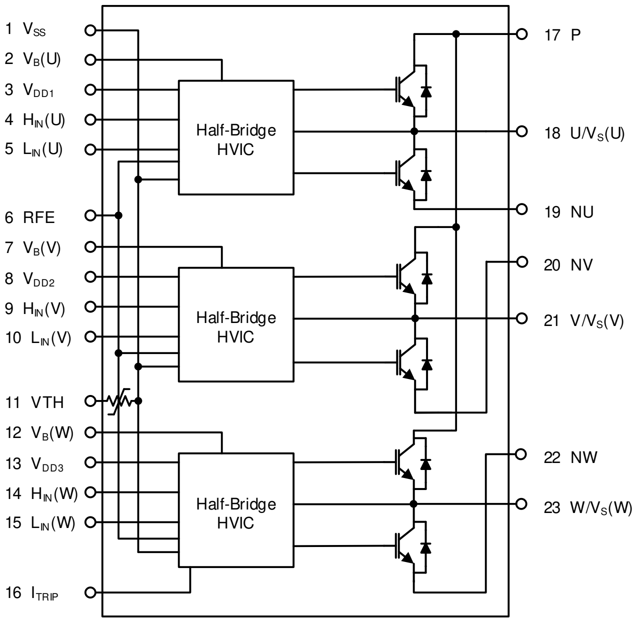


Figure 1 Internal electrical schematic.

2 Pin Configuration

2.1 Pin Assignment

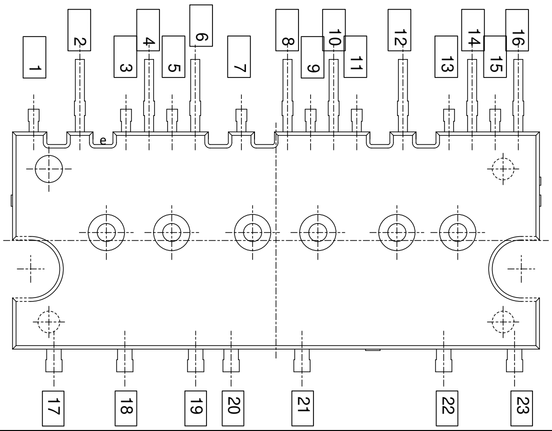


Figure 2 Module pinout

Table 2 Pin Assignment

Pin	Name	Description
1	V_{SS}	Logic ground
2	V_B(U)	U-phase high-side floating IC supply voltage
3	V_{DD1}	Low-side control supply 1
4	H_{IN}(U)	U-phase high-side gate driver input
5	L_{IN}(U)	U-phase low-side gate driver input
6	RFE	RCIN / Fault / Enable
7	V_B(V)	V-phase high-side floating IC supply voltage
8	V_{DD2}	Low-side control supply 2
9	H_{IN}(V)	V-phase high-side gate driver input
10	L_{IN}(V)	V-phase low-side gate driver input
11	VTH	Thermistor output
12	V_B(W)	W-phase high-side floating IC supply voltage
13	V_{DD3}	Low-side control supply 3
14	H_{IN}(W)	W-phase high-side gate driver input
15	L_{IN}(W)	W-phase low-side gate driver input
16	I_{TRIP}	Over-current protection input
17	P	DC bus voltage positive
18	U/V_S(U)	Motor U-phase output, U-phase high-side floating IC supply offset voltage
19	NU	U-phase low-side emitter
20	NV	U-phase low-side emitter -phase low-side emitter
21	V/V_S(V)	Motor V-phase output, V-phase high-side floating IC supply offset voltage
22	NW	W-phase low-side emitter
23	W/V_S(W)	Motor W-phase output, W-phase high-side floating IC supply offset voltage

2.2 Pin Descriptions

H_{IN}(U,V,W) and L_{IN}(U,V,W) (Low side and high side control pins)

These pins are positive logic and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about 800kΩ is internally provided to pre-bias inputs during supply start-up and an ESD diode is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time T_{FILIN}. The filter acts according to Figure 4.

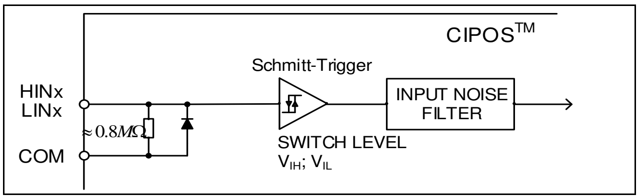


Figure 3 Input pin structure

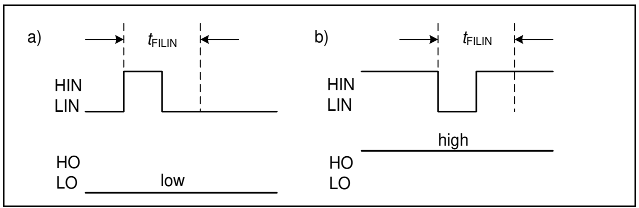


Figure 4 Input filter timing diagram

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of the high-side and low-side switch of the same inverter phase. A minimum deadtime insertion of typically 300ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

V_{DDX}, V_{SS} (Low side control supply and reference)

V_{DD} is the control supply and it provides power both to input logic and to the output power stage. Input logic is referenced to V_{SS} ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 11.1V is present.

The IC shuts down all the gate drivers power outputs, when the V_{DD} supply voltage is below V_{DDUV-} = 10.9V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_B (U,V,W) and V_S (U,V,W) (High side supplies)

V_B to V_S is the high side supply voltage. The high side circuit can float with respect to V_{SS} following the external high side power device source voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 11.1V and a falling threshold of V_{BSUV-} = 10.9V.

VS(U,V,W) provide a high robustness against negative voltage in respect of V_{SS}. This ensures very stable designs even under rough conditions.

NU, NV, NW (Low side emitters)

The low side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin V_{SS} as short as possible in order to avoid unnecessary inductive voltage drops.

VTH (Thermistor output)

A UL certified NTC resistor is integrated in the module with one terminal of the chip connected to V_{SS} and the other to VTH. When pulled up to a rail voltage such as V_{DD} or 3.3V by a resistor, the VTH pin provides an analog voltage signal corresponding to the temperature of the thermistor.

RFE (RCIN / Fault / Enable)

The RFE pin combines 3 functions in one pin: RCIN or RC-network based programmable fault clear timer, fault output and enable input.

The RFE pin is normally connected to an RC network on the PCB per the schematic in Figure 5. Under normal operating conditions, R_{RCIN} pulls the RFE pin to 3.3V, thus enabling all the functions in the IPM. The microcontroller can pull this pin low to disable the IPM functionality. This is is the Enable function.

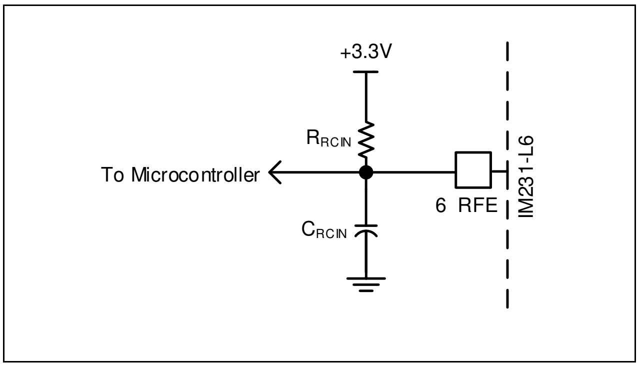


Figure 5 Typical PCB circuit connected to the RFE pin

The Fault function allows the IPM to report a Fault condition to the microncontroller by pulling the RFE pin low in one of two situations. The first is an under-voltage condition on V_{DD} and the second is when the I_{TRIP} pin sees a voltage rising above $V_{IT,TH+}$.

The programmable fault clear timer function provides a means of automatically re-enabling the module operation a preset amount of time ($T_{FLT-CLR}$) after the fault condition has disappeared. Figure 6 shows the RFE-related circuit block diagram inside the IPM.

The length of TFLT-CLR can be determined by using the formula below.

$V_{RFE}(t) = 3.3V * (1 – e^{-t/RC})$

$T_{FLT-CLR} = -R_{RCIN} * C_{RCIN} * \ln(1-V_{RFE+}/3.3V)$

For example, if R_{RCIN} is 1.2MΩ and C_{RCIN} is 1nF, the $T_{FLT-CLR}$ is about 1.7ms with V_{RFE+} of 2.2V. It is also important to note that C_{RCIN} needs to be minimized in order to make sure it is fully discharged in case of over current event.

Since the I_{TRIP} pin has a 500ns input filter, it is appropriate to ensure that C_{RCIN} will be discharged below V_{RFE-} by the open-drain MOSFET, after 350ns. Therefore, the max C_{RCIN} can be calculated as:

$V_{RFE}(t) = 3.3V * e^{-t/RC} < V_{RFE-}$

$C_{RCIN} < 350ns / (- \ln (V_{RFE-} / 3.3V) * R_{RFE\_ON})$

Consider V_{RFE-} of 0.8V and R_{RFE_ON} of 50ohm, C_{RCIN} should be less than 5nF. It is also suggested to use a R_{RCIN} of between 0.5MΩ and 2MΩ.

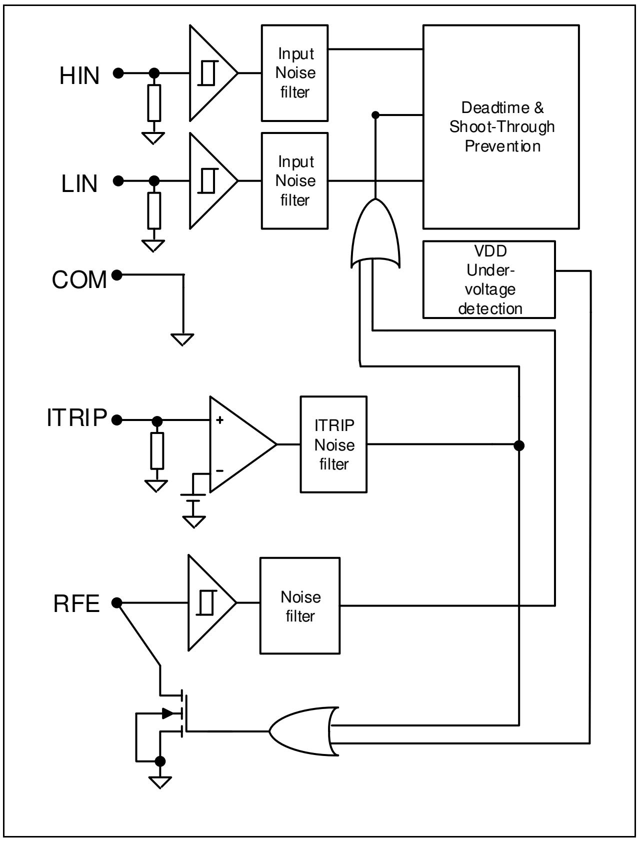


Figure 6 RFE internal circuit structure

U/V_S(U) , V/V_S(V), W/V_S(W) (High side emitter and low side collector)

These pins are connected to motor U, V, W input pins.

P (Positive bus input voltage)

The high side IGBTs are connected to the bus voltage. It is noted that the bus voltage should not exceed 450V.

3 Absolute Maximum Rating

3.1 Module

Table 3

Parameter	Symbol	Condition		Units
Storage temperature	T_{STG}		-40 ~ 150	°C
Operating case temperature	T_C		-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Isolation test voltage	V_{ISO}	1min, RMS, f = 60Hz	2000	V

3.2 Inverter

Table 4 IM241-M6

Parameter	Symbol	Condition		Units
Max. blocking voltage	V_{CES}/V_{RRM}		600	V
Output current	I_O	T_C = 25°C	4	A
Peak output current	I_{OP}	T_C = 25°C, t_p < 1ms	6	A
Peak power dissipation per IGBT	P_{tot}	T_C = 25°C	13	W
Short circuit withstand time	T_{SC}	V_{DD}=15V, V_{DC} ≤400V, T_J=150°C Allowed number of short circuits: <1000, time between short circuit: ≥ 1s	3	µs

3.3 Control

Table 5

Parameter	Symbol	Condition		Units
Low side control supply voltage	V_{DD}		-0.3 ~ 20	V
Input voltage	V_{IN}	LIN, HIN, I_{TRIP}, RFE	-0.3 ~ V_{DD}	V
High side floating supply voltage (V_B reference to V_S)	V_{BS}		-0.3 ~ 20	V

4 Thermal Characteristics

Table 6 IM241-M6

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Single IGBT thermal resistance, junction-case	$R_{TH(J-C)}$	Low side V-phase IGBT	-	9.84	11.8	K/W
Single diode thermal resistance, junction-case	$R_{TH(J-C)}$	Low side V-phase Diode	-	10.5	12.6	K/W

5 Recommended Operating Conditions

Table 7

Parameter	Symbol	Min.	Typ.	Max.	Units
Positive DC bus input voltage	P	-	-	450	V
Low side control supply voltage	V_{DD}	13.5	-	16.5	V
High side floating supply voltage	V_{BS}	12.5	-	17.5	V
Input voltage (L_{IN},H_{IN},I_{TRIP},RFE)	V_{IN}	0	-	5	V
PWM carrier frequency	F_{PWM}	-	20	-	kHz
External dead time between H_{IN} & L_{IN}	DT	1	-	-	µs
Voltage between V_{SS} and N(U,V,W)	V_{COMP}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$, $PW_{IN(OFF)}$	1	-	-	µs

6 Static Parameters

6.1 Inverter

$(V_{DD}-V_{SS}) = (V_B - V_S) = 15$ V. $T_C = 25°C$ unless otherwise specified.

Table 8 IM241-M6 (B and J type)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Collector-to-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 0.5A$	-	1.13	-	V
		$I_C = 1A$	-	1.37	1.58	V
		$I_C = 1A$, $T_J = 150°C$	-	1.36	-	V
Collector emitter leakage current of high side IGBT	I_{LKH}	$V_{IN} = 0V$, V+ = 600V	-	-	80	µA
		$V_{IN} = 0V$, V+ = 600V, $T_J = 150°C$	-	9.8	-	µA
Diode forward voltage	V_F	$I_C = 0.5A$	-	1.18	-	V
		$I_C = 1A$	-	1.38	1.60	V
		$I_C = 1A$, $T_J = 150°C$	-	1.34	-	V

6.2 Control

$(V_{DD}- V_{SS}) = (V_B - V_S) = 15$ V. $T_C = 25°C$ unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. The V_{DDUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to VS.

Table 9

Parameter	Symbol	Min.	Typ.	Max.	Units
Logic "1" input voltage (LIN, HIN)	$V_{IN,TH+}$	2.2	-	-	V
Logic "0" input voltage (LIN, HIN)	$V_{IN,TH-}$	-	-	0.8	V
V_{DD}/V_{BS} supply undervoltage, positive going threshold	$V_{DD,UV+}$, $V_{BS,UV+}$	10.6	11.1	11.6	V
V_{DD}/V_{BS} supply undervoltage, negative going threshold	$V_{DD,UV-}$, $V_{BS,UV-}$	10.4	10.9	11.4	V
V_{DD}/V_{BS} supply undervoltage lock-out hysteresis	V_{DDUVH}, V_{BSUVH}	-	0.2	-	V
RFE positive going threshold	V_{RFE+}	-	1.9	2.2	V
RFE negative going threshold	V_{RFE-}	0.8	1.1	-	V
ITRIP positive going threshold	$V_{IT,TH+}$	0.475	0.500	0.525	V
ITRIP negative going threshold	$V_{IT,TH-}$	-	0.430	-	V
ITRIP input hysteresis	$V_{IT,HYS}$	-	0.07	-	V
Quiescent V_{BS} supply current	I_{QBS}	-	-	70	µA
Quiescent V_{DD} supply current per channel	I_{QDD}	-	-	3	mA
Input bias current V_{IN}=5V for LIN, HIN	I_{IN+}	-	6.25	12.5	µA
Input bias current V_{IN}=5V for RFE	$I_{IN,RFE+}$	-	-	1	µA

Static Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units
Input bias current V_{IN}=5V for ITRIP	I_{ITRIP+}	-	5	20	µA
Bootstrap resistance	R_{BS}	-	200	-	Ω
RFE low on resistance	R_{RFE}	-	34	60	Ω

7 Dynamic Parameters

7.1 Inverter

$(V_{DD} - V_{SS}) = (V_B - V_S) = 15$ V. $T_C = 25°C$ unless otherwise specified.

Table 10 IM241-M6, B Type

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input to output turn-on propagation delay	T_{ON}	I_C = 1A, V+ = 300V	-	508	-	ns
Turn-on rise time	T_R		-	7.44	-	ns
Turn-on switching time	$T_{C(on)}$		-	52.6	-	ns
Input to output turn-off propagation delay	T_{OFF}	I_C = 1A, V+ = 300V	-	737	-	ns
Turn-off fall time	T_F		-	116	-	ns
Turn-off switching time	$T_{C(off)}$		-	101	-	ns
RFE low to six switch turn-off propagation delay	T_{EN}	V_{IN}=0 or V_{IN}=5V, V_{RFE}=5V	-	420	-	ns
ITRIP to six switch turn-off propagation delay	T_{ITRIP}	V+ = 300V,no cap on RFE	-	1.3	-	µs
Turn-on slew rate	dV / dt	I_C = 1A, V+ = 300V, V_{DD} = 15V, L = 6mH	-	6.91	-	V/ns
Turn-on switching energy	E_{ON}	I_C = 1A, V+ = 300V, V_{DD} = 15V, L = 6mH, mean of high side and low side	-	19.9	-	µJ
Turn-off switching energy	E_{OFF}		-	13.6	-	
Diode reverse recovery energy	E_{REC}		-	16.0	-	
Diode reverse recovery time	T_{RR}		-	84.2	-	ns
Turn-on switching energy	E_{ON}	I_C = 1A, V+ = 300V, V_{DD} = 15V, L = 6mH T_J = 150°C, mean of high side and low side	-	42.4	-	µJ
Turn-off switching energy	E_{OFF}		-	21.2	-	
Diode reverse recovery energy	E_{REC}		-	29.8	-	
Diode reverse recovery time	T_{RR}		-	129	-	ns

Table 11 IM241-M6, J Type

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input to output turn-on propagation delay	T_{ON}	I_C = 1A, V+ = 300V	-	588	-	ns
Turn-on rise time	T_R		-	16.4	-	ns
Turn-on switching time	$T_{C(on)}$		-	188	-	ns
Input to output turn-off propagation delay	T_{OFF}	I_C = 1A, V+ = 300V	-	1220	-	ns
Turn-off fall time	T_F		-	163	-	ns
Turn-off switching time	$T_{C(off)}$		-	157	-	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
RFE low to six switch turn-off propagation delay	T_{EN}	V_{IN}=0 or V_{IN}=5V, V_{RFE}=5V	-	490	-	ns
ITRIP to six switch turn-off propagation delay	T_{ITRIP}	V+ = 300V,no cap on RFE	-	1.3	-	µs
Turn-on slew rate	dV / dt	I_C = 1A, V+ = 300V, V_{DD} = 15V, L = 6mH, mean of high side and low side	-	1.6	-	V/ns
Turn-on switching energy	E_{ON}	I_C = 1A, V+ = 300V, V_{DD} = 15V, L = 6mH, mean of high side and low side	-	59.6	-	µJ
Turn-off switching energy	E_{OFF}		-	21.3	-	
Diode reverse recovery energy	E_{REC}		-	21.2	-	
Diode reverse recovery time	T_{RR}		-	184	-	ns
Turn-on switching energy	E_{ON}	I_C = 1A, V+ = 300V, V_{DD} = 15V, L = 6mH T_J = 150°C, mean of high side and low side	-	94.1	-	µJ
Turn-off switching energy	E_{OFF}		-	24.1	-	
Diode reverse recovery energy	E_{REC}		-	24.4	-	
Diode reverse recovery time	T_{RR}		-	261	-	ns

7.2 Control

(V_{DD}- V_{SS}) = (V_B - V_S) = 15V. T_C = 25°C unless otherwise specified.

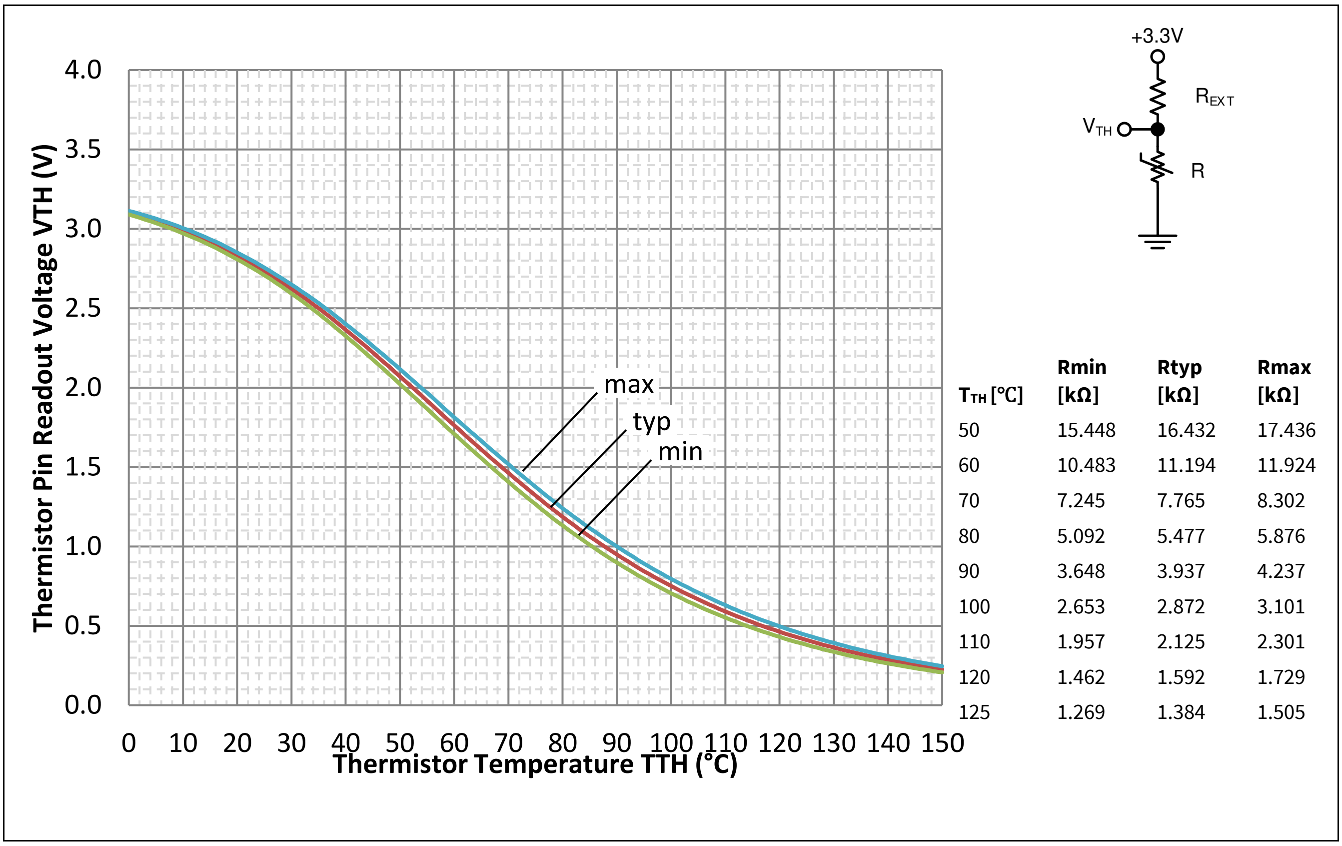
Table 12

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input filter time (HIN, LIN)	$T_{FIL,IN}$	V_{IN} = 0 or V_{IN} = 5V	-	300	-	ns
Input filter time (ITRIP)	$T_{FIL,ITRIP}$	V_{IN}=0 or V_{IN}=5V	-	500	-	ns
Internal dead time	DT_{IC}	V_{IN} = 0 or V_{IN} = 5V	-	300	-	ns
Matching propagation delay time (on and off) for same phase high-side and low-side	M_T	External dead time > 500ns	-	-	50	ns

8 Thermistor Characteristics

Table 13

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Resistance	R_{25}	T_C = 25°C, ±5% tolerance	44.65	47	49.35	kΩ
Resistance	R_{125}	T_C = 125°C	1.27	1.39	1.51	kΩ
B-constant (25/100)	B	±1% tolerance	-	4006	-	K
Temperature Range			-20	-	150	°C



T_{TH} [°C]	Rmin [kΩ]	Rtyp [kΩ]	Rmax [kΩ]
50	15.448	16.432	17.436
60	10.483	11.194	11.924
70	7.245	7.765	8.302
80	5.092	5.477	5.876
90	3.648	3.937	4.237
100	2.653	2.872	3.101
110	1.957	2.125	2.301
120	1.462	1.592	1.729
125	1.269	1.384	1.505

Figure 7 **Thermistor resistance – temperature curve, for R_{EXT}=9.76kΩ, and thermistor resistance variation with temperature.**

9 Mechanical Characteristics and Ratings

Table 14

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Comparative Tracking Index	CTI		550	-	-	V
Curvature of module backside	BC	See Figure 9	-50	-	50	µm
Mounting Torque	T	M3 screw & washer, thermal grease	0.4	0.8	1.2	Nm
		M3 screw & washer, SIL-PAD 1500ST	-	0.6	1.0	Nm
Weight	W		-	3	-	g

10 Qualification Information

Table 15

UL Certification	UL-US-L252584-15-22508102-2	
Moisture sensitivity level (SOP 29 x 12 only)	MSL3	
RoHS Compliant	Yes	
ESD	Human body model	1C
	Charge discharge model	C3

11 Diagrams & Tables

11.1 T_C Measurement Point

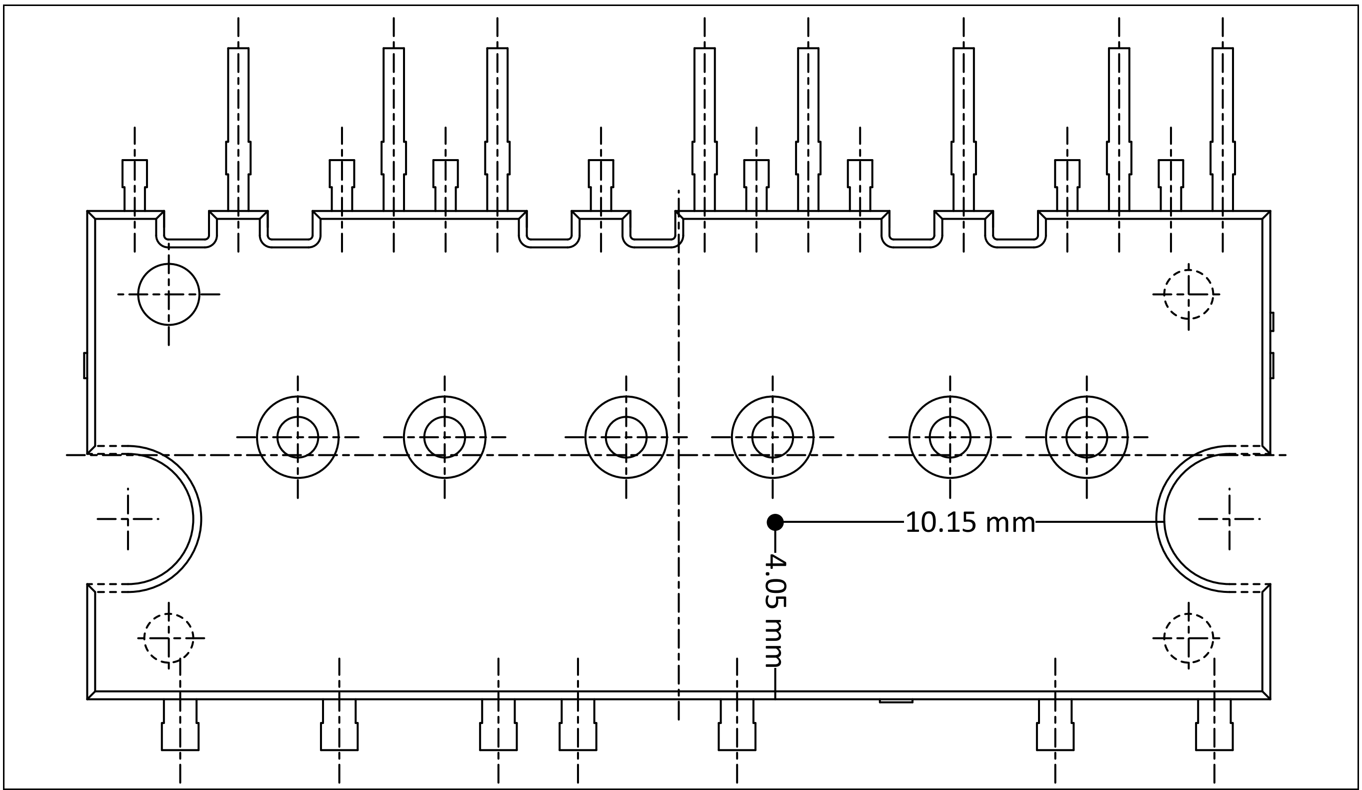


Figure 8 T_C **measurement point**

11.2 Backside Curvature Measurement Points

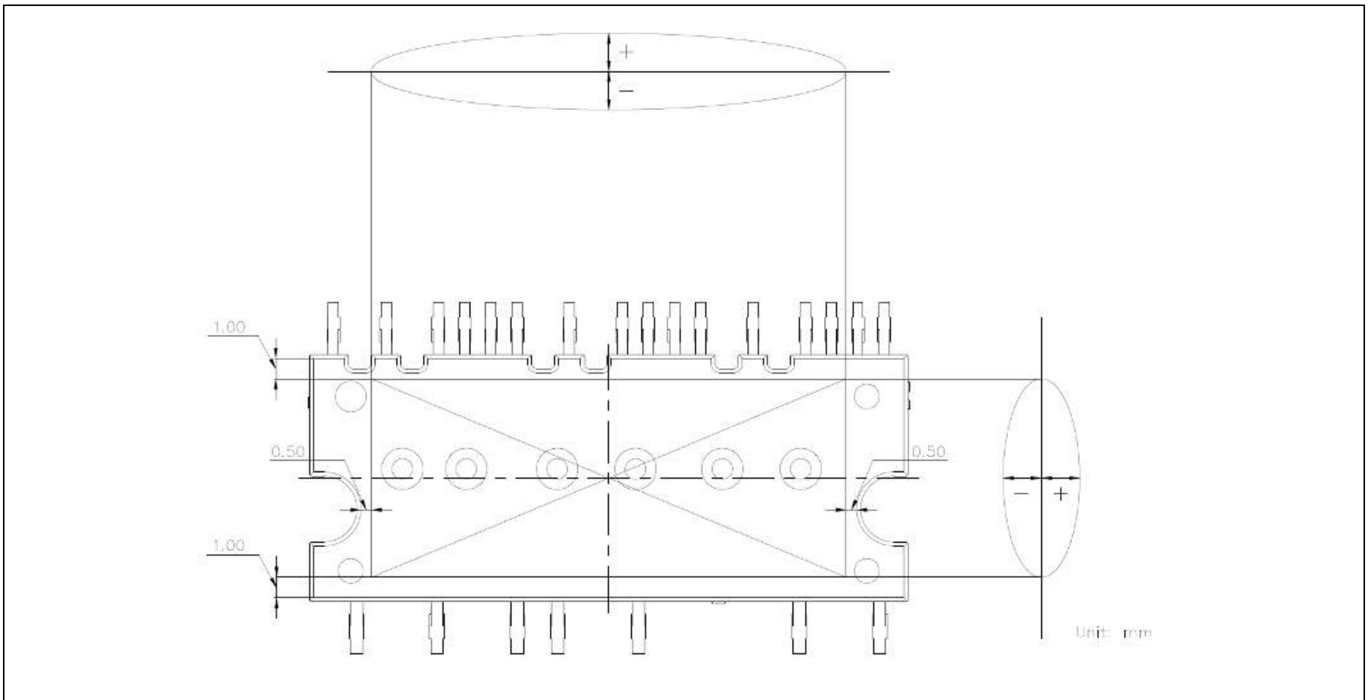


Figure 9 **Curvature measurement points**

11.3 Input-Output Logic Table

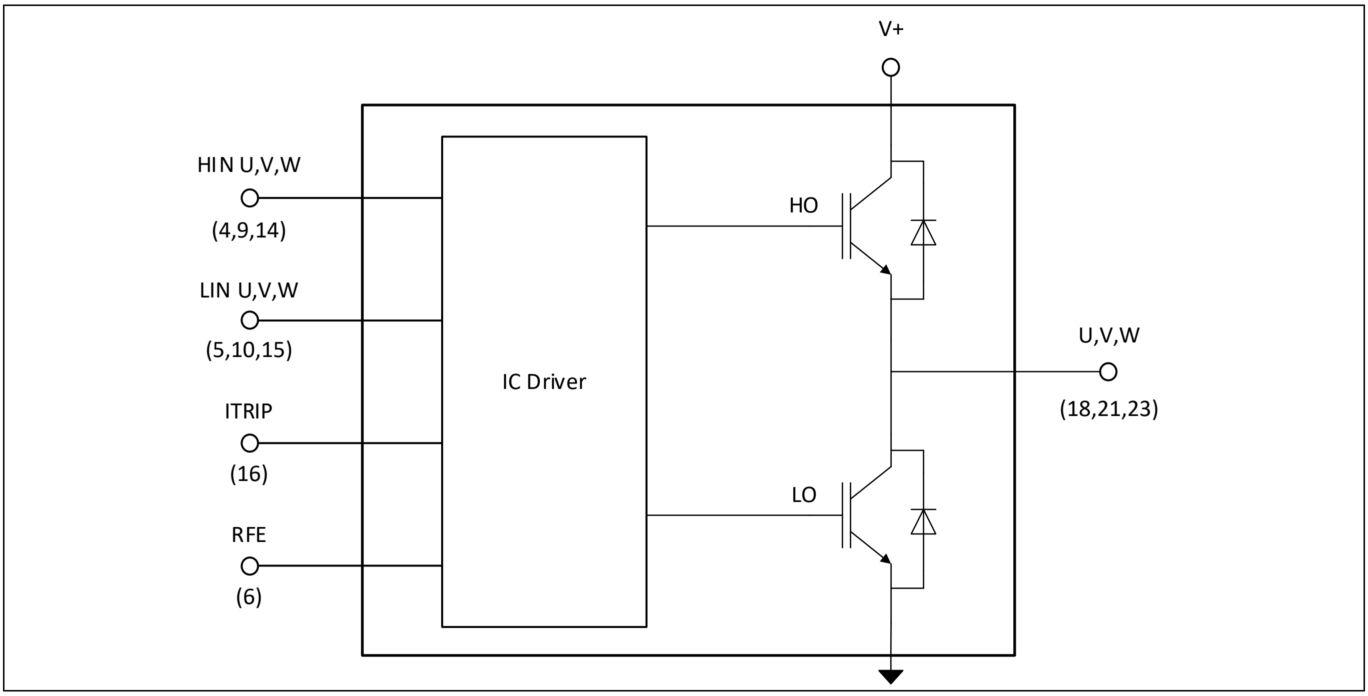


Figure 10 Module block diagram

Table 16

RFE	ITRIP	HIN U,V,W	LIN U,V,W	U,V,W
1	0	1	0	V+
1	0	0	1	0
1	0	0	0	‡
1	0	1	1	‡
1	1	x	x	‡
0	x	x	x	‡

‡ Voltage depends on direction of phase current

11.4 Switching Time Definitions

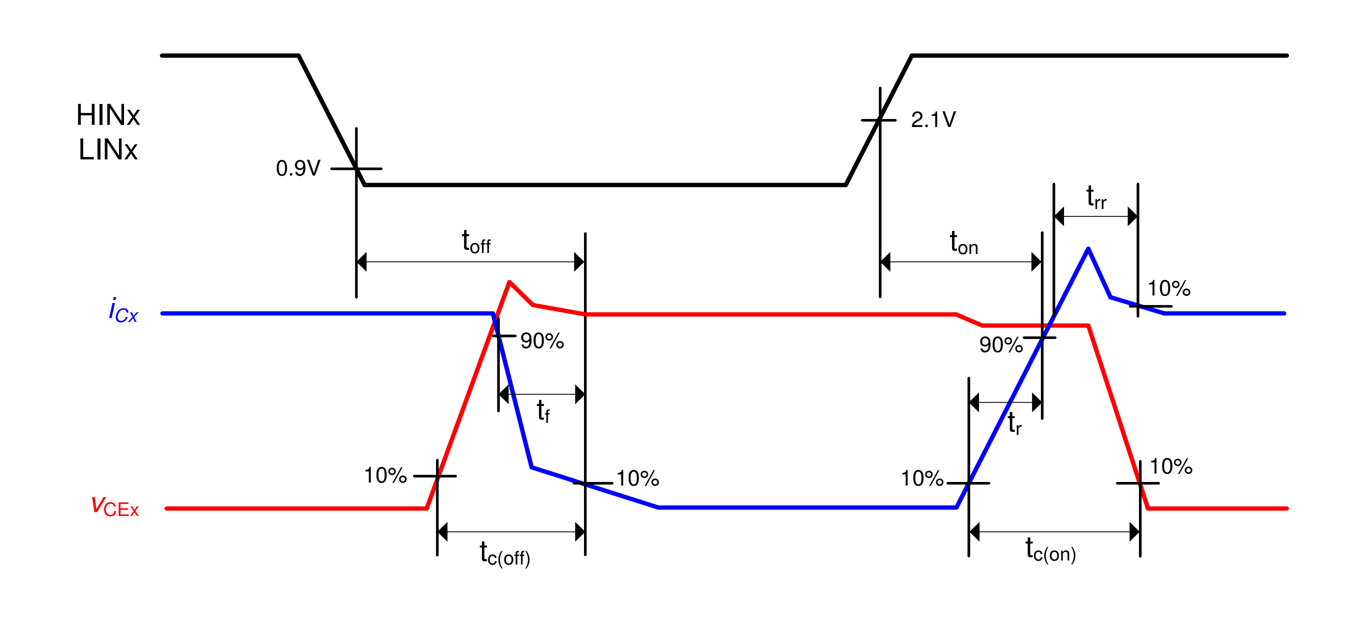


Figure 11 Switching times definition

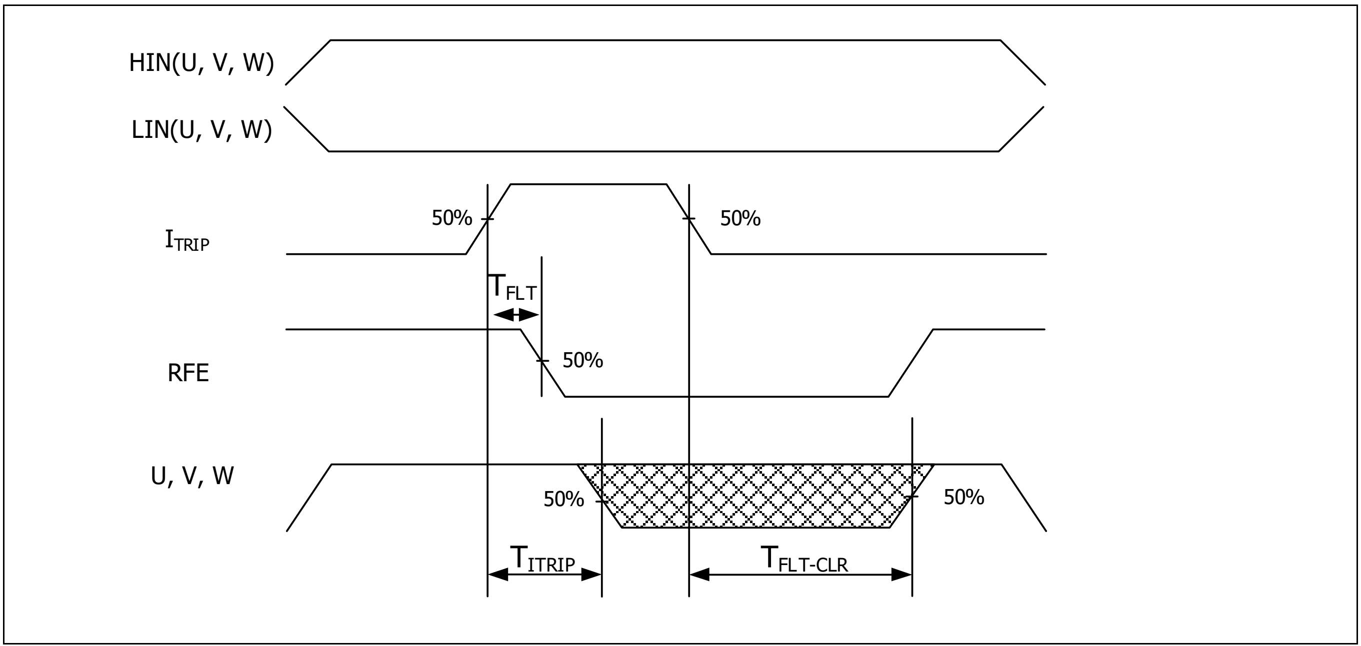


Figure 12 ITRIP time waveform

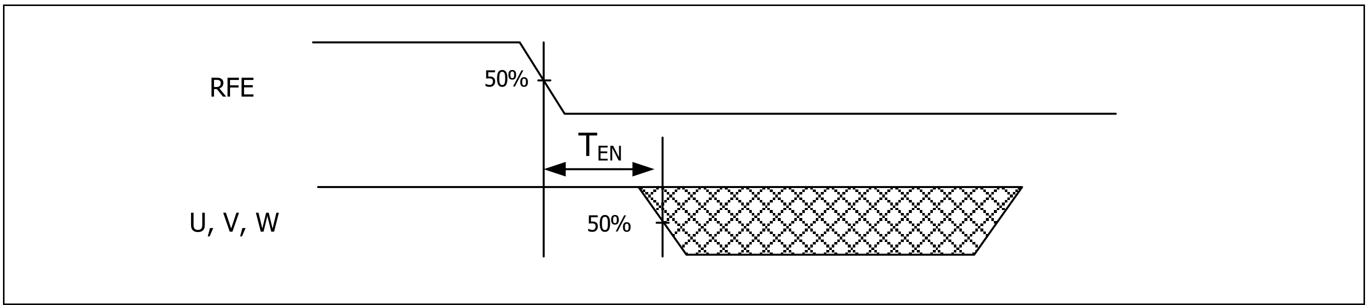


Figure 13 Output disable timing diagram

12 Application Guide

12.1 Typical Application Schematic

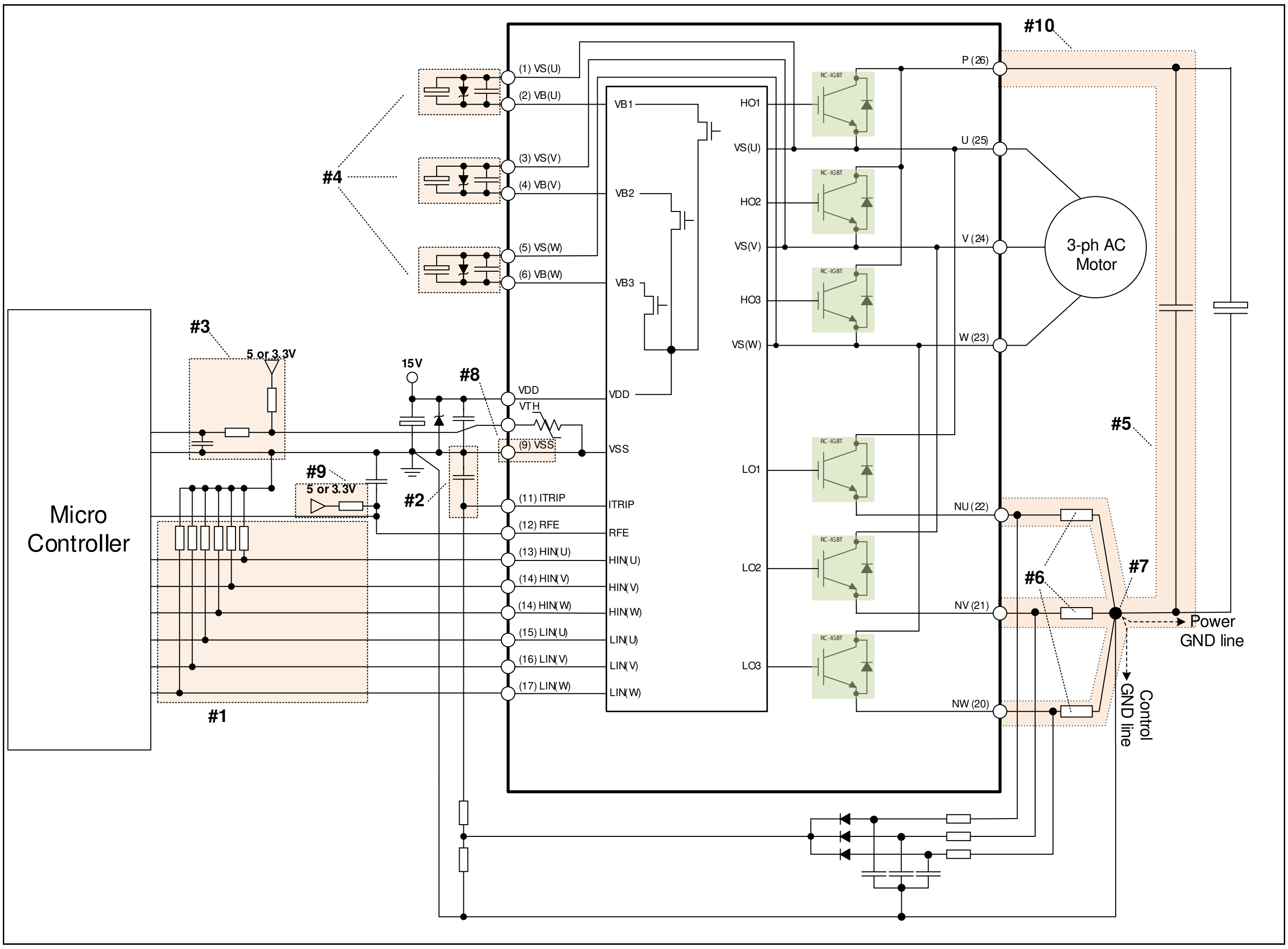


Figure 14 Application schematic

12.2 T_J vs T_{TH}

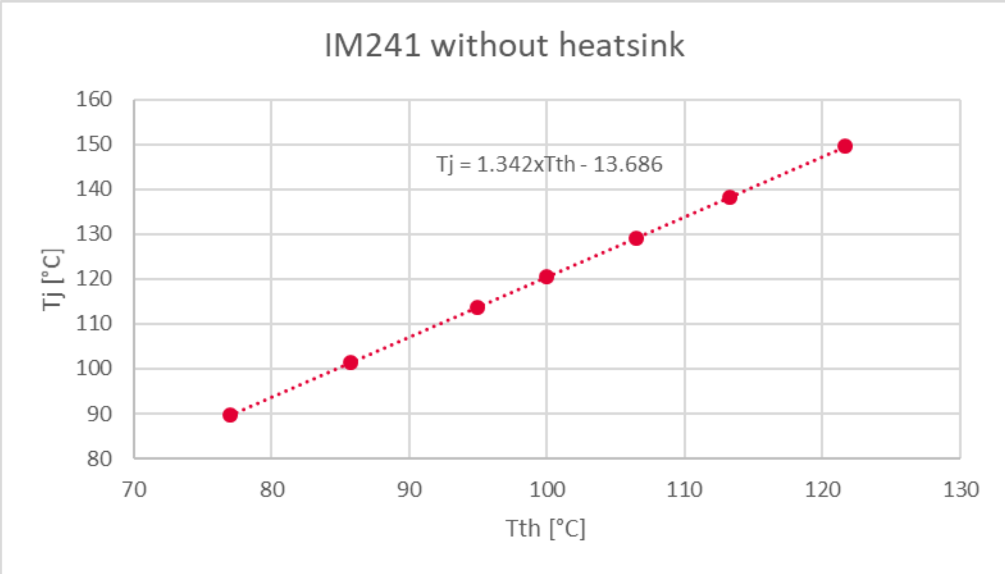


Figure 15 **Typical T_J vs T_{TH} correlation without heatsink (AN-2021-08 for reference)**

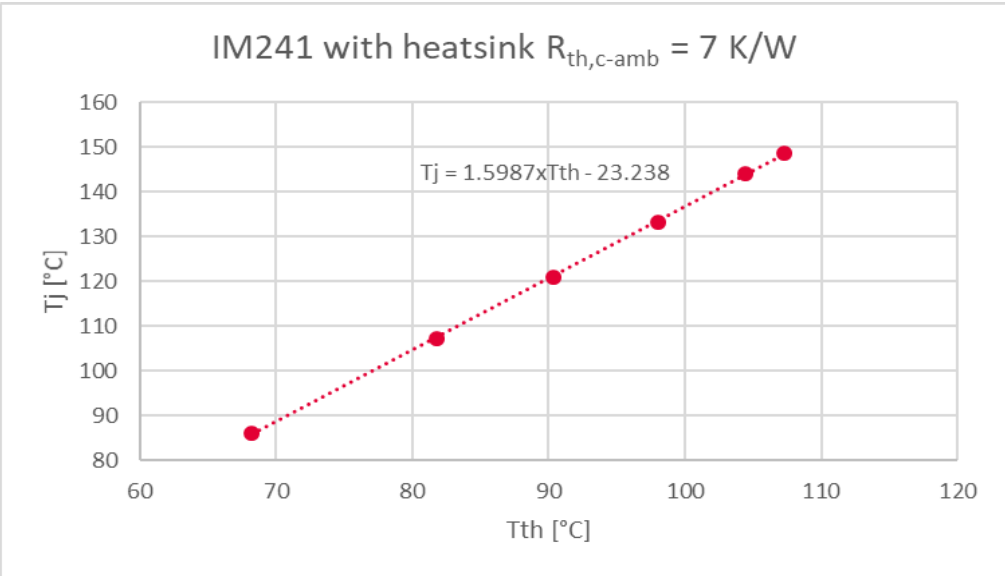


Figure 16 **Typical T_J vs T_{TH} correlation with heatsink and $Rth_{c\text{-}amb}$ = 7 K/W (AN-2021-08 for reference)**

12.3 –V_S Immunity

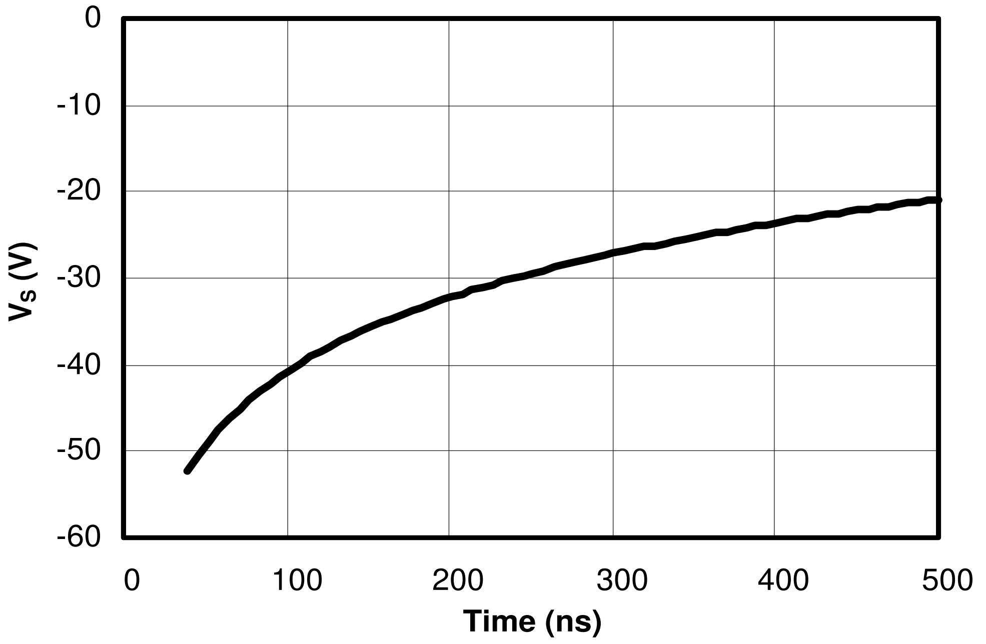
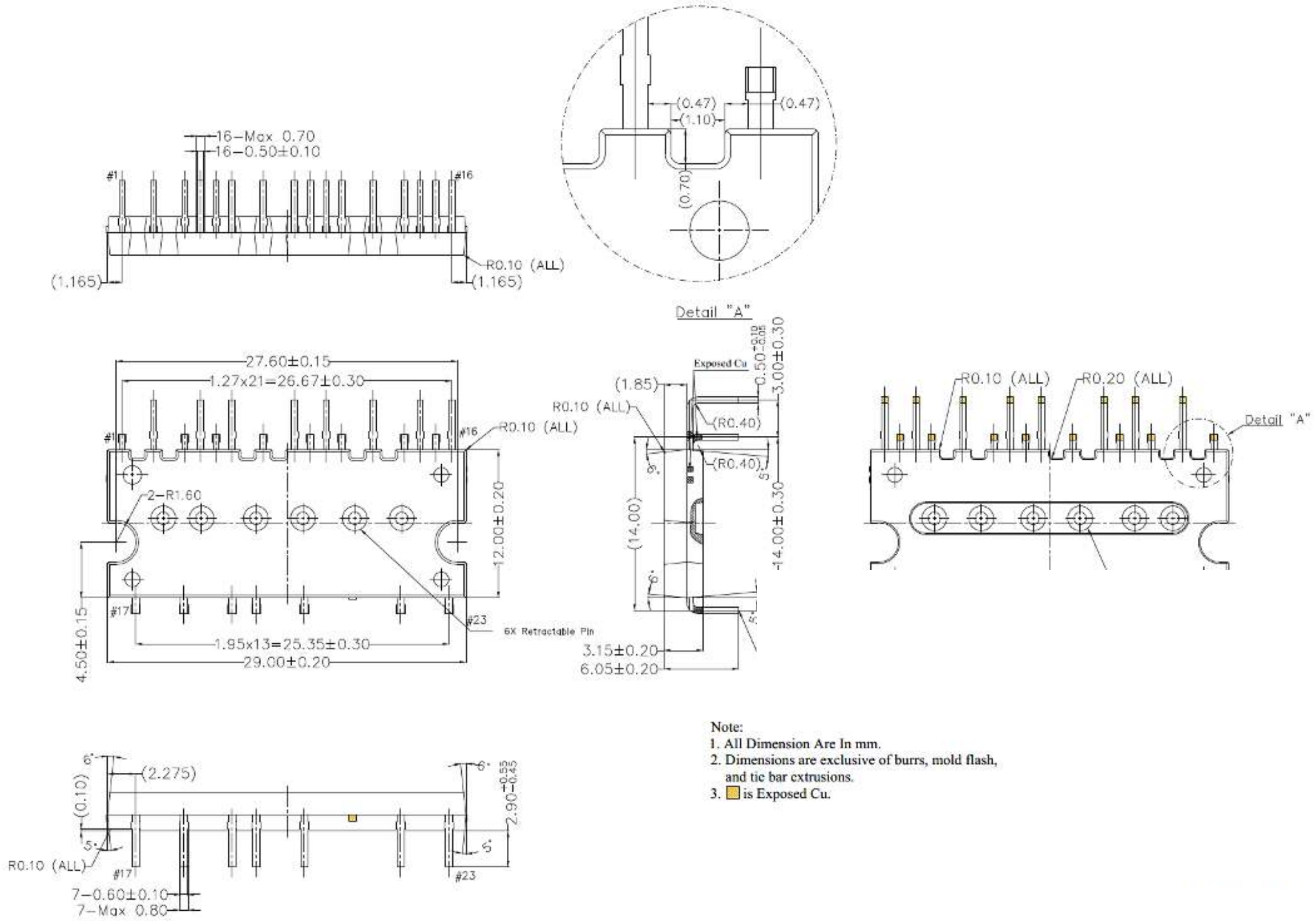


Figure 17 Negative transient V_s SOA for integrated gate driver

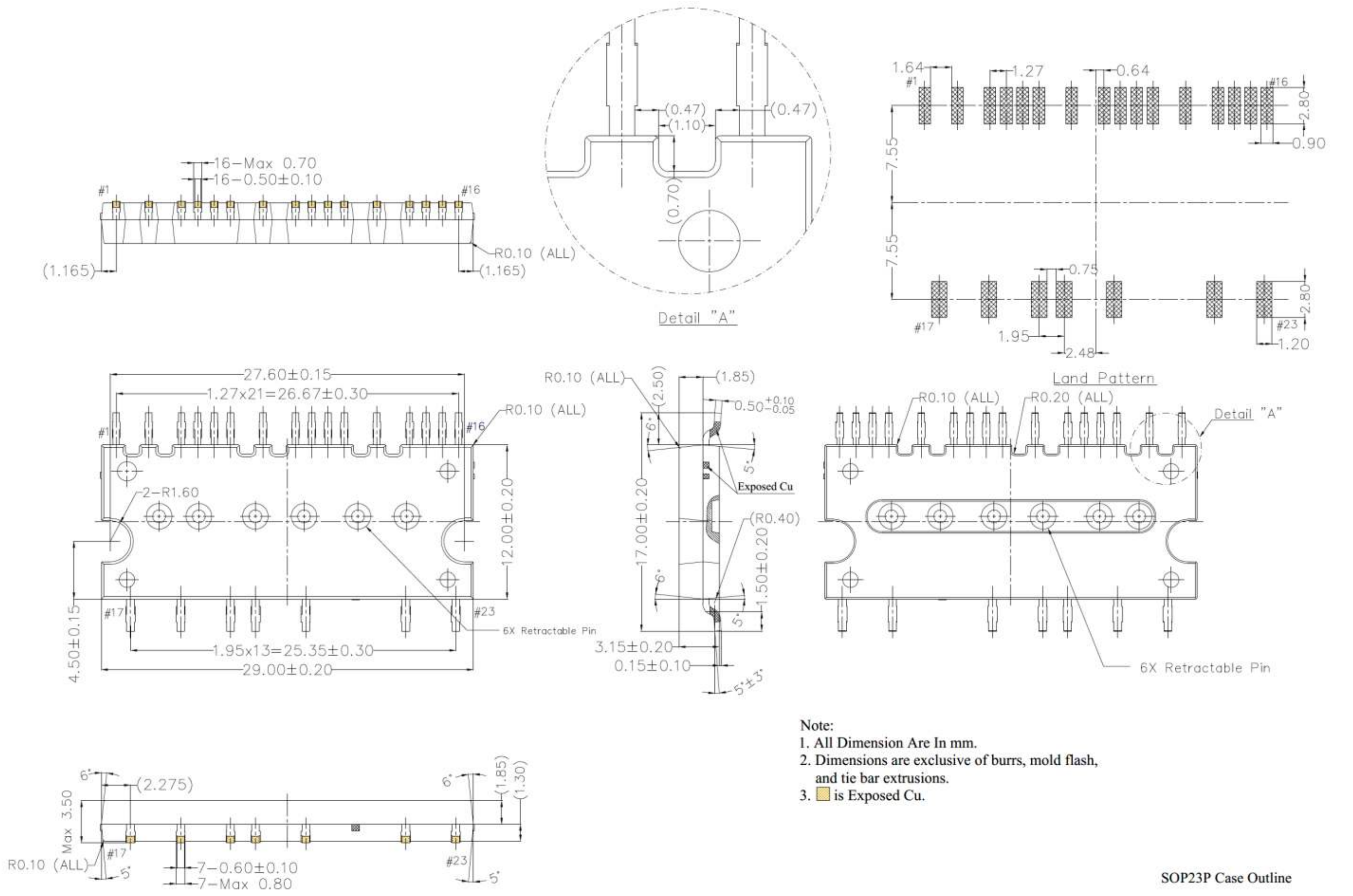
13 Package Outline

13.1 DIP 29x12



Dimensions in mm

13.2 SOP 29x12



Dimensions in mm

14 Revision History

Major changes since the last revision

Page or Reference	Description of change

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-06-26

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference