Data Sheet

MxL7204

Dual 4A Power Module

General Description

The MxL7204 power module is a complete dual 4A or single 8A output switch mode DC/DC power supply with an input voltage of 4.5V to 20V. It offers higher efficiency and improved thermal performance than the competition while matching pinout and functionality. Power modules integrate the switching controller, power FETs, inductors and all supporting components. The MxL7204 supports two outputs each with an output voltage range of 0.6V to 5.0V, set by a single external resistor. Its high efficiency design delivers up to 4A continuous current (5A peak) for each output. Only a few input and output capacitors are needed.

The device supports frequency synchronization, multiphase operation, and output voltage tracking for supply rail sequencing. High Switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability.

Fault protection features include overvoltage, overcurrent and over temperature protection. The power module is offered in a space saving and thermally enhanced 15mm × 15mm × 2.82mm LGA package.

Features

- Dual 4A output (5A peak)
- Input Voltage Range: 4.5V to 20V
- Output Voltage Range: 0.6V to 5.0V
- Current mode control / fast transient response
- Adjustable switching frequency
- Frequency synchronization (250kHz to 780kHz)
- Overcurrent protection
- Output overvoltage protection
- Thermally enhanced (15mm x 15mm x 2.82mm) LGA package

Applications

- Telecom and Networking Equipment
- Industrial Equipment

Ordering Information - Back Page

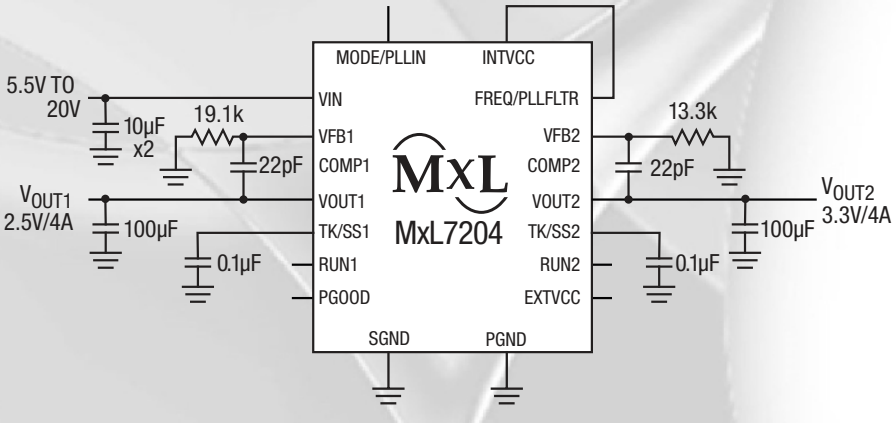

Figure 1: Typical Application Circuit

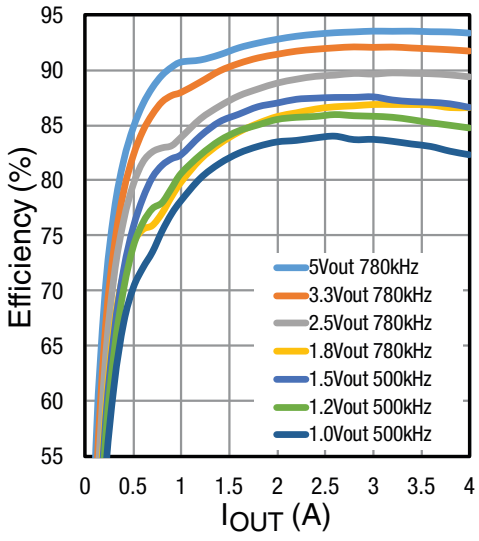

Figure 2: Efficiency $12V_{IN}$

Revision History

Revision	Release Date	Change Description
1A	2/20/18	Initial Release
1B	8/8/18	Added paralleled output voltage programming equations and Table 7. Renamed R_{FB} resistors to R_{SET}. Corrected TK/SS and VFB pin numbers in Pin Description. Harmonized name of TR/SS, FREQ/PLL-FLTR, MODE/PLLIN and PGND pins. Corrected Figure 30.

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Specifications

Absolute Maximum Ratings

Important! The stresses above what is listed under Table 1 may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under Table 1 or anyother conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above what is listed under Table 3 for extended periods of time may affect device reliability. Solder reflow profile is specified in the IPC/JEDEC J-STD-020C standard.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
V_{IN}	–0.3	22	V
V_{SW1}, V_{SW2}	–1	22	V
PGOOD, COMP1, COMP2	–0.3	6	V
$INTV_{CC}$, $EXTV_{CC}$	–0.3	6	V
MODE/PLLIN, FREQ/PLLFLTR, TK/SS1, TK/SS2	–0.3	$INTV_{CC}$	V
V_{OUT1}, V_{OUT2}	–0.3	6	V
RUN1, RUN2, VFB1, VFB2	–0.3	$INTV_{CC}$	V
$INTV_{CC}$ Peak Output Current		100mA	V
Internal Operating Temperature Range	-40	125	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (soldering 10 seconds)		245	°C

ESD Ratings

Table 2: ESD Ratings

Parameter	Minimum	Maximum	Units
HBM (Human Body Model)		3k	V
CDM (Charged Device Model)		500	V

Operating Conditions

***Table 3:* Operating Conditions**

Parameter	Minimum	Maximum	Units
V_{IN}	4.5	20	V
$INTV_{CC}$	4.5	5.5	V
PGOOD	0	5.0	V
Junction Temperature Range (T_J)	-40	125	°C
Package Power Dissipation max at 25°C		4.33	W
Package Thermal Resistance Θ_{JA}(1)		14.4	°C/W
Package Thermal Resistance Θ_{JB}(1)		7	°C/W

NOTE:
1. $\Theta_{JB} = \Theta_{JC\ BOTTOM}$ = 7°C/W, Θ_{BA} = 7.4°C/W, $\Theta_{JA} = \Theta_{JB} + \Theta_{BA}$

Electrical Characteristics

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN}=12V. Per Figure 31.

***Table 4:* Electrical Characteristics**

Symbol	Parameter	Conditions		•	Min	Typ	Max	Units
DC Specifications								
$V_{IN(DC)}$	Input DC voltage	V_{IN} ≤ 5.5V, Connect V_{IN} and $INTV_{CC}$ Together		•	4.5		20.0	V
$V_{OUT1, 2(RANGE)}$	Output voltage range	V_{IN} = 5.5V to 20.0V		•	0.6		5.0	V
$V_{OUT1, 2(DC)}$	Output voltage	C_{IN} = 10µF x 1, C_{OUT} = 22µF Ceramic, 220µF POSCAP, FREQ/PLLFLTR tied to INTVCC, V_{IN} = 12V, V_{OUT} = 2.5V	I_{OUT} = 0A	•	2.463	2.5	2.537	V
			I_{OUT} = 4A	•	2.450	2.5	2.550	
Input Specifications								
V_{RUN1}, V_{RUN2}	RUN pin on/off threshold	RUN rising			1.1	1.25	1.40	V
$V_{RUN1HYS}$, $V_{RUN2HYS}$	RUN pin on hysteresis					200		mV
$I_{INRUSH(VIN)}$	Input inrush current at start-up	I_{OUT} = 0A, C_{IN} = 10µF, C_{OUT} = 100µF, V_{OUT} = 2.5V, V_{IN} = 12V				0.25		A
$I_{Q(VIN)}$	Input supply bias current	V_{IN} = 12V, V_{OUT1} = 2.5V, switching continuous				30		mA
		V_{IN} = 12V, V_{OUT2} = 2.5V, switching continuous				30		
		V_{IN} = 20V, V_{OUT1} = 2.5V, switching continuous				35		
		V_{IN} = 20V, V_{OUT2} = 2.5V, switching continuous				35		
		Shutdown, RUN = 0, V_{IN} = 20V				50		µA
$I_{S(VIN)}$	Input supply current	V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 4A				0.93		A
		V_{IN} = 20V, V_{OUT} = 2.5V, I_{OUT} = 4A				0.59		

Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN}=12V. Per Figure 31.

Table 4: Electrical Characteristics (continued)

Symbol	Parameter	Conditions		•	Min	Typ	Max	Units
Output Specifications								
$I_{OUT1, 2(DC)}$	Output continuous current range	V_{IN} = 12V, V_{OUT} = 2.5V(1)			0		4	A
$\frac{\Delta V_{OUT1(LINE)}}{V_{OUT(NOM)}}$	Line regulation accuracy	V_{OUT} = 2.5V, V_{IN} from 6V to 20V I_{OUT} = 0A for each output				0.15	0.3	%
				•		0.25	0.5	
$\frac{\Delta V_{OUT2(LINE)}}{V_{OUT(NOM)}}$	Line regulation accuracy	V_{OUT} = 2.5V, V_{IN} from 6V to 20V I_{OUT} = 0A for each output				0.15	0.3	%
				•		0.25	0.5	
$\frac{\Delta V_{OUT1(LOAD)}}{V_{OUT(NOM)}}$	Load regulation accuracy	For each output, V_{OUT} = 2.5V, 0A to 4A, V_{IN} = 12V(2)		•		0.6	0.8	±%
$\frac{\Delta V_{OUT2(LOAD)}}{V_{OUT(NOM)}}$	Load regulation accuracy	For each output, V_{OUT} = 2.5V, 0A to 4A, V_{IN} = 12V(2)		•		0.6	0.8	±%
$V_{OUT1, 2(AC)}$	Output ripple voltage	I_{OUT} = 0A, C_{OUT} = 200µF X5R Ceramic, V_{OUT} = 2.5V	V_{IN} = 12V			15		mV
			V_{IN} = 20V			20		
f_S	Output ripple voltage frequency	I_{OUT} = 2A, V_{IN} = 12V, V_{OUT} = 2.5V FREQ/PLLFLTR = $INTV_{CC}$				780		kHz
$V_{OUTSTART}$	Turn-on overshoot	C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, I_{OUT} = 0A	V_{IN} = 12V			5		mV
			V_{IN} = 20V			3		
t_{START}	Turn-on time	C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, I_{OUT} = 0A, Resistive Load	V_{IN} = 12V			0.25		ms
			V_{IN} = 20V			0.13		
V_{OUTLS}	Peak deviation for dynamic load	Load: 0% to 50% to 0% of full load C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, V_{IN} = 12V				15		mV
t_{SETTLE}	Settling time for dynamic load step	Load: 0% to 50% to 0% of full load C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, V_{IN} = 12V				10		µs
I_{OUTPK}	Output current limit	C_{OUT} = 22µF Ceramic, 220µF POSCAP, V_{IN} = 12V, V_{OUT} = 2.5V				9		A

Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN}=12V. Per Figure 31.

Table 4: Electrical Characteristics (continued)

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Control Section							
V_{FB1}, V_{FB2}	Voltage at V_{FB} pins	I_{OUT} = 0A, V_{OUT} = 1.5V	•	0.594	0.600	0.606	V
I_{FB}	Current at V_{FB} pins				-5	-20	nA
V_{OVL}	Feedback overvoltage lockout		•	0.654	0.66	0.666	V
TRACK1 (I), TRACK2 (I),	Track pin soft-start pull-up current	TRACK1 (I),TRACK2 (I) start at 0V		1.00	1.25	1.50	µA
UVLO	Undervoltage lockout	V_{IN} Falling			3.65		V
		V_{IN} Rising			4.25		V
UVLO Hysteresis					600		mV
$t_{ON(MIN)}$	Minimum on-time				90		ns
R_{FBHI1}, R_{FBHI2}	Resistor between V_{OUTS1}, V_{OUTS2} and V_{FB1}, V_{FB2}	Each output		60.3	60.4	60.5	kΩ
$V_{PGOOD\ Low}$	PGOOD voltage low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD leakage current	V_{PGOOD} = 5V				±5	µA
V_{PGOOD}	PGOOD trip level	V_{FB} with respect to set output voltage V_{FB} ramping negative			-10		%
		V_{FB} with respect to set output voltage V_{FB} ramping positive			10		%
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} voltage	6V < V_{IN} < 20V		4.8	5	5.2	V
V_{INTVCC} Load Regulation	$INTV_{CC}$ load regulation	I_{CC} = 0mA to 50mA			1	2	%
V_{EXTVCC}	$EXTV_{CC}$ switchover voltage	$EXTV_{CC}$ ramping positive	•	4.5	4.7		V
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ hysteresis				180		mV

Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN}=12V. Per Figure 31.

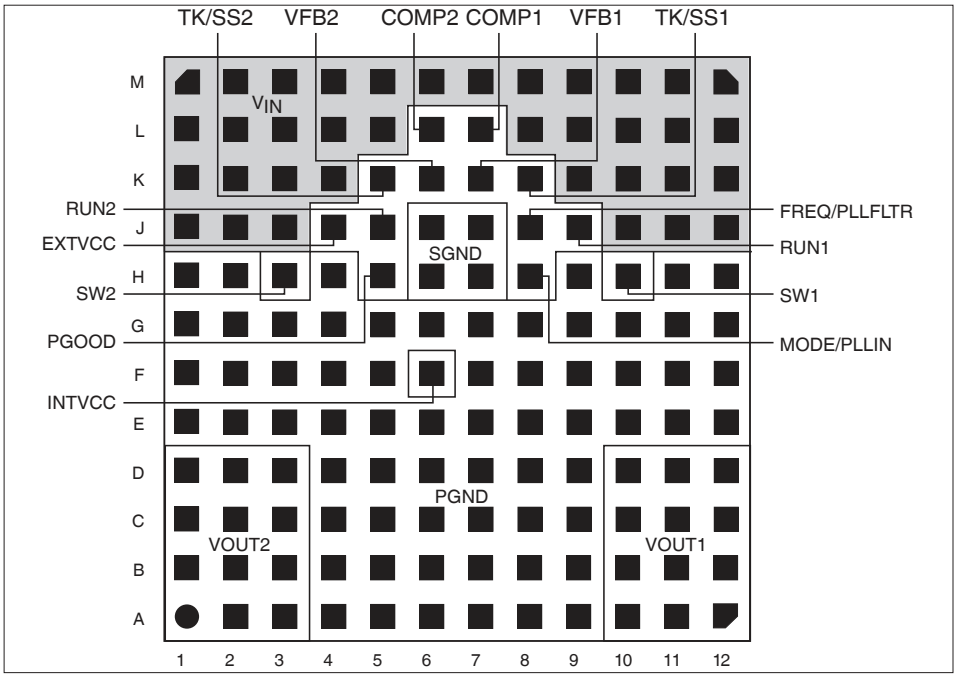
Table 4: Electrical Characteristics (continued)

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Oscillator and Phase-Locked Loop							
Frequency Nominal	Nominal frequency	FREQ/PLLFLTR tied to 1.2V		450	500	550	kHz
Frequency Low	Lowest frequency	FREQ/PLLFLTR tied to 0V		210	250	290	kHz
Frequency High	Highest frequency	FREQ/PLLFLTR > 1.8V, up to $INTV_{CC}$		700	780	790	kHz
FREQ/ PLLFLTR	Frequency set current			9	10	11	µA
RMODE_PLLIN	MODE/PLLIN input resistance				235		kΩ

NOTE:
1. For different V_{IN}, V_{OUT} and T_A, refer to the output current derating curves.

Pin Information

Pin Configuration



Top View, 15mm x 15mm x 2.82mm LGA

Figure 3: Pin Configuration

Pin Description

Table 5: Pin Description

Pin Number	Pin Name	Description
A10 - D10, A11 - D11, A12 - D12	VOUT1	Output of the channel 1 power stage. Connect the corresponding output load from the VOUT1 pins to the PGND pins. Direct output decoupling capacitance from the V_{OUT1} to PGND is recommended.
A4 - A9, B4 - B9, C4 - C9, D4 - D9, E1 - E12, F1 - F5, F7 - F12, G1 - G12, H1, H2, H4, H9, H11, H12	PGND	Ground for the power stage. Connect to the application's power ground plane.
A1 - D1, A2 - D2, A3 - D3	VOUT2	Output of the channel 2 power stage. Connect the corresponding output load from the VOUT2 pins to the PGND pins. Direct output decoupling capacitance from the V_{OUT2} to PGND is recommended.

Table 5: Pin Description (Continued)

Pin Number	Pin Name	Description
J8	FREQ/ PLLFLTR	Frequency Set pin. A 10µA current is sourced from this pin. A resistor from this pin to ground sets a voltage that in turn programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. The nominal frequency is 500kHz although it can be modified as long as the inductor ripple current is kept smaller than 40% to 50% of the output current. $I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f_{SW} \times V_{IN}}$ f_{SW} is the selected operating frequency and L is the value of the inductor.
J6, J7, H6, H7	SGND	Ground pin for all analog signals and low power circuits. Connect to PGND in one place. See layout guidelines in Figure 30.
K6, K7	VFB2, VFB1	Feedback input to the negative side of error amplifier for each channel. These pins are internally connected to their respective Vout, each via a precision 60.4kΩ resistor. The setting of each output voltage can be varied by selecting and adding a feedback resistor from its respective VFB pin to SGND.
K5	TK/SS2	Output Voltage Tracking pin and Soft-Start pins. Each channel has a 1.25µA pull-up current source. When one channel is configured to be master of the two channels, then a capacitor from this pin to ground will set a soft-start ramp rate. The remaining channel can be set up as the slave, and have the master's output applied through a voltage divider to the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking.
K8	TK/SS1	
L7	COMP1	Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. The device is internally compensated.
L6	COMP2	
H8	MODE/ PLLIN	Force Continuous Mode or Pulse-Skipping Mode Selection pin and External Synchronization Input to Phase Detector pin. Connect this pin to SGND to force both channels into forced continuous mode of operation. Connect to $INTV_{CC}$ or float to enable pulse-skipping mode of operation. A clock on the pin will force both channels into continuous mode of operation synchronized to the external clock applied to this pin.
J9	RUN1	Run Control pins. A voltage above 1.25V will turn on each channel in the module. A voltage below 1.25V on the RUN pin will turn off the related channel. Each RUN pin has a 1µA pull-up current, once the RUN pin reaches 1.25V an additional 4.5µA pull-up current is added to this pin.
J5	RUN2	
H10	SW1	Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce switch noise or leave floating with a via to the bottom of the board for probing.
H3	SW2	
H5	PGOOD	Power-good output. This open-drain output is pulled low when Vout is more than ±10% outside of its regulation point.
F6	INTVCC	Internal 5V Regulator Output. The control circuits and internal gate driver are powered from this voltage. This pin should be decoupled to SGND with a 4.7µF low ESR tantalum or ceramic capacitor. INTVCC is activated when either RUN1 or RUN2 is activated.

Table 5: Pin Description (Continued)

Pin Number	Pin Name	Description
J4	EXTVCC	External power input that is enabled through a switch to INTVCC whenever EXTVCC is greater than 4.7V. Do not exceed 6V on this input, and connect this pin to V_{IN} when operating V_{IN} on 5V. An efficiency increase will occur that is a function of the (V_{IN} – $INTV_{CC}$) multiplied by power MOSFET driver current when the feature is used. V_{IN} must be applied before $EXTV_{CC}$, and $EXTV_{CC}$ must be removed before V_{IN}. A 5V output can be tied to this pin to increase efficiency.
J1 - J3, J10 - J12, K1 - K4, K9 - K12, L1 - L5, L8 - L12, M1 - M12	VIN	IC supply input. Connect input voltage from these pins to PGND. Direct input decoupling capacitance from Vin to PGND is recommended. For V_{IN} < 5.5V, VIN should be connect to INTVCC.

NOTE:
1. Use test points to monitor signal pin connections.

Typical Performance Characteristics

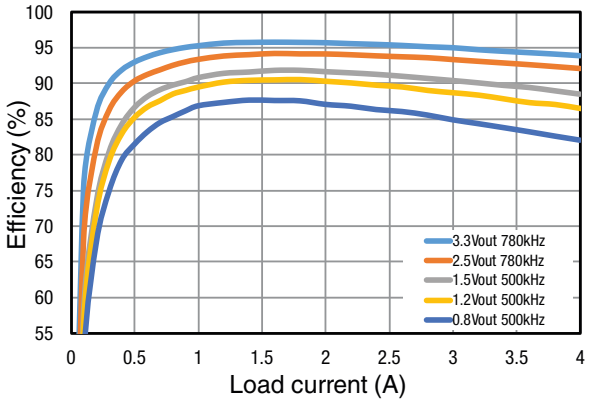


Figure 4: Efficiency, V_{IN} = 5V

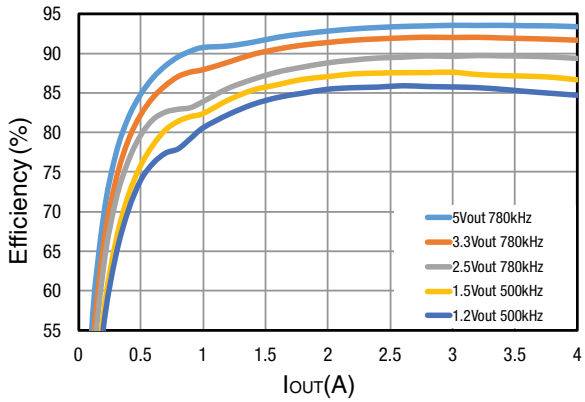


Figure 5: Efficiency, V_{IN} = 12V

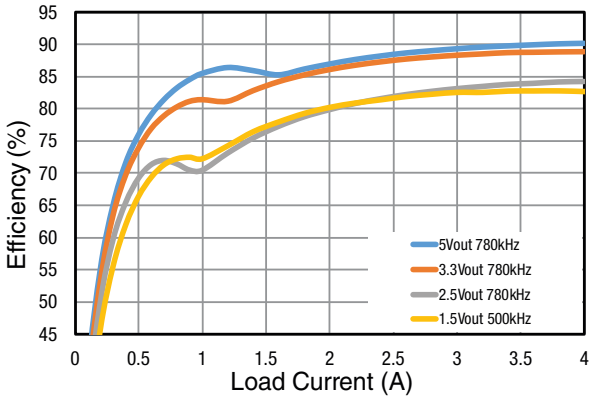


Figure 6: Efficiency, V_{IN} = 20V

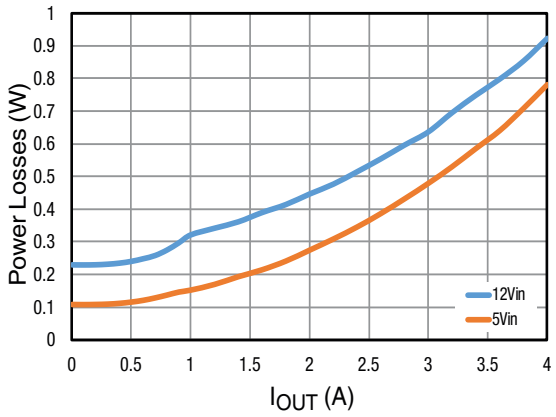


Figure 7: Power Loss, V_{OUT} = 1.5V

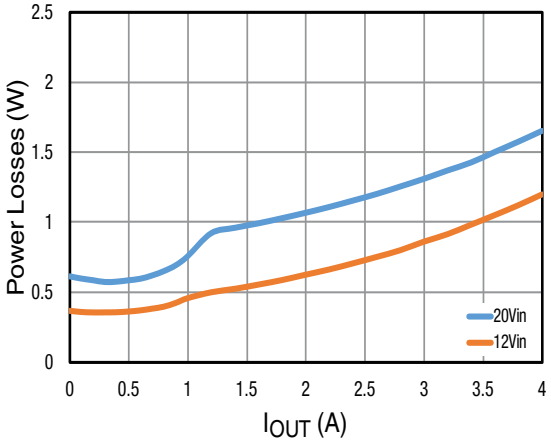


Figure 8: Power Loss, V_{OUT} = 3.3V

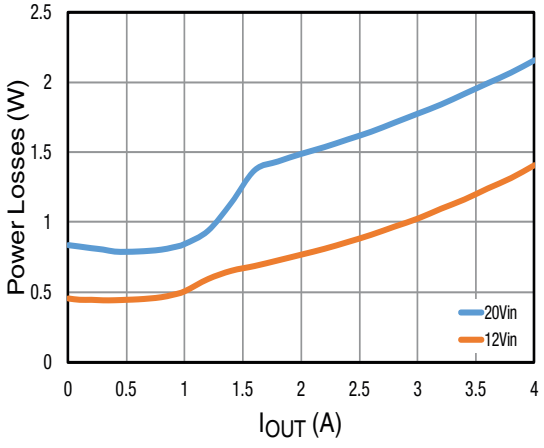


Figure 9: Power Loss, V_{OUT} = 5V

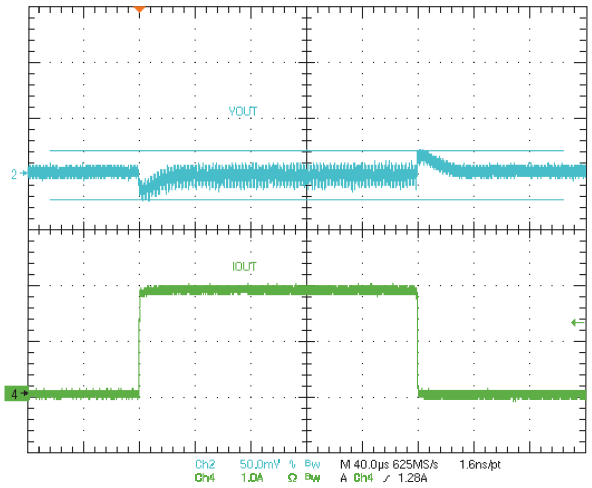


Figure 10: Load Step, CCM, V_{OUT} = 1.2V

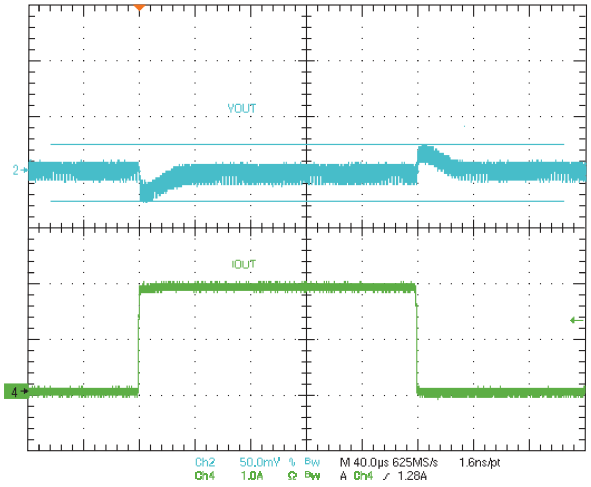


Figure 11: Load Step, CCM, V_{OUT} = 1.5V

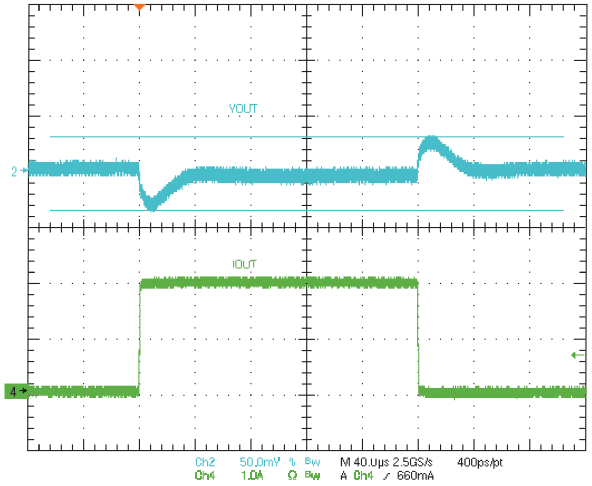


Figure 12: Load Step, CCM, V_{OUT} = 2.5V

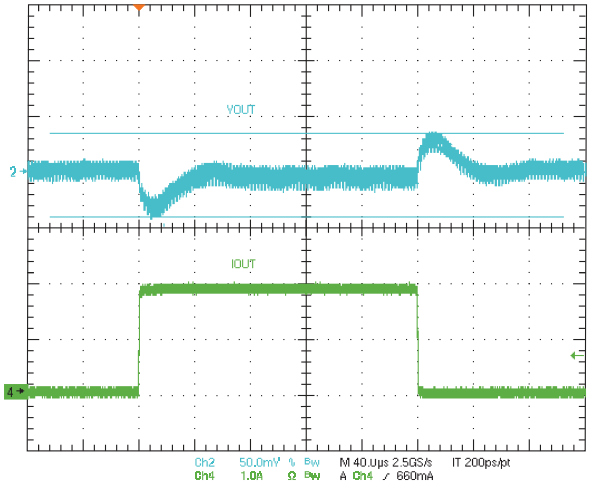


Figure 13: Load Step, CCM, V_{OUT} = 3.3V

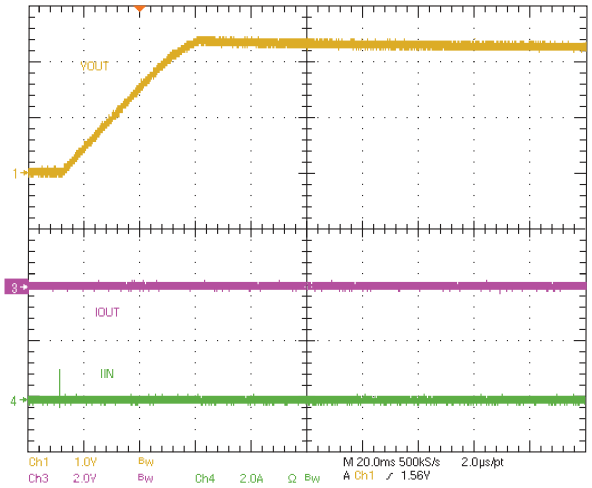


Figure 14: Start-Up, I_{OUT} = 0A

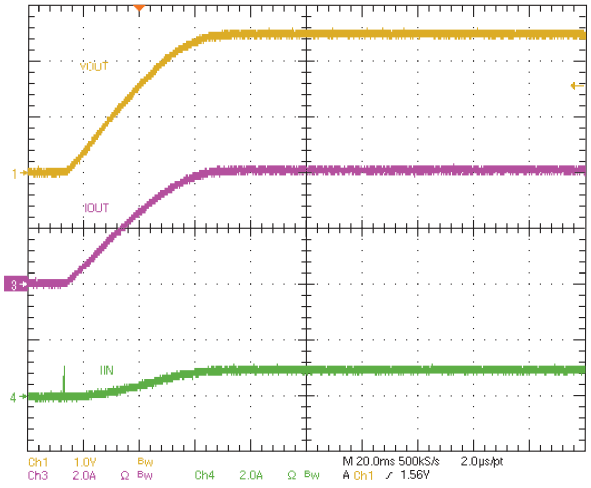


Figure 15: Start-Up, I_{OUT} = 4A

Functional Block Diagram

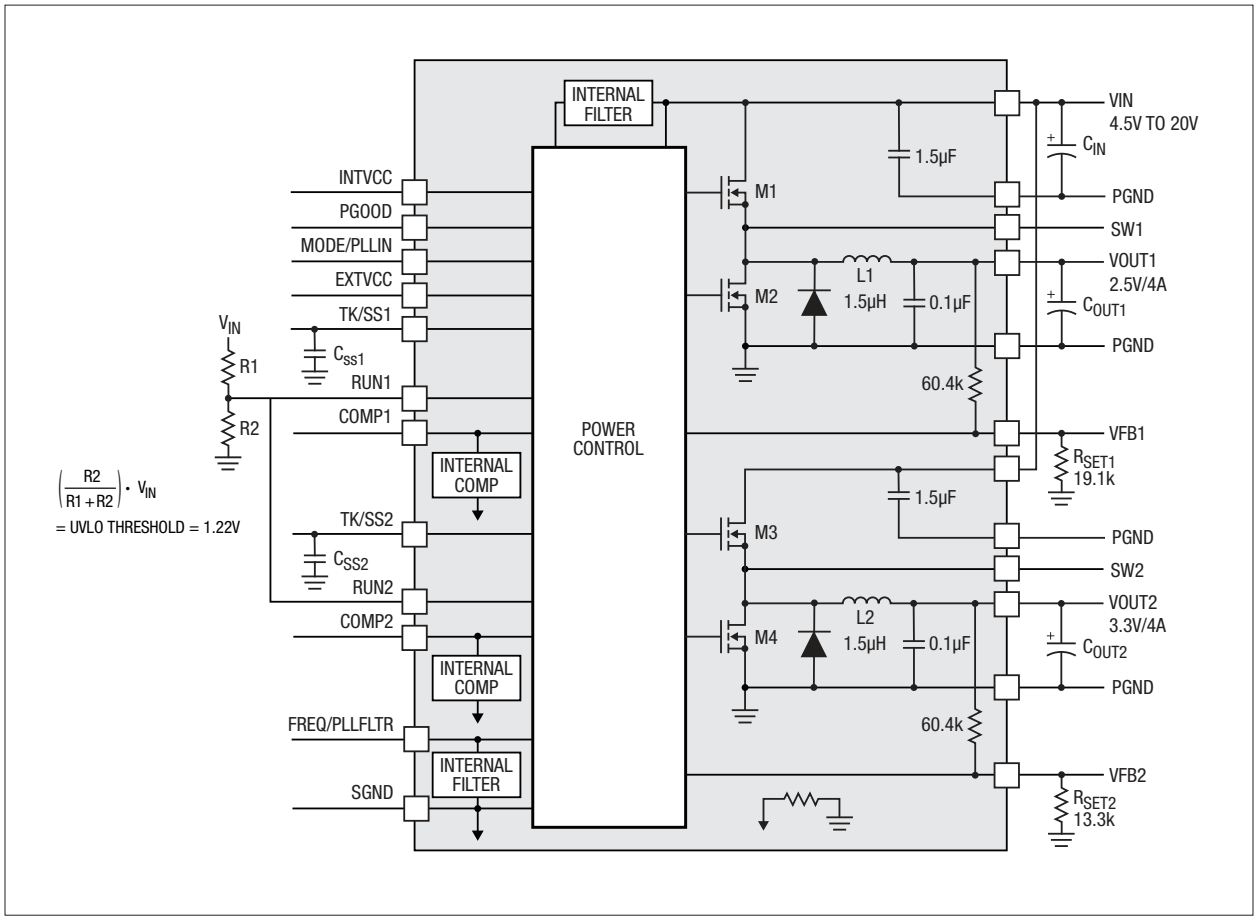


Figure 16: Functional Block Diagram

Applications Information

Power Module Description

The MxL7204 is a dual-output, standalone, synchronous step-down power module. This power module will have a continuous input voltage range of 4.5V to 20V optimized for 12 V_{IN} conversions. Output currents are up to 4A per channel. The module provides precisely regulated output voltages from 0.6V to 5.0V programmable via a single external resistor. See typical application schematic.

The module employs a constant frequency, peak current mode control loop architecture. With the current mode control and internal feedback loop compensation, the module has sufficient stability margins and good transient performance with a wide range of output capacitors including low ESR ceramic capacitors.

Current mode control provides cycle by cycle fast current limit and the current limit hiccup response in an overcurrent or output short circuit condition. Internal overvoltage and under voltage comparators pull the open drain PGOOD output low if the output voltage exits the ±10% regulation window around the output voltage set point. As the output voltage exceeds the +10% threshold, the low side FET will turn on to clamp the output voltage while keeping the high side MOSFET off. The overvoltage and under voltage detection is feedback pin referred.

The RUN pin enables and disables the respective channel of the module. Pulling RUN pin below 1.1V forces the respective regulator into shutdown mode and turns off both the high side and low side MOSFETs. The TRACK pins are used for programming the output voltage ramp and voltage tracking during start-up.

The typical switching frequency is 780kHz. The switching frequency can be programmed from 250kHz to 780kHz using the external programming resistor. For noise sensitive applications, the module can be synchronized to an external clock.

High efficiency at light loads is accomplished via the pulse-skip mode of operation using the MODE/PLLIN pin that accommodates battery operation to extend battery life.

The EXTVCC pin allows an external 5V supply to power the module and reduce the power dissipation in the internal 5V LDO. The EXTVCC has a threshold of 4.7V for activation and a max rating of 6V and must sequence on after V_{IN} and sequence off before V_{IN}.

Typical Application Circuit

The typical MxL7204 application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and output voltage.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} stepdown ratio that can be achieved for a given input voltage.

Each output of the MxL7204 is capable of 95% duty cycle at 500kHz, but the V_{IN} to V_{OUT} minimum dropout is still shown as a function of its load current and will limit output current capability related to high duty cycle on the top side switch. Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 90ns.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4kΩ internal feedback resistor connects between the VOUT1 to VFB1 and VOUT2 to VFB2. Adding a resistor R_{SETx} from VFB pin to SGND programs the output voltage:

$$V_{OUT} = 0.6V \times \frac{60.4k + R_{SETx}}{R_{SETx}} \quad , \; R_{SETx} = \frac{60.4k \times 0.6V}{V_{OUT} - 0.6V}$$

Table 6: VFB Resistor Table vs Various Output Voltages

V_{OUT}	0.6V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R_{SETx}	Open	90.9k	60.4k	40.2k	30.1k	19.1k	13.3k	8.25k

Note that when used in paralleled output mode (see Figure 33 for 5V example), the internal 60.4kΩ feedback resistor of both VOUT are in parallel. Therefore the following equations and table should be used for this mode.

$$V_{OUT} = 0.6V \times \frac{30.2k + R_{SET}}{R_{SET}} \quad , \; R_{SET} = \frac{30.2k \times 0.6V}{V_{OUT} - 0.6V}$$

Table 7: VFB Resistor Table vs Various Output Voltages for Paralleled Output Mode

V_{OUT}	0.6V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R_{SET}	Open	45.3k	30.1k	20.0k	15.0k	9.53k	6.65k	4.12k

Input Capacitors

The MxL7204 module should be connected to a low AC impedance DC source. For the regulator input, two 22µF input ceramic capacitors are used for RMS ripple current.

A 47µF to 150µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance.

Output Capacitors

The MxL7204 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, the low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 100µF to 220µF.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the MxL7204 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE/PLLIN pin to INTVCC enables pulse-skipping operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced Continuous Conduction Mode (CCM) should be used. Forced continuous operation can be enabled by tying the MODE/PLLIN pin to GND.

Multiphase Operation

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design. Figure 33 is an example of a two phase application.

Input RMS Ripple Current Cancellation

The input RMS ripple current cancellation effects of multi-phased interleaved operation are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases as shown in Figure 17.

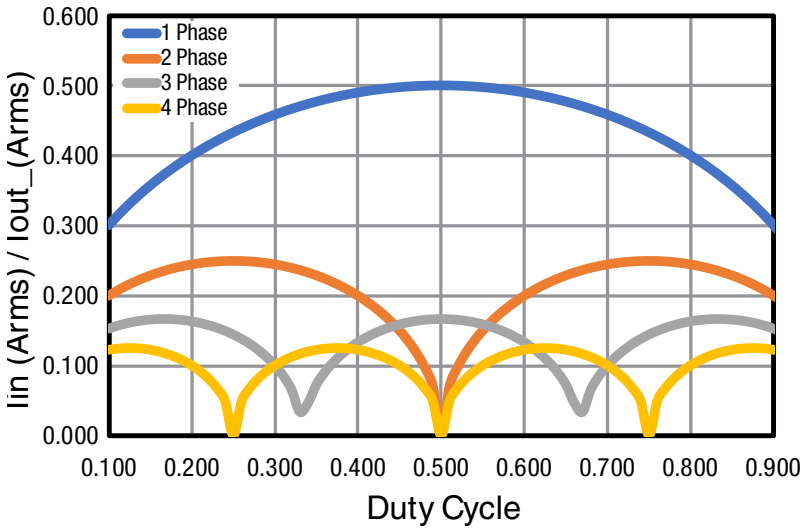


Figure 17: Normalized Input RMS Ripple Current vs Duty Cycle for One to Four Phases

Frequency Selection and Phase-Lock Loop (MODE/PLLIN and fSET Pins)

The MxL7204 device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the lower output voltages or lower duty cycle conversions at lower frequencies to improve efficiency by lowering power MOSFET switching losses. Higher output voltages or higher duty cycle conversions can be operated at higher frequencies to limit inductor ripple current. The efficiency graphs will show an operating frequency chosen for that condition. Select frequency in reference to the highest output voltage.

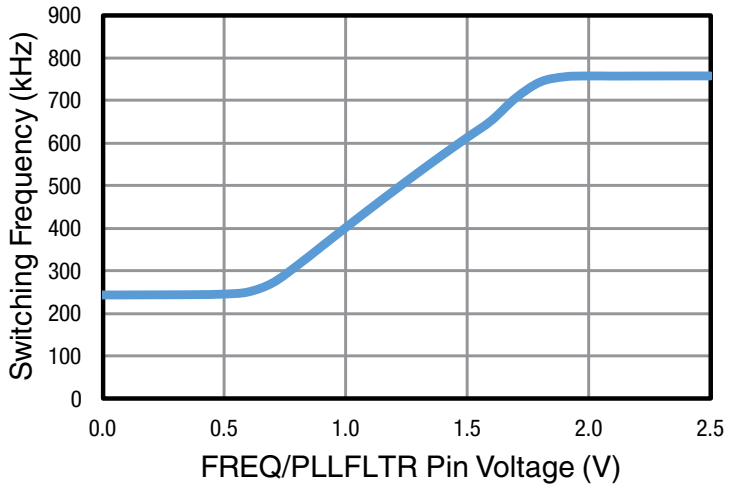


Figure 18: Operation Frequency vs. FREQ/PLLFLTR Pin Voltage

The MxL7204 switching frequency can be set with an external resistor from the FREQ/PLLFLTR pin to SGND. An accurate 10µA current source into the resistor will set a voltage that programs the frequency or a DC voltage can be applied. Figure 18 shows a graph of frequency setting versus programming voltage. An external clock can be applied to the MODE/PLLIN pin from 0V to $INTV_{CC}$ over a frequency range of 400kHz to 780kHz. The clock input high threshold is 1.6V and the clock input low threshold is 1V. The MxL7204 has the PLL loop filter components on board. The frequency setting resistor should always be present to set the initial switching frequency before locking to an external clock. Both regulators will operate in continuous mode while being synchronized to an externally clock signal.

The output of the PLL phase detector has a pair of complementary current sources that charge and discharge the internal filter network. When the external clock is applied, then the FREQ/PLLFLTR frequency resistor is disconnected with an internal switch and the current sources control the frequency adjustment to lock to the incoming external clock. When no external clock is applied, then the internal switch is on, thus connecting the external FREQ/PLLFLTR frequency set resistor for free run operation.

Minimum On-Time

Minimum on-time t_{ON} is the smallest time duration that the MxL7204 is capable of turning on the top MOSFET on either channel. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \times FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple will increase. The on-time can be increased by lowering the switching frequency. A good rule of thumb is to keep on-time longer than 110ns.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pins. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The MxL7204 uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 20 shows an example of coincident tracking. Equations:

$$SLAVE = \left(1 + \frac{60.4k}{R2}\right) \times V_{TRACK}$$

VTRACK is the track ramp applied to the slave's track pin. VTRACK has a control range of 0V to 0.6V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, the slave will coincidentally track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when VTRACK is more than 0.6V. R2 in Figure 19 will be equal to the R_{SET2} for coincident tracking. The TRACK pin can be controlled by a capacitor placed on the regulator TRACK pin to ground. A 1.25µA current source will charge the TRACK pin up to the reference voltage and then proceed up to INTVCC. After the 0.6V ramp, the TRACK pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. The TRACK pins are pulled low when the RUN pin is below 1.1V. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = \left(\frac{C_{SS}}{1.25\mu A}\right) \times 0.6$$

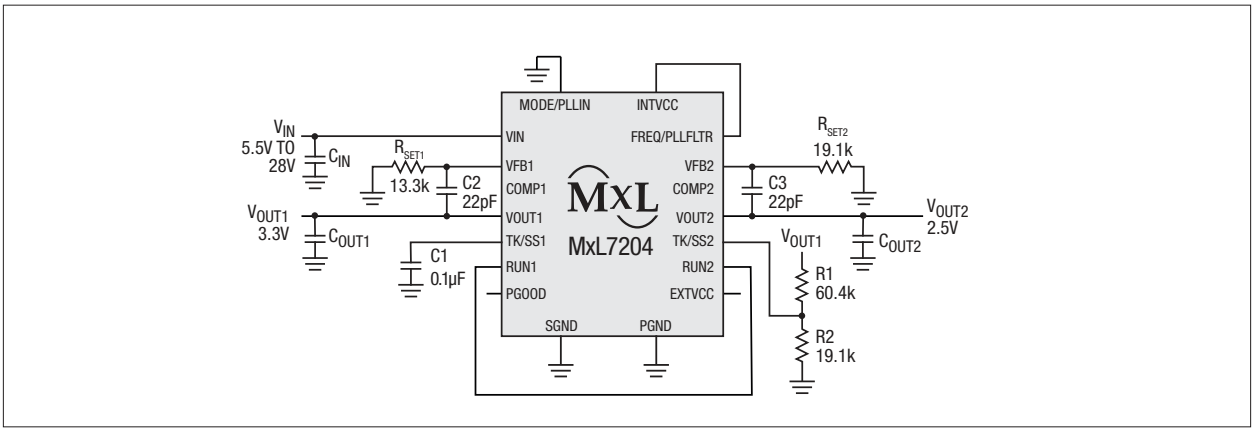


Figure 19: Example of Output Tracking Application Circuit

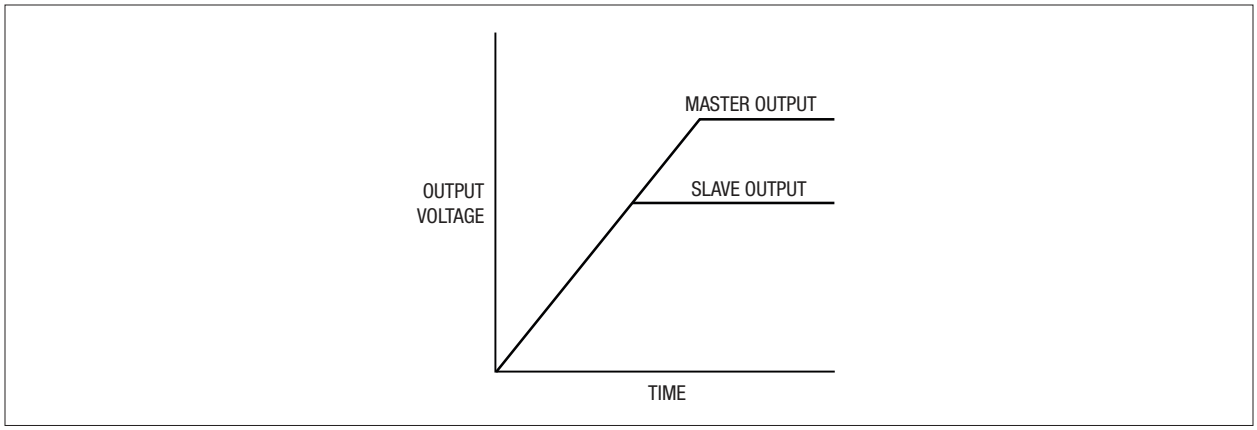


Figure 20: Output Coincident Tracking Waveform

Power Good

The PGOOD pin is an open drain pin that can be used to monitor valid output voltage regulation on both channels. This pin monitors a ±10% window around the regulation point. The PGOOD pin is pulled low when either output is outside the monitoring window, the RUN pin is below its threshold (1.25V) or when the MxL7204 is in the soft start or tracking phase. The PGOOD pin will flag power good immediately when both VFB pins are within the monitoring window. Note that there is an internal 20µs delay when VFB voltage goes out of the monitoring window.

Stability Compensation

The module has already been internally compensated for all output voltages. For improved phase margin, particularly at low output voltages, the following criteria should be met. Be sure to take capacitor deratings into account.

Table 8: Capacitor Selection

V_{OUT}		C_O min	C_{FF}
From	To		
0.6V	1.8V	200µF, Poly	22pF
1.8V	3.3V	≥100µF, Ceramic	22pF
3.3V	5.0V	≥75µF, Ceramic	22pF

Run Enable

The RUN pins have an enable threshold of 1.4V maximum, typically 1.25V with 200mV of hysteresis. They control the turn on each of the channels and $INTV_{CC}$. These pins can be pulled up to VIN for 5V operation, or a 5V Zener diode and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the channels. The RUN pins can also be used for output voltage sequencing.

$INTV_{CC}$ and $EXTV_{CC}$

The MxL7204 module has an internal 5V low dropout regulator that is derived from the input voltage.

$EXTV_{CC}$ allows an external 5V supply to power the MxL7204 and reduce power dissipation from the internal low dropout 5V regulator.

SW Pins

The SW pins are generally used for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths.

Thermal Considerations and Output Current Derating

The MxL7204 module has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board.

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are many factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated (P_{DISS}).

The thermal resistances of the MxL7204 is shown in the “Operating Ratings” section of this datasheet. The JEDEC θ_{JA} thermal resistance provided is based on tests that comply with the JESD51-2A “Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection” standard. JESD51-xx are a group of standards whose intent is to provide comparative data based on a standard test condition which includes a defined board construction. Since the actual board design in the final application will be different from the board defined in the standard, the thermal resistances in the final design may be different from those shown.

The package thermal derating curve is shown in Figure 21. The total package power dissipation (P_{PKG}) is dependent on the final application and is the sum of the losses for the two channels. The power losses for a channel will depend mainly on the input voltage, output voltage, and output current. Figure 22 and Figure 23 show the power losses for input voltages of 5V, 12V and 20V and for V_{OUT} voltages of 1.5V and 3.3V respectively (V_{IN}/V_{OUT}). Figures 24 through 29 show output current derating versus ambient temperature for various V_{IN} and V_{OUT} (V_{IN}/V_{OUT}) ratios with 0, 1, and 2 meters per second (m/s) of airflow.

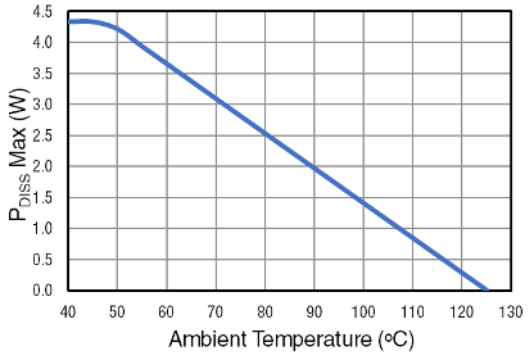


Figure 21: Package Pmax Derating vs. Ambient Temperature

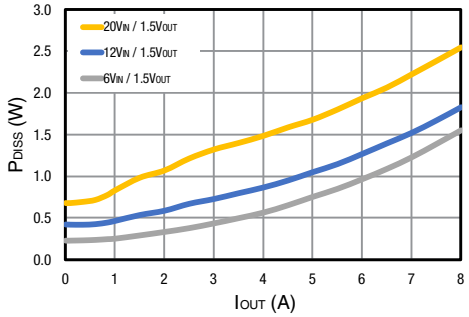


Figure 22: Power Loss, V_{OUT} = 1.5V, 500kHz

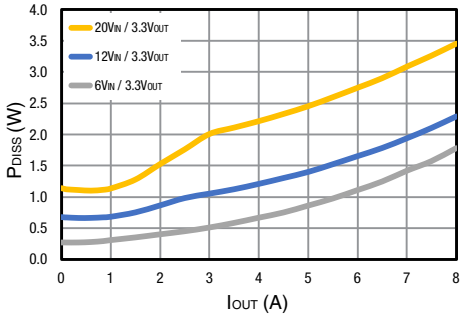


Figure 23: Power Loss, V_{OUT} = 3.3V, 780kHz

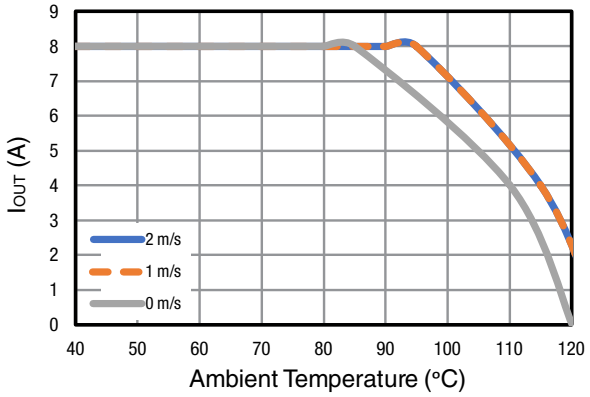


Figure 24: Output Current Derating vs. $T_{AMBIENT}$, $6V_{IN}$, $1.5V_{OUT}$

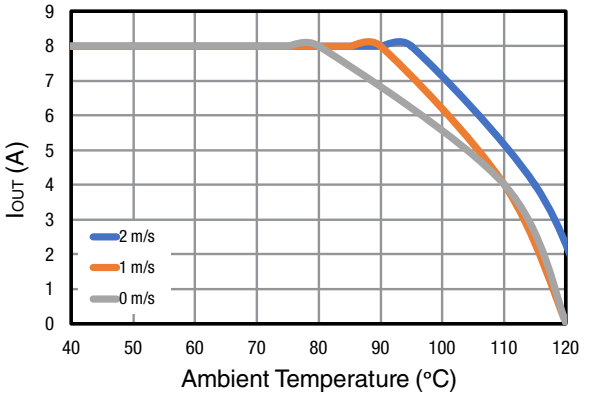


Figure 25: Output Current Derating vs. $T_{AMBIENT}$, $6V_{IN}$, $3.3V_{OUT}$

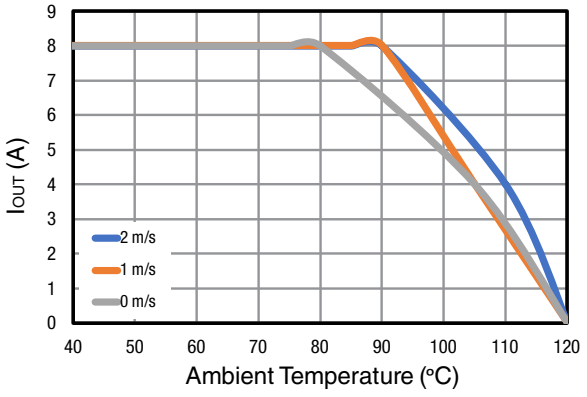


Figure 26: Output Current Derating vs. $T_{AMBIENT}$, $12V_{IN}$, $1.5V_{OUT}$

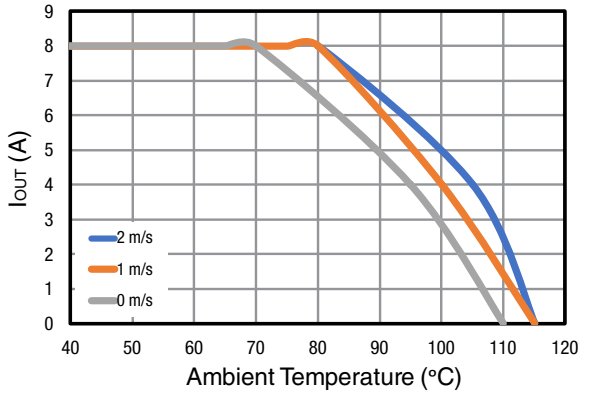


Figure 27: Output Current Derating vs. $T_{AMBIENT}$, $12V_{IN}$, $3.3V_{OUT}$

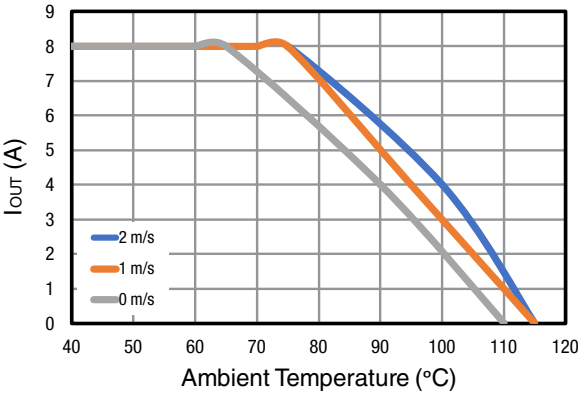


Figure 28: Output Current Derating vs. $T_{AMBIENT}$, $20V_{IN}$, $1.5V_{OUT}$

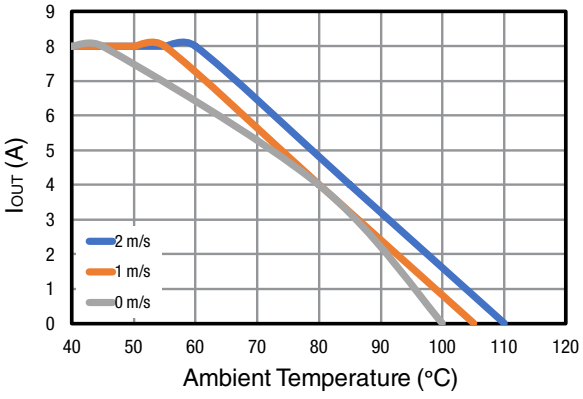


Figure 29: Output Current Derating vs. $T_{AMBIENT}$, $20V_{IN}$, $3.3V_{OUT}$

Fault Protection

The MxL7204 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation.

The device does support over current protection, and over temperature protection which will be activated if the internal temperature increases to dangerous levels.

Layout Checklist and Example

The high integration of MxL7204 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including VIN, PGND, VOUT1 and VOUT2. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the VIN, PGND and VOUT pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.
- Bring out test points on the signal pins for monitoring.

Figure 30 gives a good example of the recommended layout.

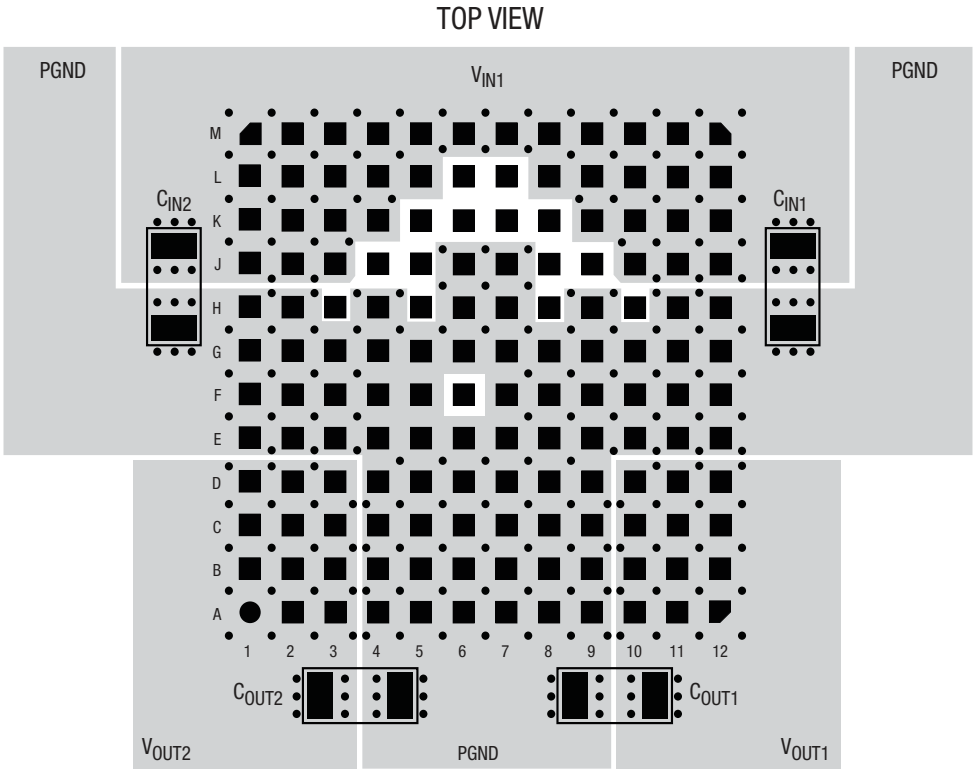


Figure 30: Recommended PCB Layout

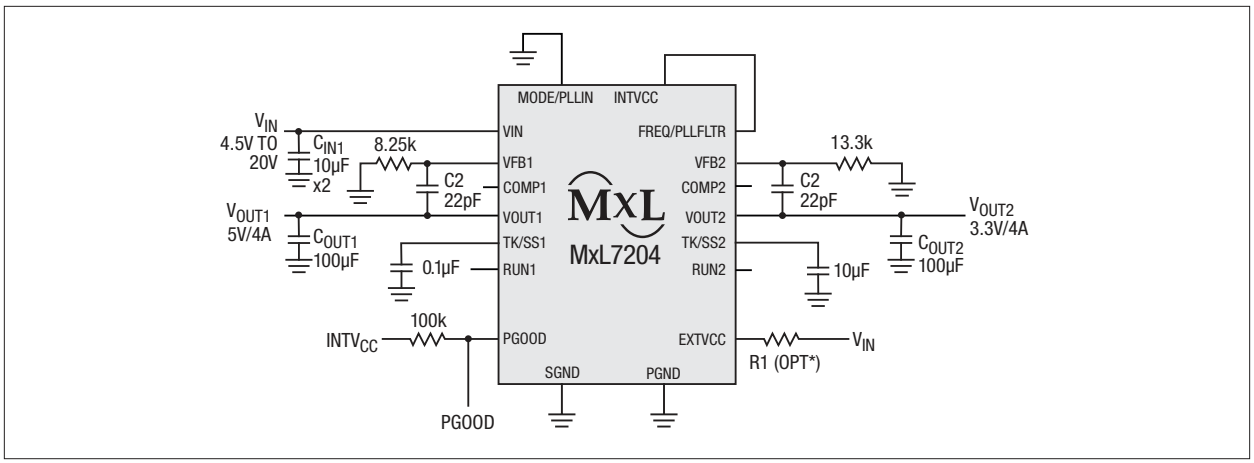


Figure 31: Typical 4.5V to 20V Input, 5V and 3.3V Outputs at 4A Design

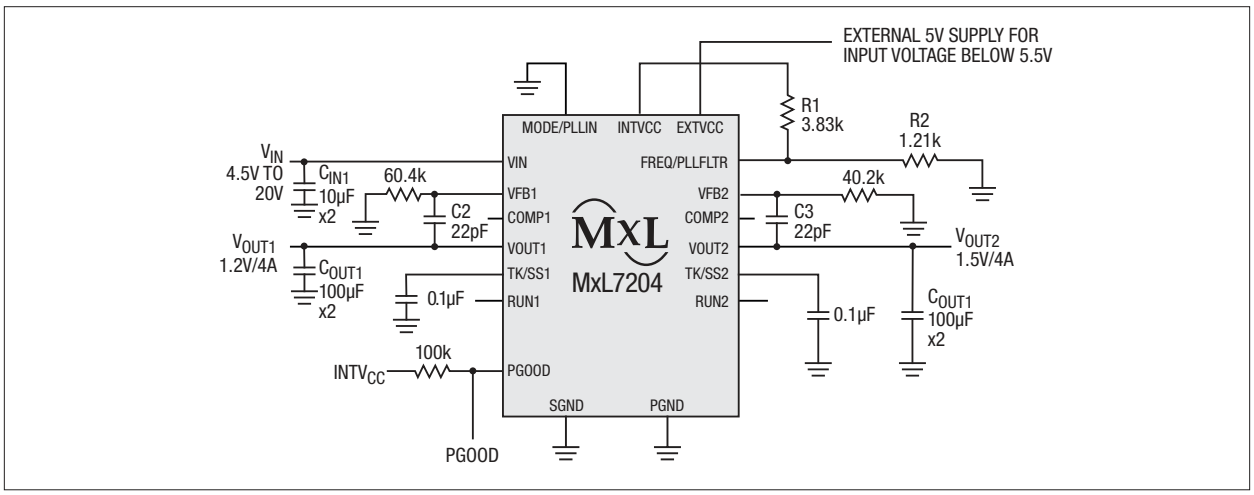


Figure 32: Typical 4.5V to 20V Input, 1.2V and 1.5V Outputs at 4A Design with Adjusted Frequency at 500kHz

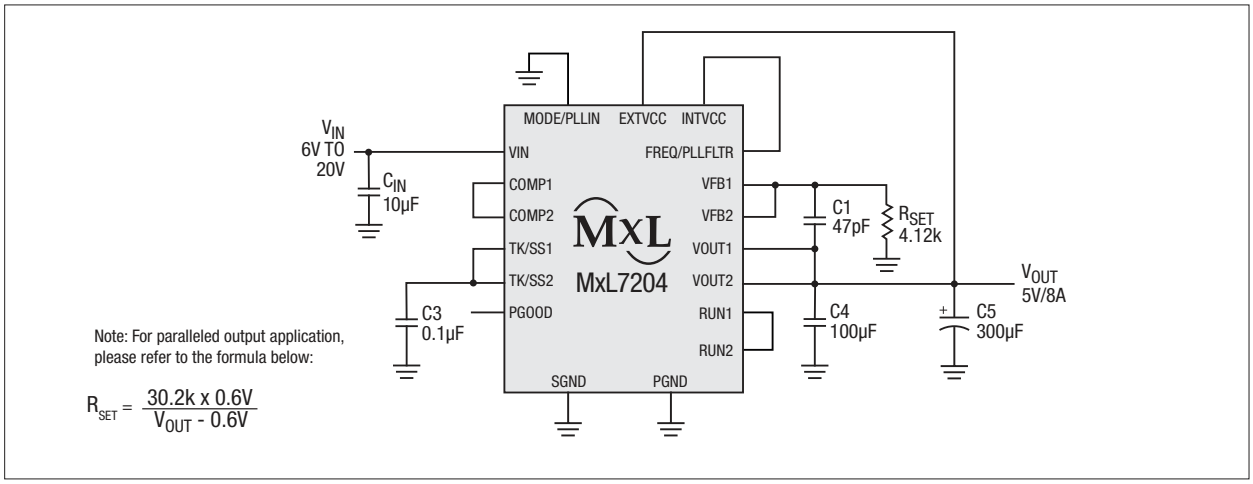
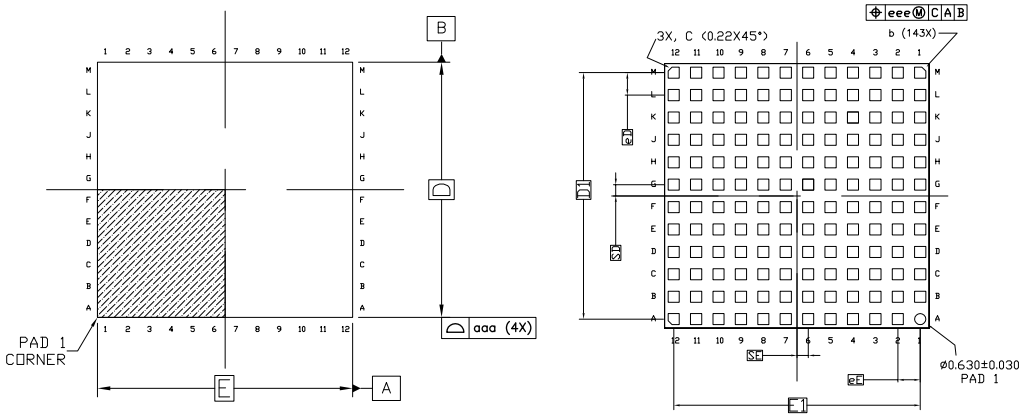


Figure 33: Output Paralleled for 5V at 8A Design

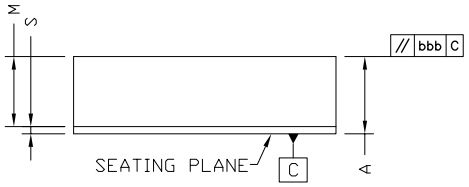
Mechanical Dimensions

15mm x 15mm x 2.82mm LGA



TOP VIEW

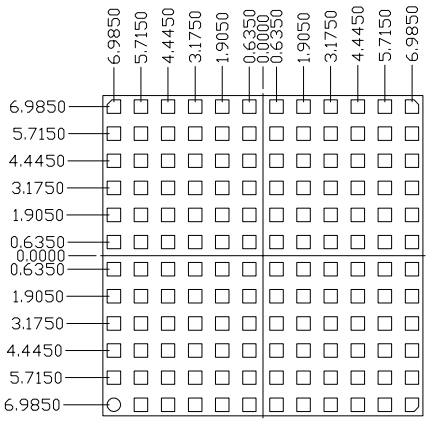
BOTTOM VIEW



SIDE VIEW

		Symbol	Common Dimensions
Package :			SIPLGA
Body Size:	X	E	15.000
	Y	D	15.000
LGA Pad Pitch :	X	eE	1.270
	Y	eD	1.270
Total Thickness :		A	2.820±0.10
Mold Thickness :		M	2.500±0.05
Substrate Thickness :		S	0.320±0.04
LGA Pad Size :		b	SQ 0.630±0.030
Stand Off :		A1	N/A
Ball Width :			N/A
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.100
Coplanarity:		ddd	N/A
LGA Pad Offset (Land) :		eee	0.050
Ball Offset (Ball) :		fff	N/A
LGA Pad Count :		n	144
Edge LGA Pad Center to Center :	X	E1	13.970
	Y	D1	13.970
Center Pkg To Adjacent Center Of LGA Pad :		SE	0.635
		SD	0.635

TERMINAL DETAILS



Suggested PCB Layout

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

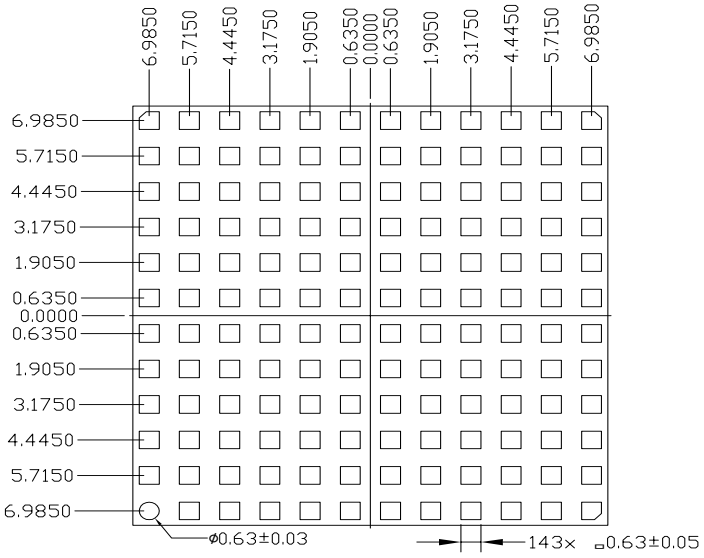
Drawing No.: POD-00000089

Revision: A.1

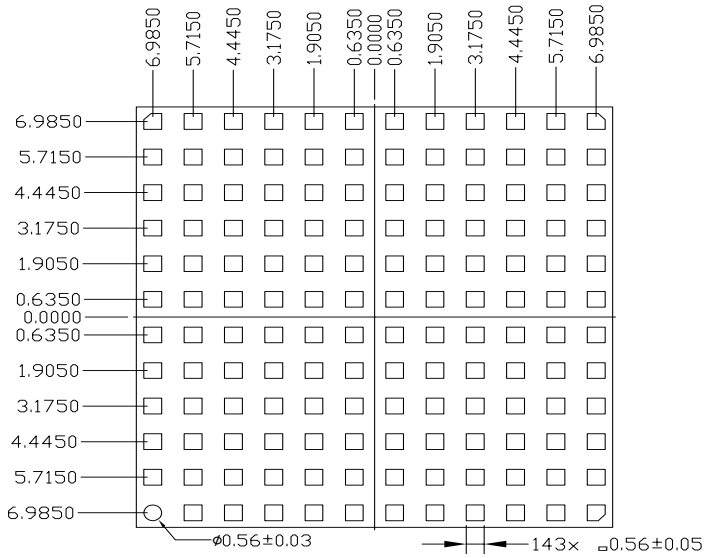
Figure 34: Mechanical Dimensions

Recommended Land Pattern and Stencil

15mm x 15mm x 2.82mm LGA



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000089

Revision: A.1

Figure 35: Recommended Land Pattern and Stencil

Ordering Information

Table 9: Ordering Information[1]

Ordering Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
MXL7204-AYA-T	-40°C ≤ T_J ≤ 125°C	Yes[2]	LGA144 15x15	Tray
MXL7204EVB	MxL7204 Evaluation Board			

NOTE:
1. Refer to www.exar.com/MxL7204 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
760.692.0711 p
760.444.8598 f
www.maxlinear.com

High Performance Analog
1060 Rincon Circle
San Jose, California 95131 USA
669.265.6100 p
669.265.6101 f
www.exar.com