# Development Board EPC90141 Quick Start Guide

*100 V Half-bridge with Gate Drive, Using EPC2070*

Revision 1.0

**EPC**

EFFICIENT POWER CONVERSION

## DESCRIPTION

The EPC90141 is a half bridge development board with onboard gate drives, featuring the 100 V rated EPC2070 GaN field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2070 by including all the critical components on a single board that can be easily connected into the majority of existing converter topologies.

The EPC90141 development board measures 2" x 2" and contains two EPC2070 GaN FET in a half bridge configuration and one EPC2038 GaN FET used to augment the bootstrap supply. The EPC90141 features the uPI Semiconductor uP1966E gate driver. The board also contains all critical components and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on **EPC2070** please refer to their datasheets available from EPC at **www.epc-co.com**. The datasheet should be read in conjunction with this quick start guide.

**Table 1: Performance Summary (T$_A$ = 25°C) EPC90141**

| Symbol | Parameter | Conditions | Min | Nominal | Max | Units |
|--------|-----------|------------|-----|---------|-----|-------|
| $V_{DD}$ | Gate Drive Regulator Supply Range | | 7.5 | | 12 | V |
| $V_{IN}$ | Bus Input Voltage Range[1] | | | | 80 | V |
| $I_{OUT}$ | Switch Node Output Current [2] | | | | 5 | A |
| $V_{PWM}$ | PWM Logic Input Voltage Threshold [3] | Input 'High' | 2.3 | | | V |
| | | Input 'Low' | | | 0.5 | V |
| | PWM 'High' State Input Pulse Width | $V_{PWM}$ rise and fall time < 10ns | 20 | | | ns |
| | PWM 'Low' State Input Pulse Width [4] | $V_{PWM}$ rise and fall time < 10ns | See Note 4 | | | ns |

*(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 100 V for EPC2070.*

*(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.*

*(3) When using the on board logic buffers, refer to the uP1966E datasheet when bypassing the logic buffers.*

*(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.*
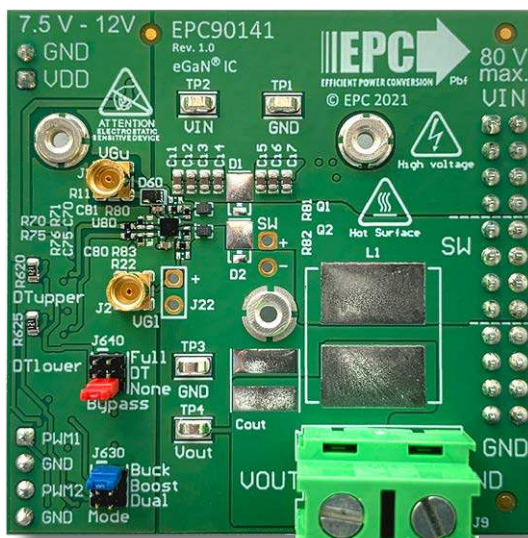


Front view



Back view
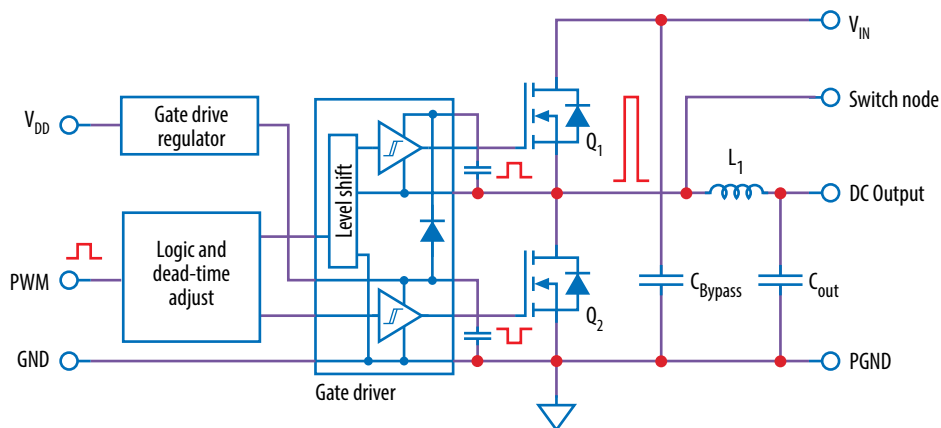
**EPC90141 development board**



*Figure 1: Block diagram of EPC90141 development board default configuration*

## QUICK START PROCEDURE

The EPC90141 development board is easy to set up as a buck or boost converter to evaluate the performance of two EPC2070 eGaN FETs. This board includes a logic PWM input signal polarity changer used to ensure positive PWM polarity for the switching device when configured in either the buck or boost modes, and can accommodate both single and dual PWM inputs. Furthermore, the board includes a dead-time generating circuit that adds a delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. In the default configuration, this dead time circuit ensures that both the high and low side FETs will not be turned on at the same time thus preventing a shoot-through condition.  The dead-time and/or polarity changing circuits can be utilized or bypassed for added versatility.

### Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM for the FETs. The input mode is set by choosing the appropriate jumper positions for J630 (mode selection) as shown in figure 2(a) for a single-input buck converter (**blue** jumper across pins 1 & 2 of J630), (b) for a single-input boost converter (**blue** jumpers across pins 3 & 4 of J630),  and (c) for a dual-input operation (**blue** jumpers across pins 5 & 6 of J630).

**Note**: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time.

### Dead-time settings

*Dead-time* is defined as the time between when one FET turns off and the other FET turns on, and for this board is referenced to the input of the gate driver. The dead-time can be set to a specific value where resistor R620 delays the turn on of the upper FET and resistor R625 delays the turn on of the lower FET as illustrated in figure 3.

The required resistance for the desired dead-time setting can be read off the graph in figure 4. An example for 10 ns dead-time setting shows that a 120 Ω resistor is needed.

**Note**: This is the default deadtime and resistor value installed. A minimum dead-time of is 5 ns and maximum of 15 ns is recommended.

### Bypass settings

Both the polarity changer and the deadtime circuits can be bypassed using the jumper settings on J640 (Bypass), for direct access to the gate driver input. There are three bypass options: 1) No bypass, 2) Dead-time bypass, 3) Full bypass. The jumper positions for J640 for all three bypass options are shown in figure 5.
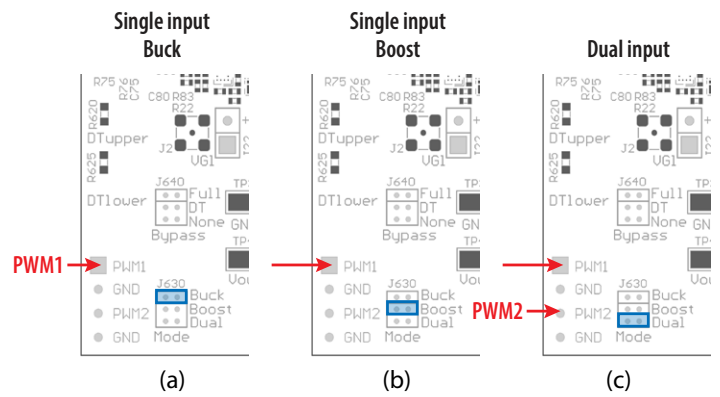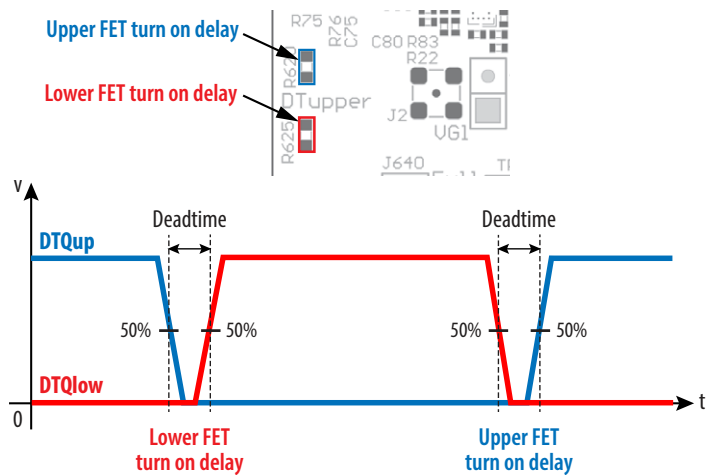


Figure 2:  Input mode selection on J630



Figure 3:  Definition of dead-time between the upper-FET gate signal (DTQup) and the lower-FET gate signal (DTQlow)
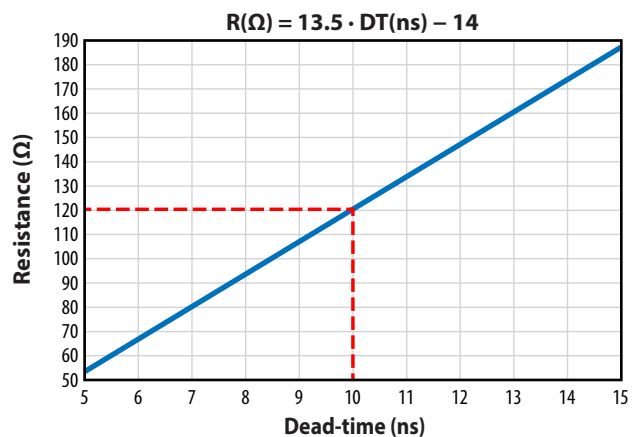


$$R(\Omega) = 13.5 \cdot DT(ns) - 14$$

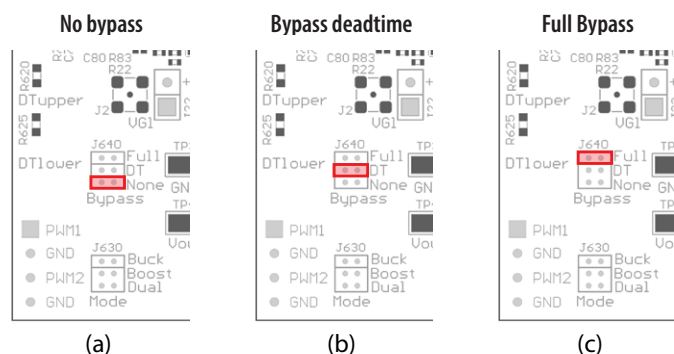Figure 4:  The required resistance values for R620 or R625 as a function of desired dead-time



Figure 5: Bypass mode Jumper settings for J640

In **no-bypass mode**, figure 5(a) (red jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized. In **dead-time bypass mode**, figure 5(b) (red jumpers across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit. In **full bypass mode**, Figure 5(c) (red jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized.

### Bypass mode warnings

- *It is important to provide the correct PWM signals that includes dead-time and polarity for either buck or boost operation when making use of bypass modes.*

- When operating in **full bypass mode**, the input signal specifications revert to that of the uP1966A gate driver IC. Refer to the uP1966A datasheet for details.

### Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select **Single Input Buck Mode**, the bypass jumper J640 **must** be set to the **no-bypass mode**, the **buck mode** J630 **must** be selected as shown in figure 6(a).

To select **Dual Input Buck Mode**, the bypass jumper J640 **may** be configured to any of the valid settings, the dual-input mode J630 **must** be selected as shown in figure 6(b).

**Note**: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. With power off, connect the input power supply bus to VIN and ground / return to GND.

2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 6.

3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).

4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.

5. Turn on the gate drive supply – make sure the supply is set between 7.5 V and 12 V.

6. Turn on the controller / PWM input source.

7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (*do not exceed the absolute maximum voltage*). Probe switch-node to see switching operation.

8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.

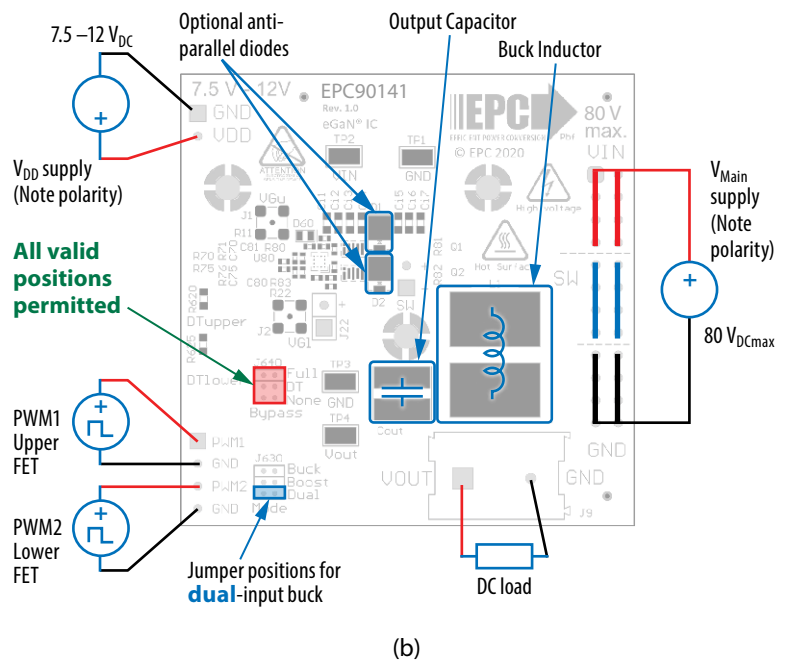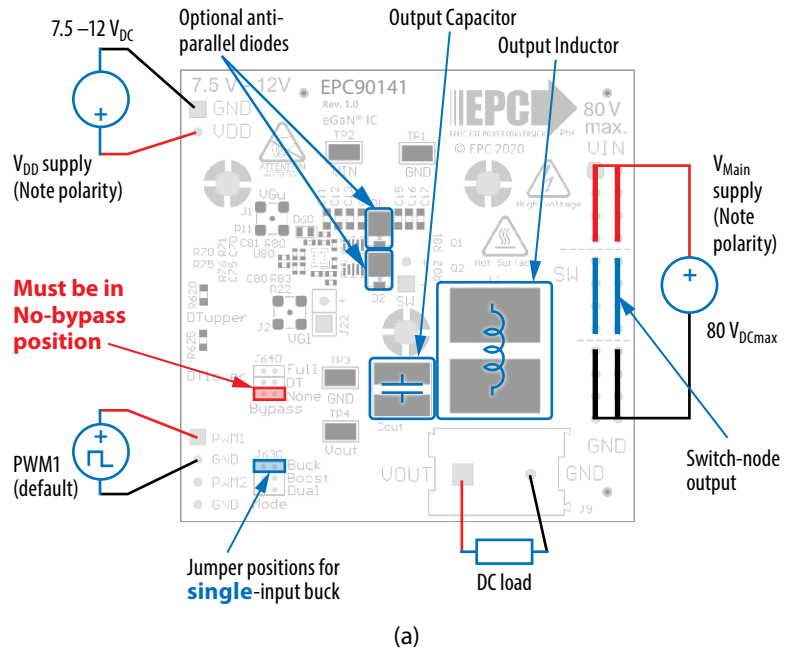9. For shutdown, please follow steps in reverse.



(a)



(b)

*Figure 6: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.*

## Boost Converter configuration

*Warning: Never operate the boost converter mode without a load, as the output voltage can increase beyond the maximum ratings.*

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select **Single Input Boost Mode**, the bypass jumper J640 **must** be set to the **no-bypass mode**, the boost mode J630 **must** be selected as shown in figure.7(a).

To select **Dual Input Boost Mode**, the bypass jumper J640 **may** be configured to any of the valid settings, the **dual-input mode** J630 **must** be selected as shown in figure 7(b).

**Note**: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 7, or provided off board. Anti-parallel diodes can also be installed using the additional pads on the right side of the EPC2070 FETs.

2. With power off, connect the input power supply bus to $V_{OUT}$ and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (**labeled as VIN**) to your circuit as required, e.g., resistive load.

3. With power off, connect the gate drive supply to $V_{DD}$ (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).

4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.

5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.

6. Turn on the controller / PWM input source.

7. **Making sure the output is not open circuit**, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (*do not exceed the absolute maximum voltage*). Probe switch-node to see switching operation.

8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.

9. For shutdown, please follow steps in reverse.



(a)



(b)
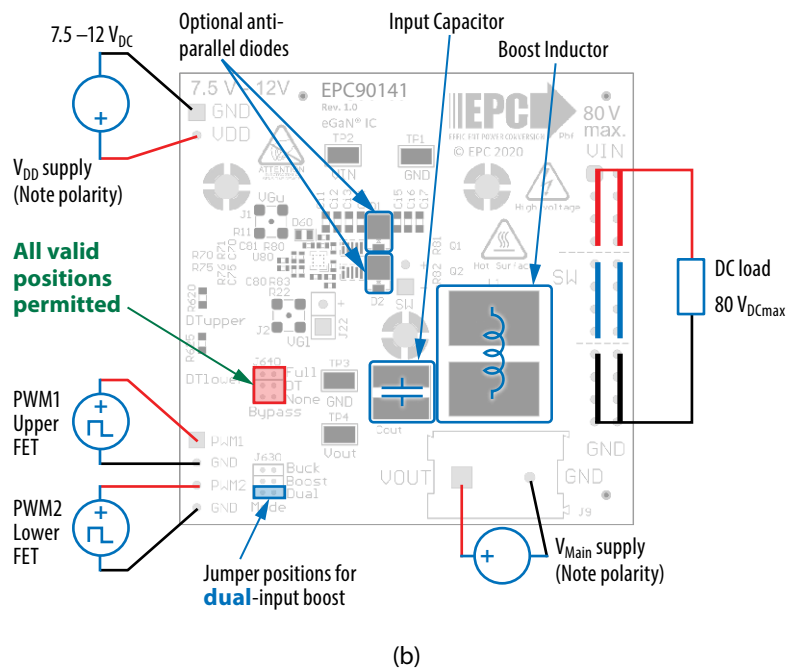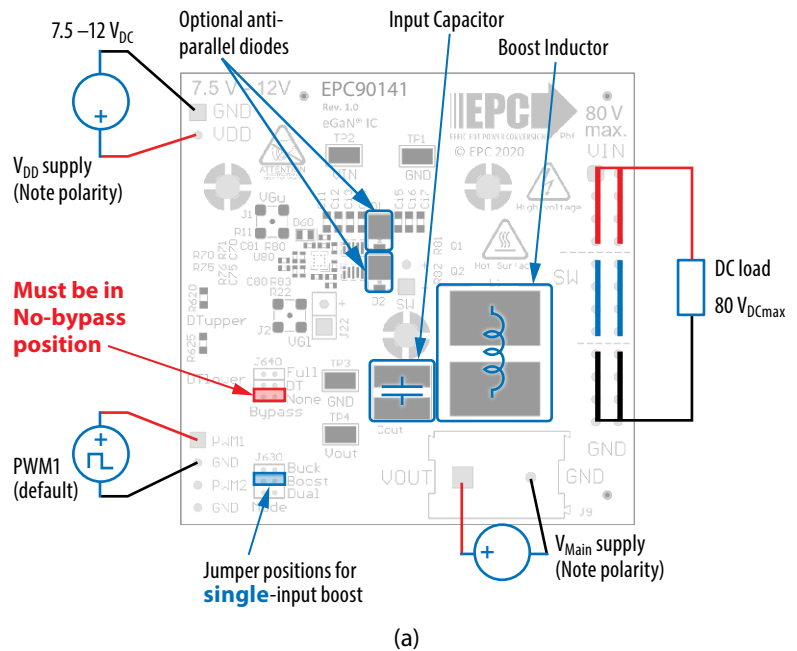
*Figure 7: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, input capacitor, PWM, and load connections with corresponding jumper settings.*

## MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 8. Figure 9 shows an actual switch-node voltage measurement when operating the board as a buck converter.

When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J33) and an MMCX connector (J32) are provided for switch-node measurement.

A differential probe is recommended for measuring the high-side bootstrap voltage. IsoVu probes from Tektronix has a mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx.

**NOTE.** For information about measurement techniques, the EPC website offers: "AN023 Accurately Measuring High Speed GaN Transistors" and the How to GaN educational video series, including: HTG09- Measurement



(a)



(b)
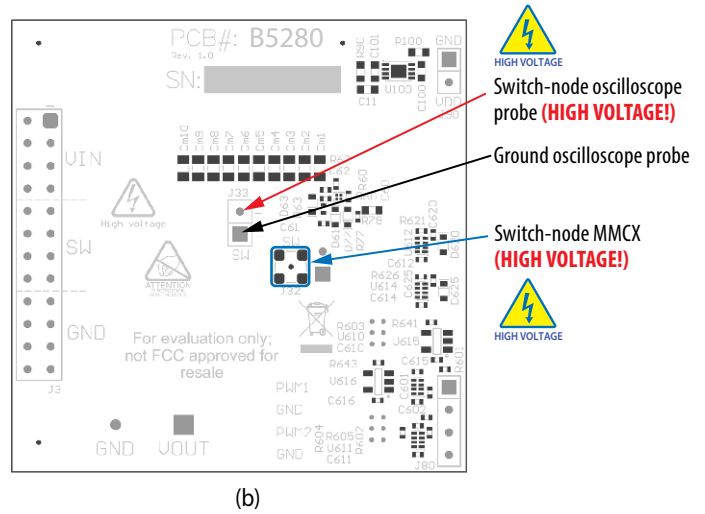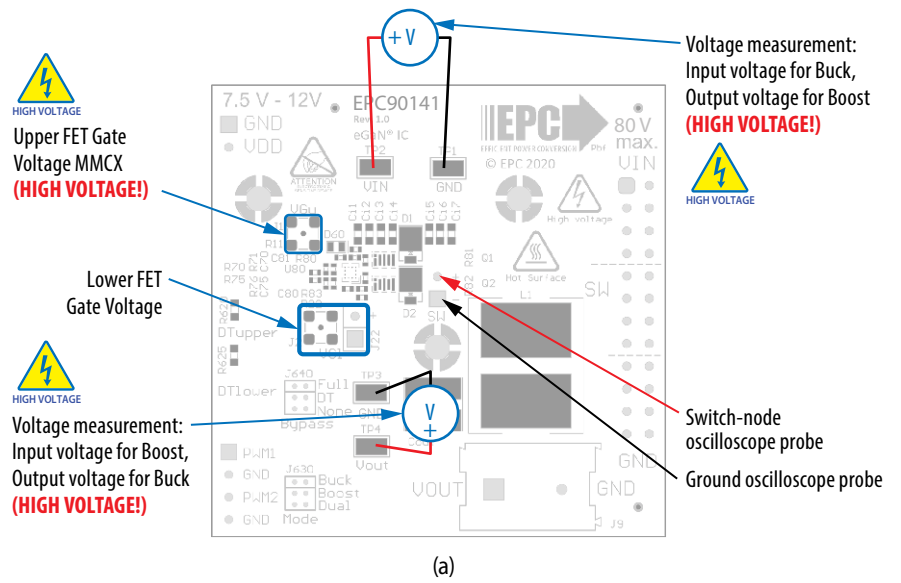
Figure 8:  Measurement points (a) top side, (b) bottom side
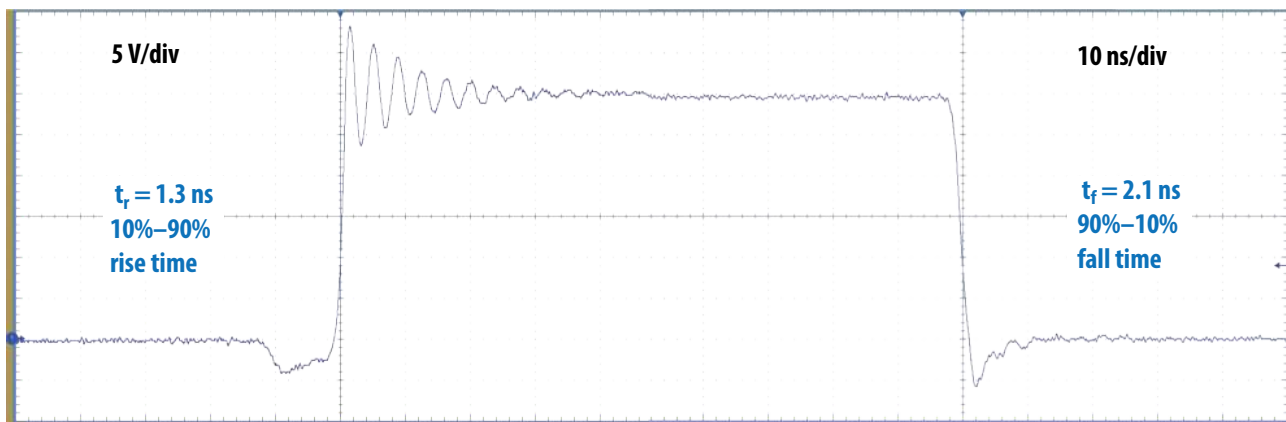


$V_{IN} = 32$ V, $V_{OUT} = 8$ V, $I_{OUT} = 20$ A, $f_{sw} = 250$ kHz, L = 2.2 µH

Figure 9:  Typical switch-node waveform when operated as a buck converter

## THERMAL CONSIDERATIONS

The EPC90141 board is equipped with three mechanical spacers that can be used to easily attach a heat-spreader or heatsink as shown in figure 10 (a), and only requires a thermal interface material (TIM), a custom shape heat-spreader/heatsink, and screws. Prior to attaching a heat-spreader, any component exceeding 1 mm in thickness under the heat-spreader area will need to be removed from the board as shown in figure 10 (b).
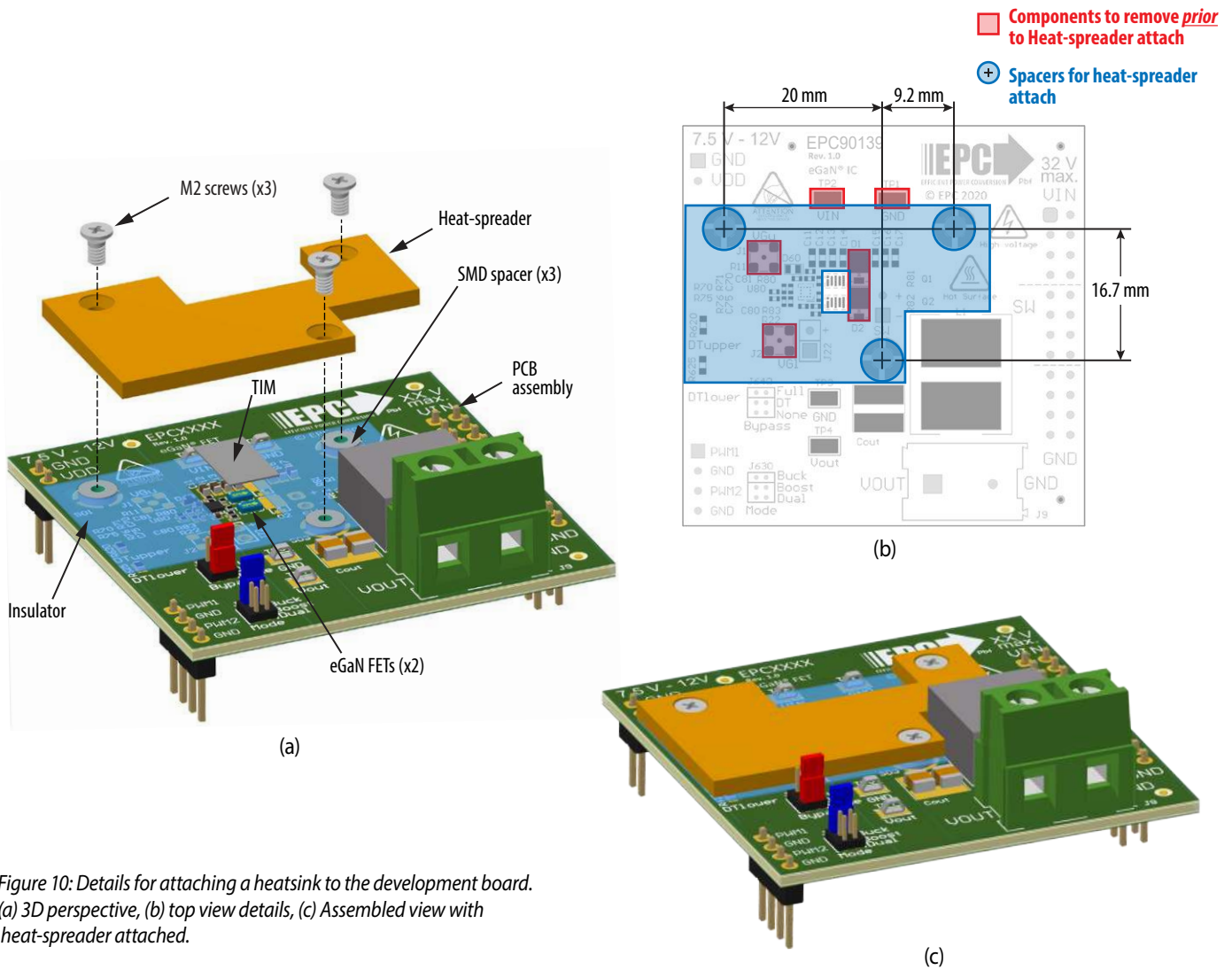


Figure 10: Details for attaching a heatsink to the development board. (a) 3D perspective, (b) top view details, (c) Assembled view with heat-spreader attached.

The design of the heat-spreader is shown in figure 11 and can be made using **aluminum** or **tellurium copper** for higher performance.

The heat-spreader is held in place using countersunk screws that fasten to the mechanical spacers which will accept M2 x 0.4 mm thread screws such as McMasterCarr 91294A002.

When assembling the heatsink, it may be necessary add a thin insulation layer to prevent the heat-spreader from short circuiting with components that have exposed conductors such as capacitors and resistors, as shown in figure 11. ***Note that the heat-spreader is ground connected by the lower most mounting post***. A rectangular opening in the insulator must be provided to allow the TIM to be placed over the FETs to be cooled with a minimum clearance of 3 mm on each side of the rectangle encompassing the FETs. The TIM will then be similar in size or slightly smaller than the opening in the insulator shown by the red dashed outline in figure 12.

EPC recommends Laird P/N: A14692-30, Tgard™ K52 with thickness of 0.051 mm the for the insulating material.

A TIM is added to improve the interface thermal conductance between the FETs and the attached heat exchanger. The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.

- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.

- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.
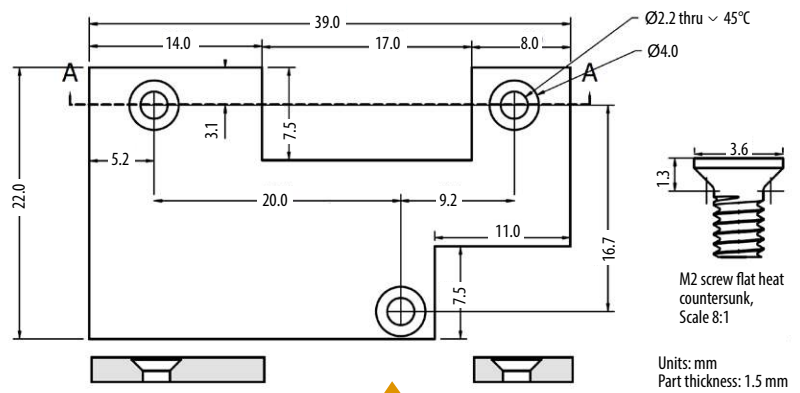


Figure 11: Heat-spreader details
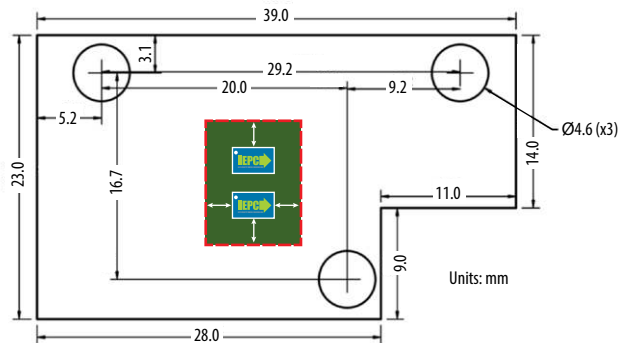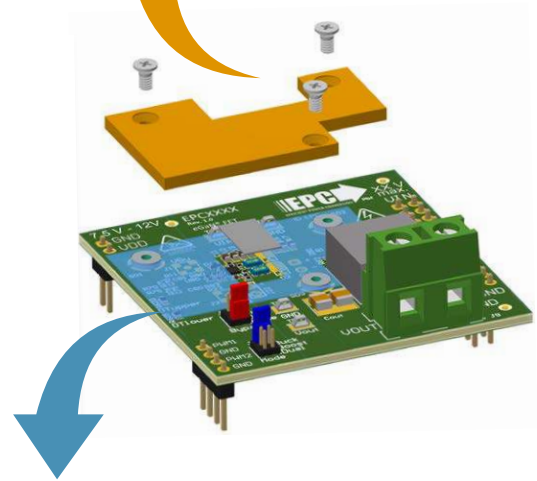


Figure 12: Insulator sheet details with opening for the TIM with location of the FETs

EPC recommends the following thermal interface materials:

| | | |
|---|---|---|
| **t-Global** | P/N: TG-A1780 X 0.5 mm | (highest conductivity of 17.8 W/m·K) |
| **t-Global** | P/N: TG-A6200 X 0.5 mm | (moderate conductivity of 6.2 W/m·K) |
| **Bergquist** | P/N: GP5000-0.02 | (~0.5 mm with conductivity of 5 W/m·K) |
| **Bergquist** | P/N: GPTGP7000ULM-0.020 | (conductivity of 7 W/m·K) |

**NOTE**. The EPC90141 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult:
D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

**Table 2: Bill of Materials**

| Item | Qty | Reference | Part Description | Manufacturer | Part Number |
|---|---|---|---|---|---|
| 1 | 3 | C11, C100, C101 | CAP CER 1 µF 25V X7R 0603 | TDK | C1608X7R1E105K080AB |
| 2 | 9 | C60, C61, C81, C610, C611, C612, C614, C615, C616 | CAP CER 0.1 µF 25V X7R 0402 | Yageo | CC0402KRX7R8BB104 |
| 3 | 1 | C62 | CAP CER 0.022 µF 25V X7R 0402 | TDK | C1005X7R1E223K050BB |
| 4 | 1 | C80 | CAP CER 4.7 µF 10 V X5R 0402 | TDK | C1005X5R1A475K050BC |
| 5 | 2 | C601, C602 | CAP CER 47 pF 50 V C0G/NPO 0402 | Yageo | CC0402JRNPO9BN470 |
| 6 | 2 | C620, C625 | CAP CER 100 pF 50 V X7R 0402 | Yageo | CC0402KRX7R9BB101 |
| 7 | 7 | Ci1, Ci2, Ci3, Ci4, Ci5, Ci6, Ci7 | CAP CER 0.22 µF 100 V X7S 0603 | Taiyo Yuden | HMK107C7224KAHTE |
| 8 | 10 | Cm1, Cm2, Cm3, Cm4, Cm5, Cm6, Cm7, Cm8, Cm9, Cm10 | CAP CER 1 µF 100 V X7R 0805 | AVX | 08051C105K4Z2A |
| 9 | 1 | D60 | DIODE ZENER 5.1 V 150 mW 0603 | Bourns | CD0603-Z5V1 |
| 10 | 4 | D61, D63, D620, D625 | DIODE SCHOTTKY 30 V 30 mA SOD523 | Diodes Inc. | SDM03U40-7 |
| 11 | 1 | J3 | Header Male 100 mil 2 row, 12 pos., Thru Vert. | Amphenol | 67997-272HLF |
| 12 | 1 | J9 | 7.62mm 2 pos. Euro Block | Wurth | 691216410002 |
| 13 | 1 | J80 | Header Male 100 mil 1 row, 4 pos., Thru Vert. | Tyco | 4-103185-0-04 |
| 14 | 1 | J90 | Header Male 100 mil 1 row, 2 pos., Thru Vert. | Tyco | 4-103185-0-02 |
| 15 | 2 | J630, J640 | Header Male 50 mil 2 row, 3 pos., Thru Vert. | Sullins | GRPB032VWVN-RC |
| 16 | 1 | JP630 | 50 mil Jumper **Blue** withHandle | Harwin Inc | M50-2030005 |
| 17 | 1 | JP640 | 50 mil Jumper **Red** withHandle | Harwin Inc | M50-2020005 |
| 18 | 2 | Q1, Q2 | 100 V 25 mΩ 1.7A | EPC | EPC2070 |
| 19 | 1 | Q60 | 100 V 3300 mΩ 0.5A | EPC | EPC2038 |
| 20 | 1 | R62 | RES SMD 27 K Ω 5% 1/10 W 0402 | Panasonic | ERJ-2GEJ273X |
| 21 | 1 | R63 | RES 20 Ω 5% 1/16 W 0402 | Stackpole | RMCF0402JT20R0 |
| 22 | 2 | R70, R75 | RES SMD 2.2 Ω 5% 1/10 W 0402 | Panasonic | ERJ-2GEJ2R2X |
| 23 | 11 | R71, R76, R601, R602, R603, R604, R605, R621, R626, R641, R643 | RES SMD 10 K Ω 1% 1/16 W 0402 | Yageo | RC0402FR-0710KL |
| 24 | 1 | R77 | RES 0 Ω JUMPER 1/16 W 0402 | Stackpole | RMCF0402ZT0R00 |
| 25 | 3 | R78, R90, R100 | RES SMD 0 Ω JUMPER 1/10W 0603 | Panasonic | ERJ-3GEY0R00V |
| 26 | 2 | R80, R82 | RES SMD 10 Ω 1% 1/10W 0402 | Panasonic | ERJ-2RKF10R0X |
| 27 | 2 | R81, R83 | RES 2 Ω 5% 1/16 W 0402 | Stackpole | RMCF0402JT2R00 |
| 28 | 2 | R620, R625 | RES SMD 120 Ω 1% 1/10 W 0603 | Yageo | RC0603FR-07120RL |
| 29 | 3 | SO1, SO2, SO3 | Round Standoff Threaded M2x0.4 Steel 0.039" (1.00mm) | Wurth | 9774010243R |
| 30 | 4 | TP1, TP2, TP3, TP4 | HookUP SMD | Keystone | 5015 |
| 31 | 1 | U80 | 80 V Half Bridge eGaN Driver | Upi | uP1966A |
| 32 | 1 | U100 | 5.0 V 250 mA DFN | MicroChip | MCP1703T-5002E/MC |
| 33 | 4 | U610, U611, U612, U614 | Reconfig Logic | Nexperia | 74LVC1G99GT,115 |
| 34 | 2 | U615, U616 | Bi directional SW 5E 5.5 V | Texas Instruments | SN74LVC1G66DBV |

**Table 3: Optional Components**

| Item | Qty | Reference | Part Description | Manufacturer | Part Number |
|---|---|---|---|---|---|
| 1 | 2 | C70, C75 | CAP CER 100 pF 50 V X7R 0402 | Yageo | CC0402KRX7R9BB101 |
| 2 | 1 | Cout | Custom | TBD | TBD |
| 3 | 2 | D1, D2 | DIODE SCHOTTKY 100 V 2 A DO220AA | Vishay | SS2PH10-M3 |
| 4 | 1 | D77 | DIODE SCHOTTKY 40 V 300 mA SOD523 | ST MIcroelectronics | BAT54KFILM |
| 5 | 2 | J1, J2, J32 | MMCX Jack SMD Vert. | Molex | 734152063 |
| 6 | 1 | L1 | Custom | TBD | TBD |
| 7 | 2 | R11, R22 | RES 0 Ω JUMPER 1/16 W 0402 | Stackpole | RMCF0402ZT0R00 |
| 8 | 1 | R60 | RES SMD 4.7 Ω 5% 1/10 W 0402 | Panasonic | ERJ-2GEJ4R7X |

## Logic Supply
### 12 VDC

J90
Vdd12
2
1
100 mil TH
GND

## 5 V Logic Regulator

V1
AP1006_Rev2_01_12Vto5VlinPSU.SCHDOC
Vdd12
VCC
GND
5V
R90
0603
0 Ω 0.1 W
VCC
C11
0603
1 µF 25 V
GND
GND

## Intermediate Capacitors

VIN — Cm1 0805 1 µF 100 V — GND
VIN — Cm2 0805 1 µF 100 V — GND
VIN — Cm3 0805 1 µF 100 V — GND
VIN — Cm4 0805 1 µF 100 V — GND
VIN — Cm5 0805 1 µF 100 V — GND
VIN — Cm6 0805 1 µF 100 V — GND
VIN — Cm7 0805 1 µF 100 V — GND
VIN — Cm8 0805 1 µF 100 V — GND
VIN — Cm9 0805 1 µF 100 V — GND
VIN — Cm10 0805 1 µF 100 V — GND

## Main Supply Input

J3A
1 2
3 4
5 6
7 8
VIN VIN
VIN VIN
VIN VIN
VIN
Bottom Side install
Amphenol
67997-272HLF

Net Class
ClassName: HighVoltageGate

J1
SMD MMCX
EMPTY
R11
0402
0 Ω 1/16 W
EMPTY
VGu
EMPTY
VSW

### Upper Gate

**ATTENTION**
ELECTROSTATIC
SENSITIVE DEVICE

**ATTENTION**
HOT SURFACE

**HIGH VOLTAGE**

**HIGH VOLTAGE**

## Signal Inputs

**ATTENTION**
ELECTROSTATIC
SENSITIVE DEVICE

J80
1
2
3
4
PWM1
PWM2
100 mil TH
GND GND

## Dead-time and Buffers

DT
AP1010_Rev3_02_GeneralDeadtime.SCHDOC
VCC — VCC
PWM1 — In1
PWM2 — In2
Qup
Qlow
GND
GND

## Gate Driver

GD
AP1017_Rev2_01_100VBGA_GateDriverWboot.SCHDOC
VCC — VCC
HIN — PWMH
LIN — PWML
GND
VGuH
VGuL
VSW
VGlH
VGlL
VGl
GND

## Power Stage

PS
EPC2070_Rev1_0_PhaseLeg.SCHDOC
VGu — VGu
VGuH — VGuH
VGuL — VGuL
VSW — VSW
VGlH — VGlH
VGlL — VGlL
VGl — VGl
VIN — VIN
SW
GND
GND

TP2 SMD TP
Keystone5015
VIN

TP4 SMD TP
Keystone5015
VOUT

L1
TBD
EMPTY
VSW
VOUT

TP1 SMD TP
Keystone5015

Cout
TBD
EMPTY

TP3 SMD TP
Keystone5015

GND GND GND

J9
1
2
7.62 mm TH
EMPTY
GNDP

### Sync Buck Output

J3B
9 10
11 12
13 14
15 16
VSW VSW
VSW VSW
VSW VSW
VSW
Bottom Side install

## SW Output

## Lower Gate

R22
0402
0E 1/16 W
EMPTY
VGl
J22
1
2
J2
SMD MMCX
EMPTY
GND GND

## Switch-node

VSW
J32
SMD MMCX
EMPTY
J33
1
2
Hole 100 mil 1 row, 2 pos.
GND GND

Hole 100 mil 1 row, 2 pos.

## GND

J3C
17 18
19 20
21 22
23 24
Bottom Side install
GND GND

## Heatspreader Mount

SO1
Spacer M2 1mm
9774010243R
SO2
Spacer M2 1mm
9774010243R
SO3
Spacer M2 1mm
9774010243R
GND

FD1 FD2 FD3
**PCB Fiducial**

Figure 13: EPC90141 main schematic

VIN

Vin — VIN

GND

GND

**DC Input
70 Vmax.**

VIN
Ci1
220 nF 100 V
0603
GND

VIN
Ci2
220 nF 100 V
0603
GND

VIN
Ci3
220 nF 100 V
0603
GND

VIN
Ci4
220 nF 100 V
0603
GND

VIN
Ci5
220 nF 100 V
0603
GND

VIN
Ci6
220 nF 100 V
0603
GND

VIN
Ci7
220 nF 100 V
0603
GND

**HF Loop Capacitors**

VGu

VGuH    R80
        0402
        1 1/16 W    VGu

VGuL    R81
        0402
        0 Ω 1/16 W

VGl

VGlH    R82
        0402
        1 1/16 W    VGl

VGlL    R83
        0402
        0 Ω 1/16 W

VIN

Q1
EPC2070
100 V 22 mΩ 1.7 A

SW — SW

Q2
EPC2070
100 V 22 mΩ 1.7 A

GND

VIN

D1
SS2PH10-M3
100 V , 2 A
EMPTY

D2
SS2PH10-M3
100 V , 2 A
EMPTY

GND

**Power Stage          Optional Diodes**

Figure 14: Power Stage schematic using the EPC2070

Sync Boot = Install R60 and D77, remove R77
No Sync Boot = Install R77, remove R60 and D77

Default = No Sync Boot

Q60
EPC2038
100 V 3300 mΩ 0.5 A

VBSin

C60
0402
100 nF 25 V

GND

R60
0402
4.7 0.1 W
EMPTY

5VHS1

D60
CD0603-Z5V1
5V 1, 150 mW

VSWN

D61
SDM03U40-7

4.7 V

30 V 30 mA

C61
0402
100 nF 25 V

GND

Gbtst

C62
0402
22 nF 25 V

R62
0402
27 k 0.1 W

R63
0402
20 1/16 W

D63
SDM03U40-7
30 V 30 mA

VGI

**Synchronous Boostrap Power Supply**

D77
BAT54KFILM
40 V 300 mA

VCC    VCC    R78
0603
0 Ω 0.1 W

VBSin

R77
0402
0 Ω 0.1/16 W

4.7 V

GND

GND

4.7 V

C80
0402
4.7 µF 10 V

GND

R70
0402
2.2 0.1 W

PWMH

C70
0402
100 pF 50 V
EMPTY

R71
0402
10 k 1/16 W

GND    GND

U80
uP1966E

C81
0402
100 nF 25 V

5VHS1    VSWN

UVLO    UVLO

Hin

Level
Shift

VGuL    VGuH

VSWN    VSW

Logic

VDD    4.7 V

Lin

VGlow    VGIH
VGIL

GND

GND

**Gate Driver**

R75
0402
2.2 0.1 W

PWML

C75
0402
100 pF 50 V
EMPTY

R76
0402
10 k 1/16 W

GND    GND

Figure 15: Gate Driver schematic

VCC — VCC

GND — GND

JP630
M50-2030005
50 mil

J630
PolQlow      1    2    VCC
PolQup       3    4    VCC
Dual         5    6    VCC
GRPB032VWVN-RC
50 mil TH

**Buck Single Signal**
**Boost Single Signal**
**Dual Signal**

**Dual/Single PWM, Buck, and Boost Mode Selector**

JP640
M50-2020005
50 mil

J640
SWbyp      1    2    VCC
           3    4    VCC
UseDT      5    6    VCC
GRPB032VWVN-RC
50 mil TH

**Full Bypass**
**DT Bypass**
**No Bypass**

**Bypass Mode Select**

In1

R601
0402
10 k 1/16 W

C601
0402
47 pF 50 V

GND    GND

U610
74LVC1G99GT,115
VCC

In1    2
       3
       5
PolQup 6

C610
0402
100 nF 25 V

GND

R603
0402
10 k 1/16 W

GND

7    InBufQup

Polarity 0=Non-invert, 1= Invert

**Signal Polarity and Input Buffers**

R620
0603
120 0.1 W

D620
SDM03U40-7
30 V 30 mA

C620
0402
100 pF 50 V

GND

**Deadtime Upper**
Default = 10 ns

SWbyp    1

U612
74LVC1G99GT,115
VCC

       2
       3
UseDT  5
       6

R621
0402
10 k 1/16 W

GND

7    DTQup

GND

C612
0402
100 nF 25 V

GND

**Output Buffers and Signal Select**

In1
SWbyp

U615
SN74LVC1G66DBV
Bi directional SW 5E 5.5 V
VCC
GND

R641
0402
10 k 1/16 W

GND   GND

C615
0402
100 nF 25 V

GND

Qup

In2

R602
0402
10k 1/16W

C602
0402
47pF 50V

GND    GND

U611
74LVC1G99GT,115
VCC

In1    2
In2    3
Dual   5
PolQlow 6

C611
0402
100 nF 25 V

GND

R605
0402
10 k 1/16 W

R604
0402
10 k 1/16 W

GND    GND

7    InBufQlow

Polarity 0=Non-invert, 1= Invert

R625
0603
120 0.1 W

D625
SDM03U40-7
30 V 30 mA

C625
0402
100 pF 50 V

GND

**Deadtime Lower**
Default = 10 ns

SWbyp    1

U614
74LVC1G99GT,115
VCC

       2
       3
UseDT  5
       6

R626
0402
10 k 1/16 W

GND

7    DTQlow

GND

C614
0402
100 nF 25 V

GND

In2
SWbyp

U616
SN74LVC1G66DBV
Bi directional SW 5E 5.5 V
VCC
GND

R643
0402
10 k 1/16 W

GND   GND

C616
0402
100 nF 25 V

GND

Qlow

Figure 16: Dead-time and Bypass schematic

U100
5.0 V 250 mA DFN
MCP1703T-5002E/MC

VCC

R100
0603
0 Ω 0.1 W

C100
0603
1 µF 25 V

GND

IN    OUT
GND

GND

C101
0603
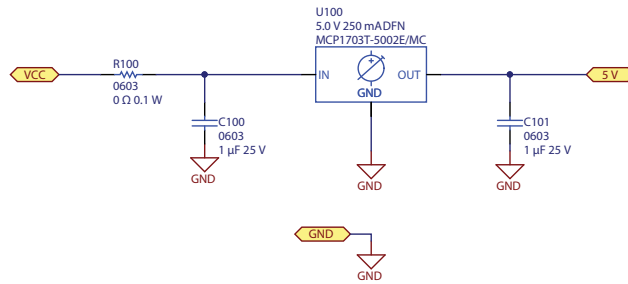1 µF 25 V

5 V

GND

GND

GND

Figure 17:  Logic Supply Regulator schematic

## For More Information:

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