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National Semiconductor

October 2005

LF411JAN
Low Offset, Low Drift JFET Input Operational Amplifier

General Description

This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and guaranteed input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

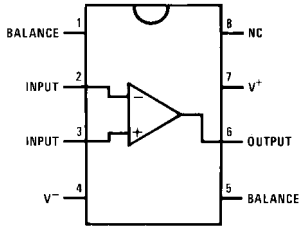
- Internally trimmed offset voltage: 0.5 mV(Typ)
- Input offset voltage drift: 30 µV/°C
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 3 MHz Typ.
- High slew rate: 7V/µs (min.)
- Low supply current: 1.8 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion: A_V = 10, R_L = 10KΩ, $V_O = 20V_{P-P}$, BW = 20Hz - 20KHz <0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 1.5 µs

Ordering Information

NS Part Number	JAN Part Number	NS Package Number	Package Description
JL411BPA	JM38510/11904BPA	J08A	8LD CERDIP

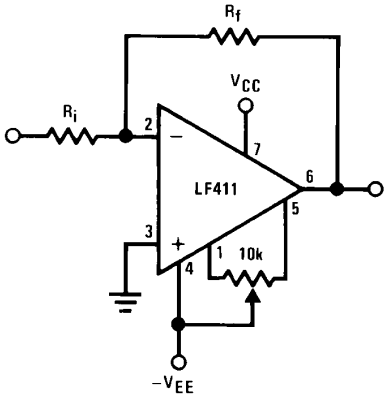
Connection Diagram

8LD Ceramic Dual-in Line Package



Top View
See NS Package Number J08A

Typical Connection



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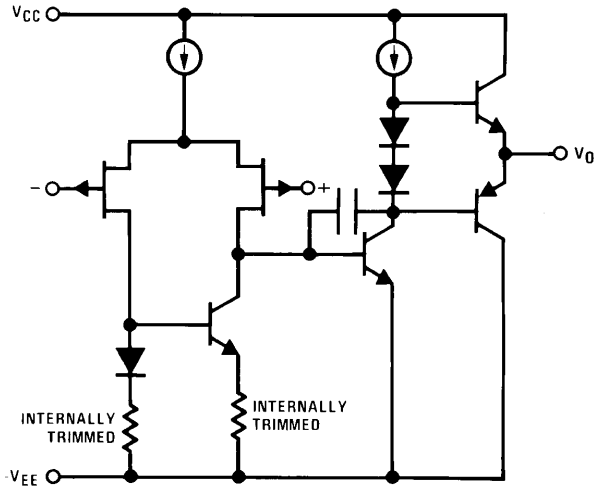
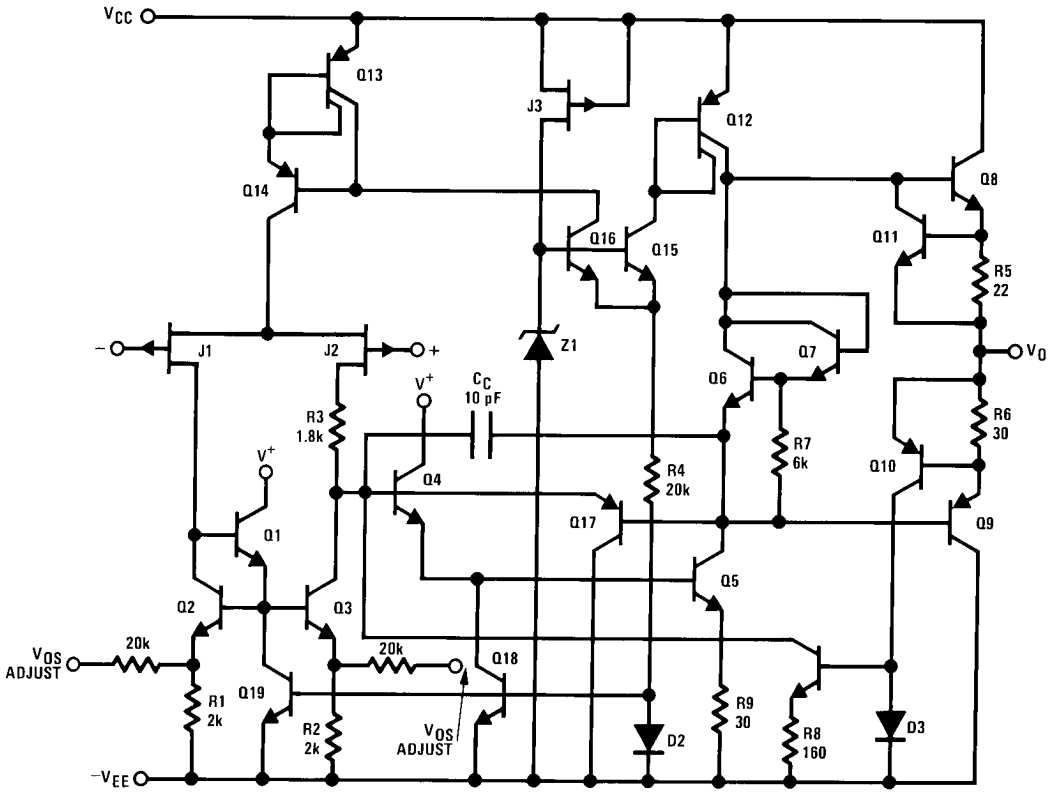
Simplified Schematic



20152406

Detailed Schematic



20152434

Absolute Maximum Ratings (Note 1)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 4)	±15V
Output Short Circuit Duration	Continuous
Power Dissipation (Note 2), (Note 3)	400mW
T_{Jmax}	175˚C
Thermal Resistance	
θ_{JA}	
Still Air	162˚C/W
400LF/Min Air Flow	65˚C/W
θ_{JC}	20˚C/W
Operating Temperature Range	$-55˚C \le T_A \le 125˚C$
Storage Temperature Range	$-65˚C \le T_A \le 150˚C$
Lead Temperature (Soldering, 10 seconds)	300˚C
Package Weight (Typical)	TBD
ESD Tolerance (Note 5)	750V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp ˚C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

Electrical Characteristics

DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V_{CC} = 26V, -V_{CC} = -4V, V_{CM} = -11V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 4V, -V_{CC} = -26V, V_{CM} = 11V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
				-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		±V_{CC} = ±5V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
±I_{IB}	Input Bias Current	+V_{CC} = 26V, -V_{CC} = -4V, V_{CM} = -11V, t ≤ 25mS		-0.4	0.2	nA	1
				-10	50	nA	2
		t ≤ 25mS		-0.2	0.2	nA	1
				-10	50	nA	2
		+V_{CC} = 4V, -V_{CC} = -26V, V_{CM} = 11V, t ≤ 25mS		-0.2	1.2	nA	1
				-10	70	nA	2
I_{IO}	Input Offset Current	t ≤ 25mS		-0.1	0.1	nA	1
				-20	20	nA	2
+PSRR	Power Supply Rejection Ratio	+V_{CC} = 10V to 20V, -V_{CC} = -15V		80		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+V_{CC} = 15V, -V_{CC} = -10V to -20V		80		dB	1, 2, 3
CMR	Input Voltage Common Mode Rejection	V_{CM} = -11V to +11V		80		dB	1, 2, 3
$V_{IO\ Adj}$+	Adjustment for Input Offset Voltage			8.0		mV	1, 2, 3
$V_{IO\ Adj}$-	Adjustment for Input Offset Voltage				-8.0	mV	1, 2, 3
I_{OS}+	Output Short Circuit Current	t ≤ 25mS		-80		mA	1, 2, 3
I_{OS}-	Output Short Circuit Current	t ≤ 25mS			80	mA	1, 2, 3
I_{CC}	Supply Current				3.5	mA	1, 2
					4.0	mA	3
ΔV_{IO} / ΔT	Input Offset Voltage	25˚C ≤ T_A ≤ +125˚C	(Note 6)	-30	30	µV/˚C	2
		-55˚C ≤ T_A ≤ 25˚C	(Note 6)	-30	30	µV/˚C	3
+V_{OP}	Output Voltage Swing	R_L = 10KΩ		12		V	4, 5, 6
		R_L = 2KΩ		10		V	4, 5, 6
-V_{OP}	Output Voltage Swing	R_L = 10KΩ			-12	V	4, 5, 6
		R_L = 2KΩ			-10	V	4, 5, 6
+A_{VS}	Open Loop Voltage Gain	R_L = 2KΩ, V_O = 0 to 10V	(Note 7)	50		K	4
			(Note 7)	25		K	5, 6
-A_{VS}	Open Loop Voltage Gain	R_L = 2KΩ, V_O = 0 to -10V	(Note 7)	50		K	4
			(Note 7)	25		K	5, 6
A_{VS}	Open Loop Voltage Gain	R_L = 10KΩ, V_O = ±2V, ±V_{CC} = ±5V	(Note 7)	20		K	4, 5, 6

Electrical Characteristics (Continued)

AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

AC: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR+	Slew Rate	V_I = -5V to +5V		7.0		V/µS	7
				5.0		V/µS	8A, 8B
SR-	Slew Rate	V_I = +5V to -5V		7.0		V/µS	7
				5.0		V/µS	8A, 8B
TR_{TR}	Transient Response Rise Time	A_V = 1, V_I = 50mV, C_L = 100pF, R_L = 2KΩ			200	nS	7, 8A, 8B
TR_{OS}	Transient Response Overshoot	A_V = 1, V_I = 50mV, C_L = 100pF, R_L = 2KΩ			40	%	7, 8A, 8B
NI_{BB}	Noise Broadband	BW of 10Hz to 15KHz			15	μV_{RMS}	7
NI_{PC}	Noise Popcorn	BW of 10Hz to 15KHz, R_S = 100KΩ			80	μV_{PK}	7
+tS	Settling Time	A_V = 1			1,500	nS	12
-tS	Settling Time	A_V = 1			1,500	nS	12

DC Drift Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±15V, V_{CM} = 0V

Delta Calculations performed at Group B, subgroup 5, Only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current			-0.1	0.1	nA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 4: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

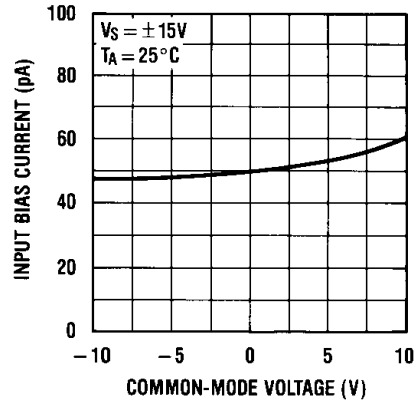
Note 5: Human body model, 100pF discharged through 1.5KΩ.

Note 6: Calculated parameter. For calculation use V_{IO} test at $\pm V_{CC}$ = ±15V

Note 7: Datalog in K = V/mV.

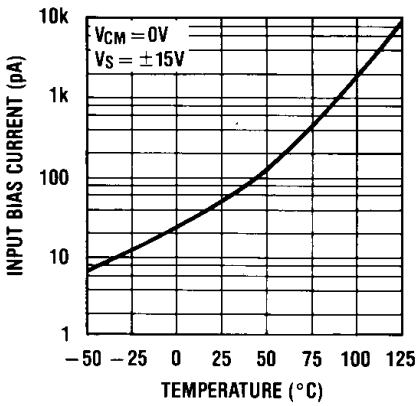
Typical Performance Characteristics

Input Bias Current



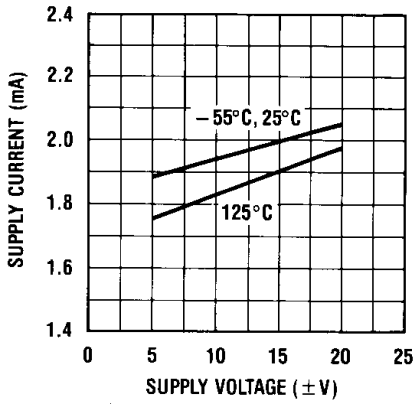
20152411

Input Bias Current



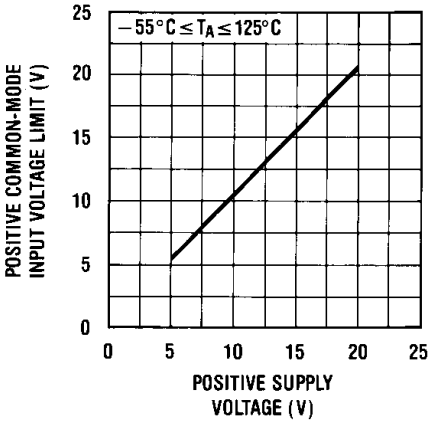
20152412

Supply Current



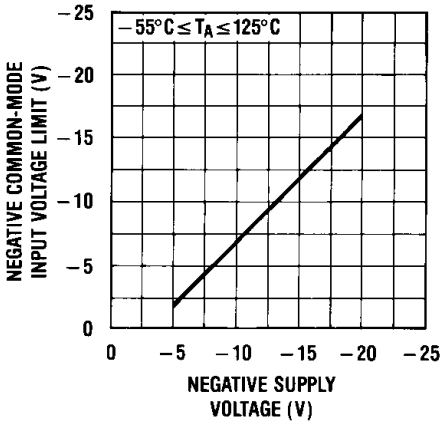
20152413

Positive Common-Mode Input Voltage Limit



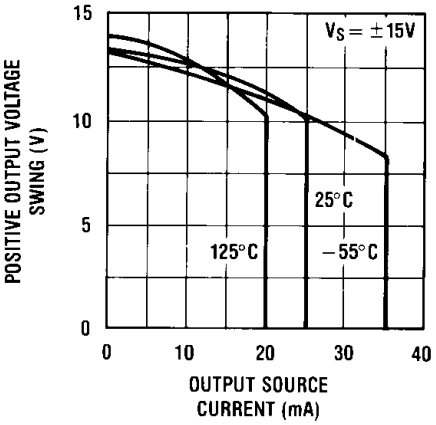
20152414

Negative Common-Mode Input Voltage Limit



20152415

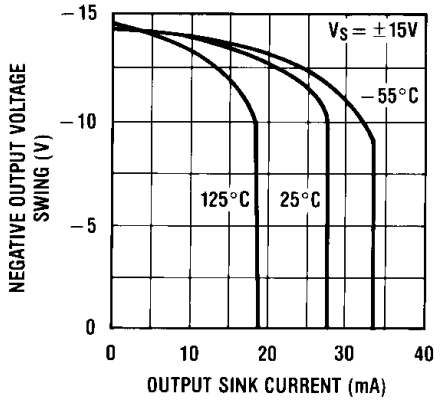
Positive Current Limit



20152416

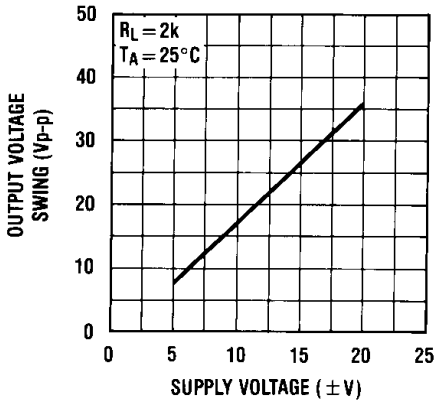
Typical Performance Characteristics (Continued)

Negative Current Limit



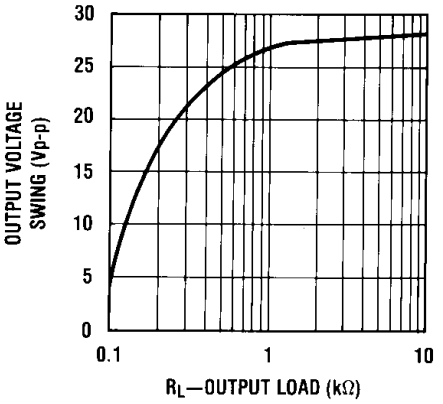
20152417

Output Voltage Swing



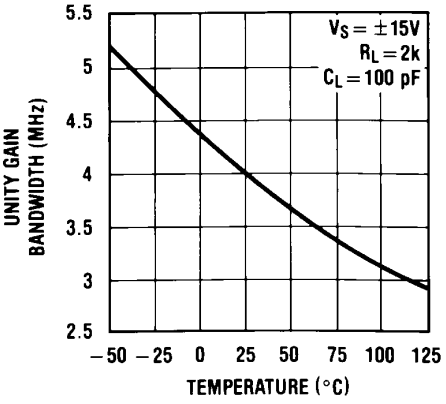
20152418

Output Voltage Swing



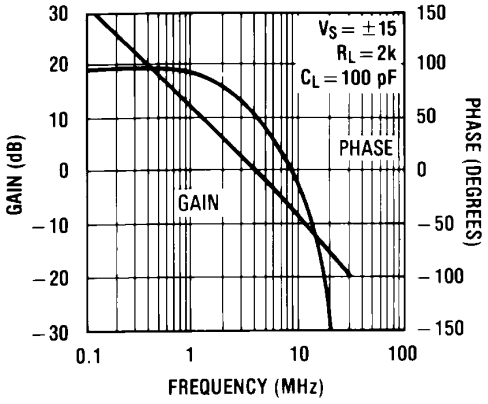
20152419

Gain Bandwidth



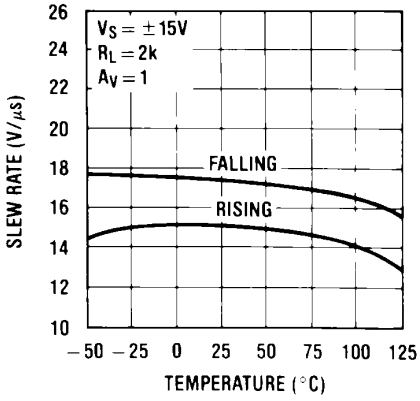
20152420

Bode Plot



20152421

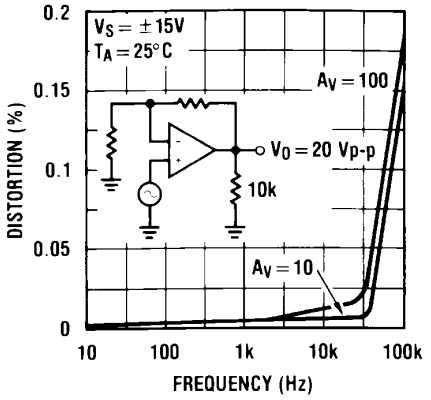
Slew Rate



20152422

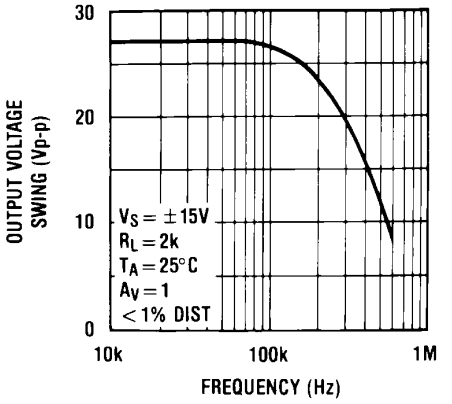
Typical Performance Characteristics (Continued)

Distortion vs Frequency



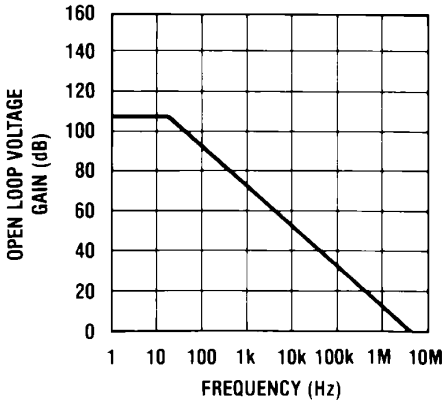
20152423

Undistorted Output Voltage Swing



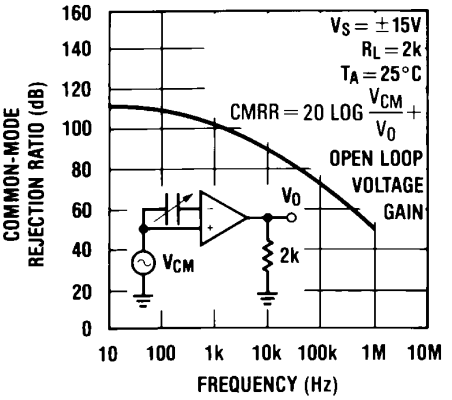
20152424

Open Loop Frequency Response



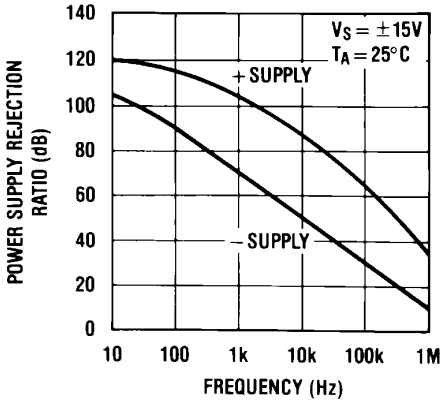
20152425

Common-Mode Rejection Ratio



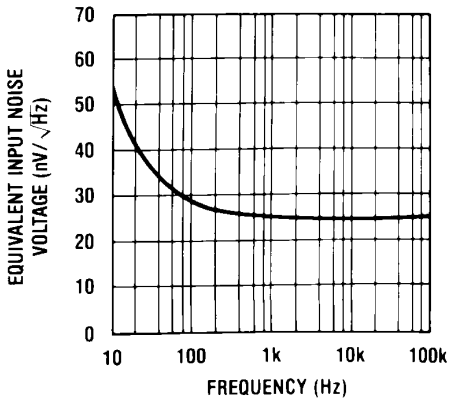
20152426

Power Supply Rejection Ratio



20152427

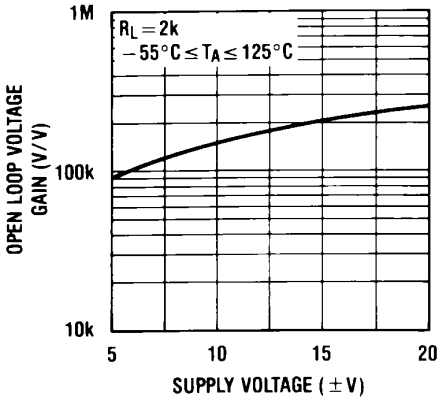
Equivalent Input Noise Voltage



20152428

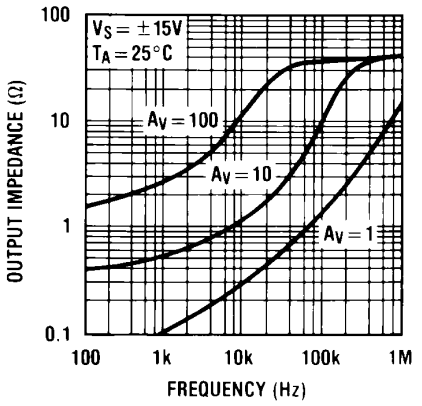
Typical Performance Characteristics (Continued)

Open Loop Voltage Gain



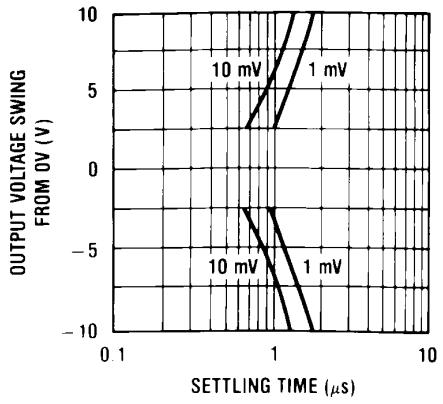
20152429

Output Impedance



20152430

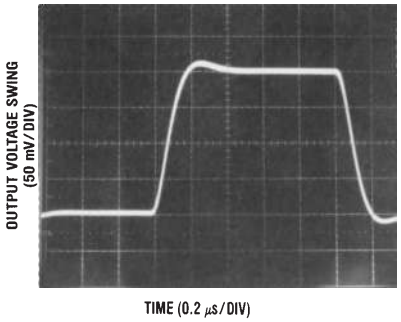
Inverter Settling Time



20152431

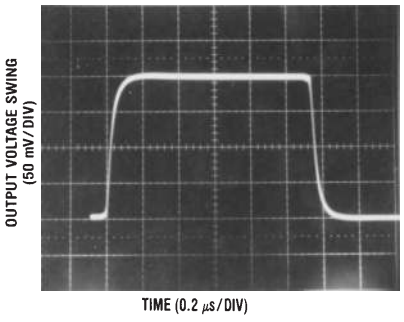
Pulse Response R_L=2 kΩ, C_L10 pF

Small Signal Inverting



20152439

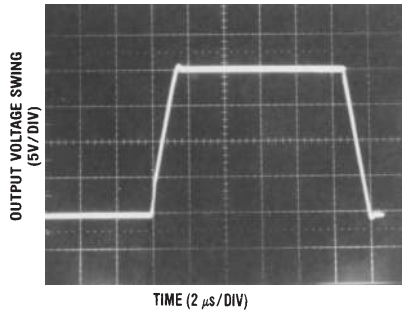
Small Signal Non-Inverting



20152440

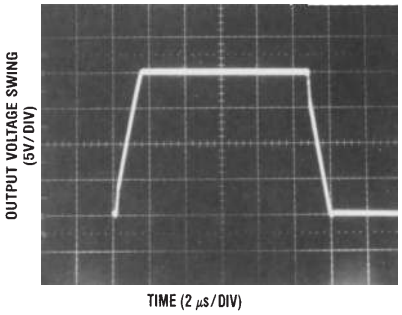
Pulse Response R_L=2 kΩ, C_L10 pF (Continued)

Large Signal Inverting



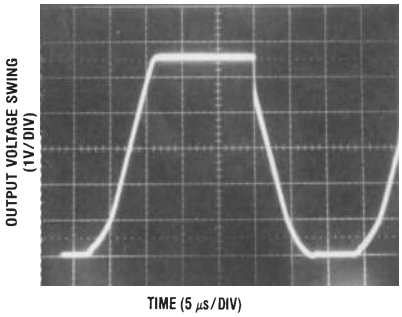
20152441

Large Signal Non-Inverting



20152442

Current Limit (R_L=100Ω)



20152443

Application Hints

The LF411JAN series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

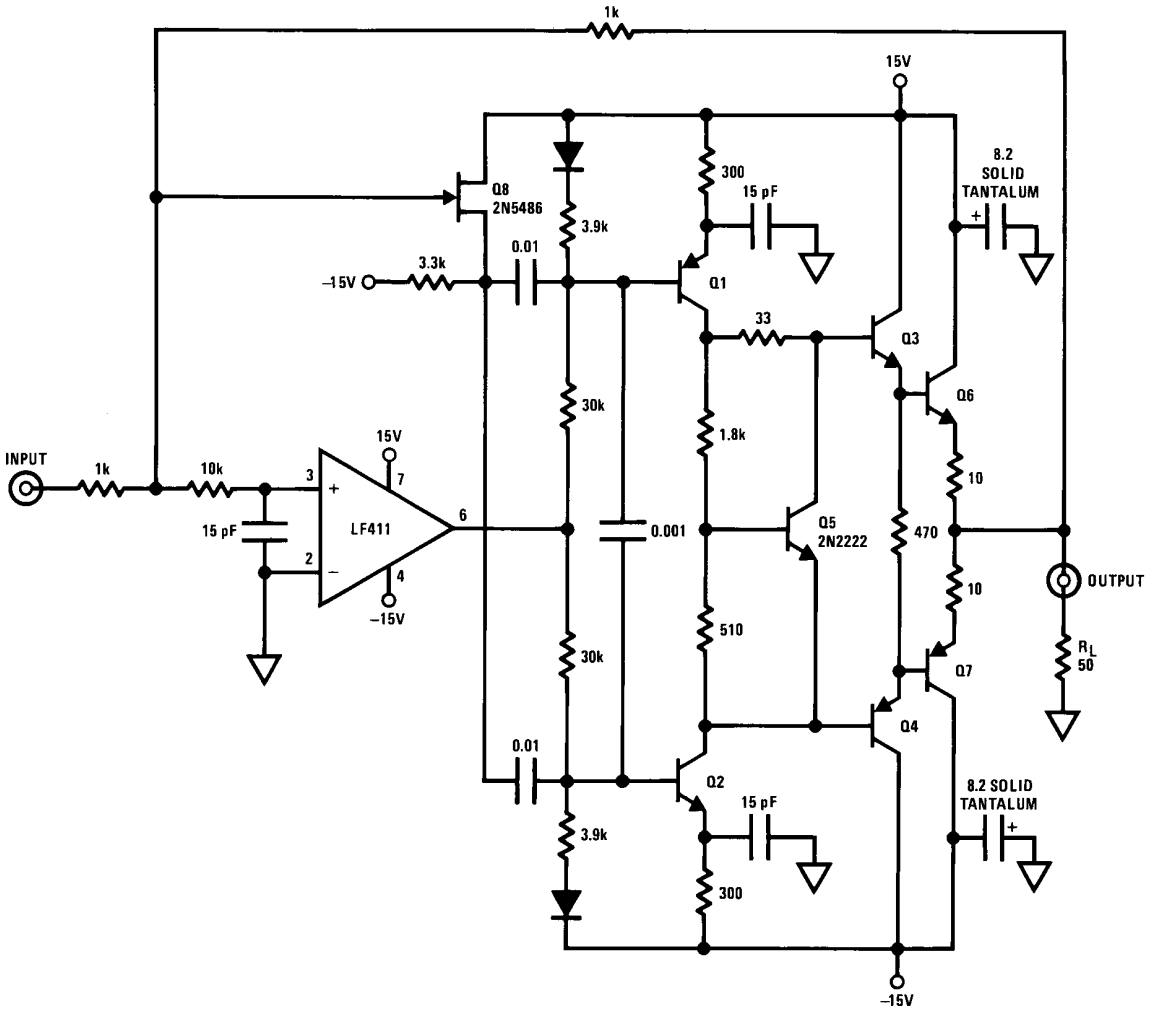
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the ex-

Application Hints (Continued)

pected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster

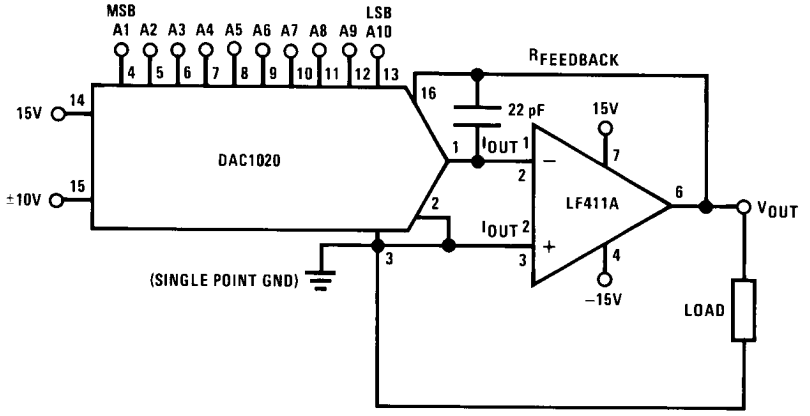


20152409

PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust



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$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

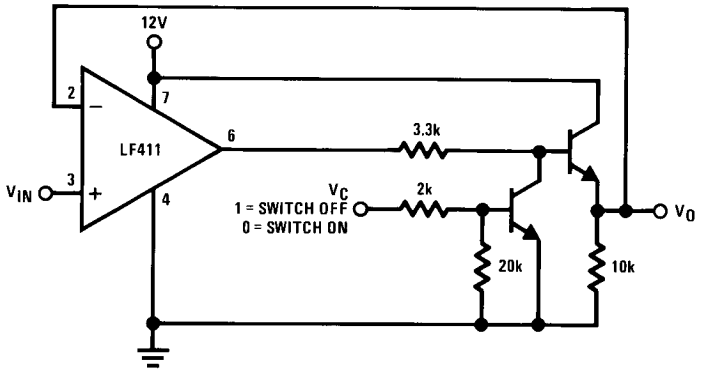
$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$$

where A_N=1 if the A_N digital input is high

A_N=0 if the A_N digital input is low

Single Supply Analog Switch with Buffered Output



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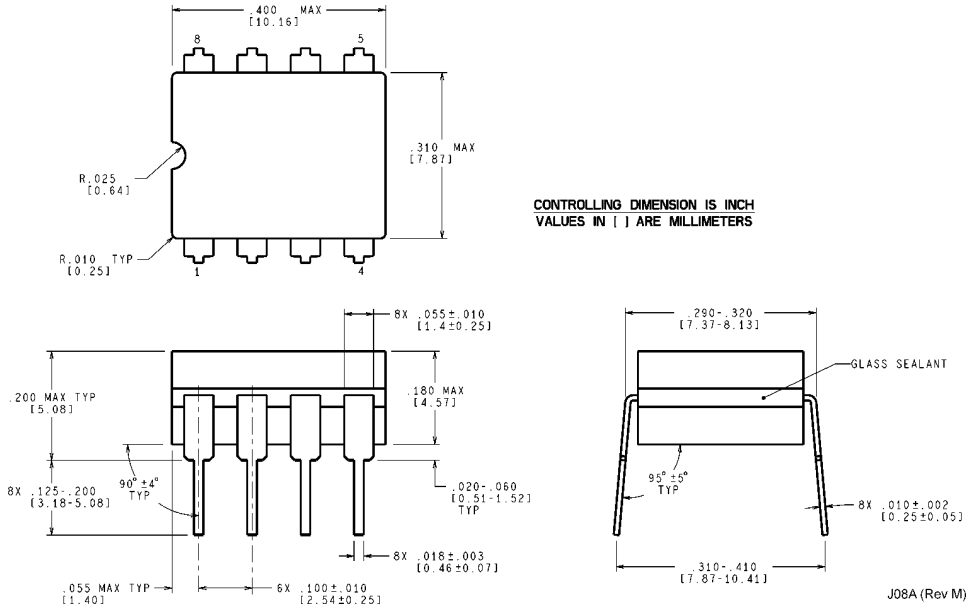
Revision History

Date Released	Revision	Section	Originator	Changes
10/11/05	A	New Release to corporate format	L. Lytle	1 MDS data sheet was converted into the corporate data sheet format. MDS MJLF411-X Rev 0C1 will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted



Ceramic Dual-in-Line Package (J)
NS Package Number J08A

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