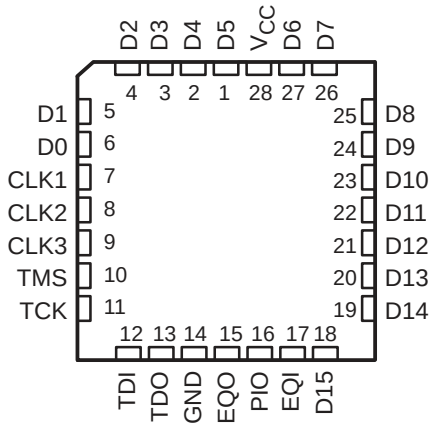
- **Member of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Contains a 1024-Word by 16-Bit Random-Access Memory (RAM) to Store the States of a Digital Bus**
- **Test Operations Are Synchronous to the Test Clock or System Clock(s)**
- **Contains Texas Instruments Event Qualification Module for Real-Time System Test**
- **Eight Protocols for On-Line Signal Monitoring and Test Operations**
- **Inputs Are TTL-Voltage Compatible**
- **Performs Parallel-Signature Analysis (PSA) of Data Inputs With User-Definable Feedback**
- **Data Inputs Are Maskable During PSA Operations**
- **Cascaded PSA Mode Allows Compression of Parallel Data Paths Greater Than 16 Bits in Width**
- **Direct Memory Access (DMA) Speeds Memory and Register File Read/Write Operations**
- **Power-Down Mode When RAM Is Idling Reduces Power Dissipation**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Packaged in 28-Pin Plastic Chip Carriers**

FN PACKAGE
(TOP VIEW)



description

The SN74ACT8994 digital bus monitor (DBM) is a member of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components supports IEEE Standard 1149.1-1990 (JTAG) boundary scan to facilitate testing of complex circuit-board assemblies. The DBM is a boundary-scannable device designed to monitor and/or store the values of a digital bus up to 16 bits in width. It resides in parallel with the bus being monitored.

Data at the D-input pins can be stored in a scannable random-access memory (RAM). Up to 1024 words of 16 bits can be stored. A parallel-signature analysis (PSA) can be performed on the data or on the contents of memory. The PSA operations use a linear-feedback shift-register technique to compress data into a signature. The user can configure the device to mask any combination of data inputs and control the feedback used during PSA operations.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description (continued)

The DBM receives instructions via the IEEE Standard 1149.1-1990 test access port (TAP) interface. The TAP interface consists of test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO) pins.

The DBM can be operated in the off-line mode or the on-line mode. In the off-line mode, the device performs test operations independent of system conditions. Off-line test operations include parallel-signature analysis (PSA) on the contents of RAM and external test.

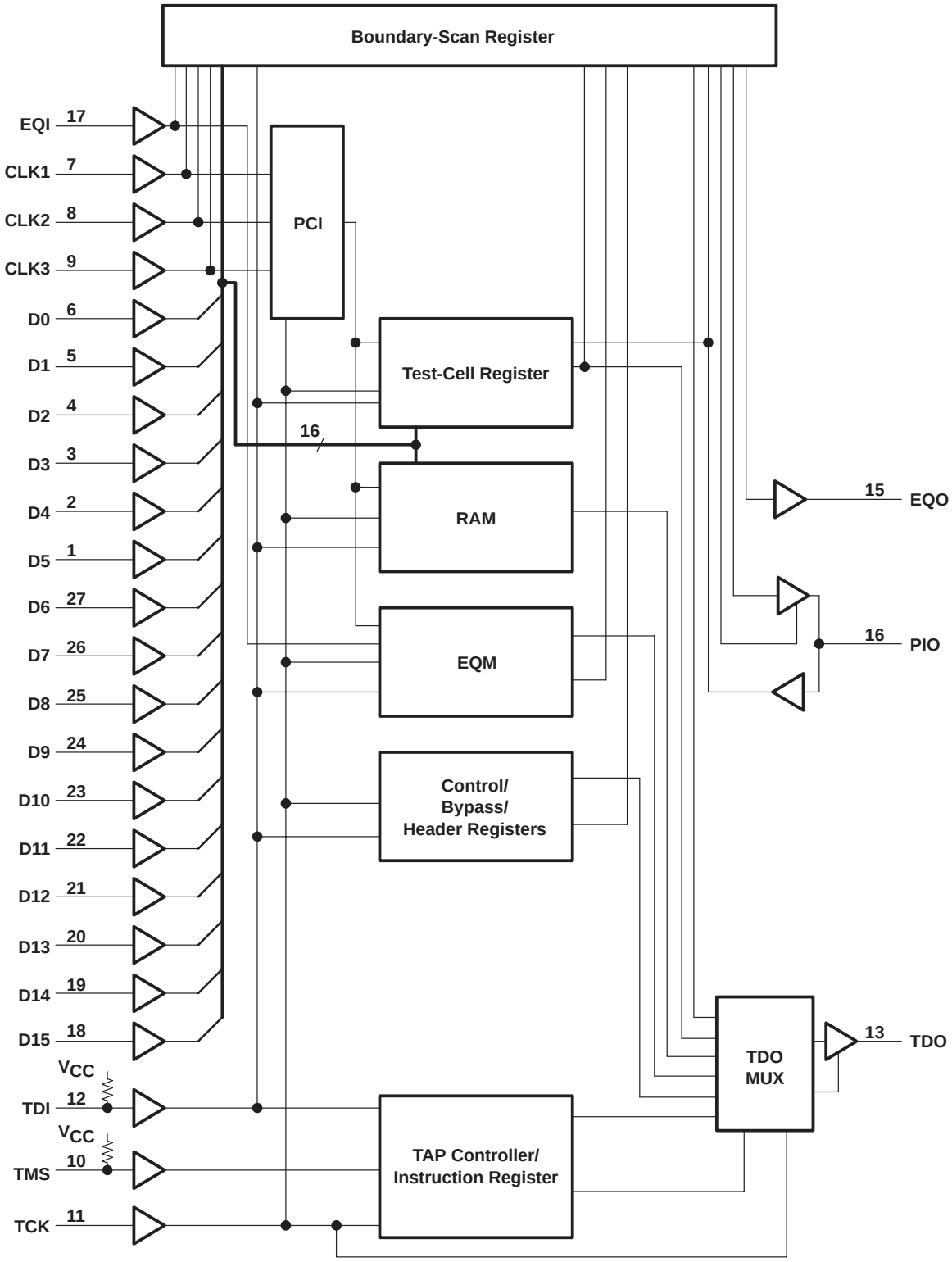
In the on-line mode, the DBM can be configured to perform test operations that are initiated based on system conditions and that operate synchronously to a logical combination of one or more system clocks. The device allows sample, storage, and/or PSA operations to be performed according to one of eight protocols. Compare patterns, which can be stored in the event-qualification module (EQM), allow the user to define specific values of the 16-bit bus for which the test operations are to be performed.

The 1024-word by 16-bit RAM and the EQM register files can be serially accessed using IEEE-Standard-1149.1-1990-compatible read and write instructions. However, direct memory access (DMA) instructions also are provided to speed transfer of large amounts of data to and from the RAM and EQM.

The polynomial input/output (PIO) is a bidirectional pin used to cascade more than one DBM to provide signature analysis on a bus larger than 16 bits.

The SN74ACT8994 is characterized for operation from 0°C to 70°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK1, CLK2, CLK3	7, 8, 9	I	Clock 1, 2, and 3. CLK1−CLK3 provide various types of system clock and control signals to the DBM for the purpose of synchronizing test operations to the system under test.
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15	6, 5, 4, 3, 2, 1, 27, 26, 25 24, 23, 22, 21, 20, 19, 18	I	Data bus inputs. D15−D0 form the 16-bit digital bus that is monitored by the DBM. Data that appears at this bus can be compressed into a 16-bit signature and/or stored in the 1024-word RAM. Each data bit can be individually masked during test operations.
EQI	17	I	Event-qualification input. EQI is used to receive an external (global) event signal from user-defined event-qualification logic. EQI can be configured to initiate test operations in the on-line mode.
EQO	15	O	Event-qualification output. EQO is used to transmit any of several internally generated status signals. EQO can be configured to transmit internal (local) event signals to external (global) event-qualification logic.
GND	14		Ground
PIO	16	I/O	Polynominal input/output. PIO is used to cascade more than one DBM to provide signature analysis on a bus larger than 16 bits. Its configuration as an input or output for a particular DBM device depends on the significance (most, middle, or least) of that DBM in the scan path.
TCK	11	I	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Scan operations of the DBM are synchronous to TCK. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	12	I	Test data input. One of four pins required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	13	O	Test data output. One of four pins required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	10	I	Test mode select. One of four pins required by IEEE standard 1149.1-1990. TMS directs the DBM through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	28		Supply voltage

detailed description

The general architecture of the DBM is shown in the functional block diagram. The DBM contains eight data registers and an instruction register that are accessed serially through the TAP. The TAP controller is a finite-state machine that issues control and enable signals throughout the device, based on its current state. The instruction register (IR) provides additional control signals that are specific to the current instruction. Test data is transmitted serially from TDI through the scan path to TDO. The IR or one of the eight data registers is always selected in the scan path by the TAP control signals issued to the TDO multiplexer.

The 1024-word RAM can be used to store data from the bus being monitored during test operations. The RAM is accessed via the TAP interface when the RAM register (RAMR) is selected in the scan path.

The event-qualification module (EQM) contains two data registers that contain configuration, compare, and mask data associated with on-line test operations. The EQM also contains the state machines for the eight protocols that include various start/stop, start/pause/resume, and do-while algorithms. These protocols operate synchronously to the clock signal generated by the programmable clock interface (PCI). The PCI generates a clock signal from one of 32 different logical combinations of CLK1, CLK2, CLK3, and TCK. The user configures the PCI through the control register (CTLR).

detailed description (continued)

The test-cell register (TCR) is a data register that performs PSA operations on the data bus or on the contents of RAM. During PSA operations, the TCR is a linear-feedback shift register. The CTLR configures the data masking and controls the feedback for PSA operations. The boundary-scan register (BSR), header register (HR), and bypass register (BR) are data registers that can be serially accessed through the TAP interface.

instruction register

The 8-bit instruction register (IR) contains the DBM current instruction, which controls all operations of the device. When the IR is placed in the scan path, the IR status word is loaded into the IR and shifted out on TDO when the new instruction is shifted in.

The IR status word contains four status bits. The $\overline{\text{IRERR}}$ status bit is asserted when an opcode that does not exhibit even parity is loaded into the IR. The OVF status bit is asserted when the RAM address counter is incremented past its maximum value of 3FFh (register value given in hexadecimal format, indicated by the letter h following the value). The RUN and EOT status bits pertain to on-line testing and are asserted when a protocol is active (RUN) or the end of the protocol is reached (EOT).

boundary-scan register

The boundary-scan register (BSR) is a 24-bit register that includes one boundary-scan cell (BSC) for each of the non-JTAG input and output pins of the device, two BSCs for PIO (one for input data and one for output data), and one BSC for the PIO direction signal. The BSR is used to capture the data appearing at the device periphery and to apply test data to the device outputs.

bypass register

The bypass register (BR) is a 1-bit register required by IEEE Standard 1149.1-1990. It provides an abbreviated scan path through the DBM when the current test operations do not require it to access one of the other data registers.

control register

The 45-bit control register (CTLR) issues configuration, control, and enable signals to the device. Data shifted into the CTLR configures the data mask and feedback for PSA operations. It also configures the programmable clock interface and selects the test operations to be performed (see test operations).

event-qualification register 1

Event-qualification register 1 (EQR1) is a 32-bit register that configures the DBM for on-line testing (event-qualified testing). Data shifted into EQR1 selects and controls one of eight event-qualification protocols and configures the event and status signals. The event signal triggers test operations according to the protocol being executed. The status signal is output via EQO. EQR1 also contains the loop counter, which controls the number of times an event-qualification protocol is executed.

event-qualification register 2

Event-qualification register 2 (EQR2) is used to load the event counter, expected data, and mask data (16-word-deep register files) for event-qualified tests. Depending on the current instruction, it is either 48 or 56 bits in length and can be thought of as three 16-bit data segments and two 4-bit address segments. One 4-bit address segment addresses the event counter, while the other 4-bit address segment addresses the expected data and mask data.

The register files can be accessed using IEEE-Standard-1149.1-1990-compatible instructions or DMA instructions. When using IEEE-Standard-1149.1-1990-compatible instructions, EQR2 is configured as a 56-bit register. The data appearing in the 16-bit data segments is loaded into or out of the addresses specified by the register's two 4-bit address segments.

event-qualification register 2 (continued)

During execution of the DMA instructions, EQR2 is configured as a 48-bit register containing only the three 16-bit data segments. Using DMA instructions allows a continuous stream of data to be loaded or unloaded from the register files. After each 48th bit of the data stream has been shifted to or from the register files, the register file addresses are automatically incremented and the first data bit of the next address is shifted.

header register

The header register (HR) is an 8-bit register that initiates DMA write operations on the RAM and on the EQR2 register files. When a DMA write instruction is active, the data being shifted from TDI to TDO is compared against the current value of the HR and the DMA write operation begins after a match is found. When the value of the HR is set to 00h, DMA write operations can only be initiated by the TAP and are not initiated by the TDI-to-TDO data flow.

random-access memory register

The random-access memory register (RAMR) is used to access the 1024-word RAM. Depending on the current instruction, it is either 16 bits or 26 bits in length and can be thought of as a 16-bit data segment and a 10-bit address segment.

The RAMR can be accessed using IEEE-Standard-1149.1-1990-compatible instructions or DMA instructions. When using the IEEE-Standard-1149.1-1990-compatible instructions, RAMR is configured as a 26-bit register. The data appearing in the 16-bit data segment is loaded into or out of the address specified by the register's 10-bit address.

During execution of the DMA instructions, RAMR is configured as a 16-bit register containing only the 16-bit data segment. Using DMA instructions allows a continuous stream of data to be loaded or unloaded from the register. After each 16th bit of the data stream has been shifted to or from the register, the address is automatically incremented and the first data bit of the next address is shifted.

test-cell register

The test-cell register (TCR) is a 16-bit register. It can perform PSA operations on the data inputs or on the contents of RAM. The resulting signature can be scanned out and compared against an expected value. The TCR is also used during test operations to capture the current value of the data bus.

test operations

The primary function of the DBM is to perform test operations while monitoring a digital bus. The test operations can be initiated by system conditions (on-line mode) or independent of system conditions (off-line mode). The description of each of the system test operations follows.

sample

The data at the D inputs is captured in the test-cell register and can be shifted out via TDO for inspection.

parallel-signature analysis

A parallel-signature analysis (PSA) is performed on the data appearing at the D inputs. The test-cell register is configured as a linear-feedback shift register that compresses the data into a signature. The user can configure the device to mask data bits from PSA operations and control the feedback of the linear-feedback shift register. When an input is masked, it is ignored and has no effect on the generated signature.

trace

The data at the D inputs is stored in the RAM. The RAM address is automatically incremented after each write cycle. The device can be configured to clear the RAM address to 000h at the beginning of test execution. It also can be configured to allow write cycles to continue after the maximum address 3FFh is reached (thus clearing the address to 000h and overwriting data).

trace/PSA

The trace and PSA operations are executed simultaneously. All the configuration options for the trace and PSA operations are available for trace/PSA.

In the off-line mode, system test operations are performed via the TAP controller. This is done independent of system conditions.

In the on-line mode, the device is configured to perform system test operations that are dependent on system conditions (event-qualified testing) and synchronous to the system clock(s). Eight different event-qualification protocols offer a wide range of test schemes that control when system test operations take place.

An event can be configured as a match between expected data from the register files and data at the D inputs (local event-qualified testing). Mask data bits from the register files allow any combination of bits to be ignored when the compare takes place. The EQI pin can also be configured as an event to trigger system test operations (global event-qualified testing). The device can be configured to output one of several different status signals via EQO. These are used for global event-qualified testing.

The DBM has instructions that enable the user to perform a self-test on the RAM. This is done by filling the RAM with known values and performing a PSA on its contents. Instructions are included to expedite the loading of the RAM with known values, as well as to perform PSA on the contents of the RAM.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC}
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2) . . . . . 1.1 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	EQO		−4	mA
		PIO, TDO		−16	
I_{OL}	Low-level output current	EQO		4	mA
		PIO, TDO		16	
T_A	Operating free-air temperature		0	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	EQO	V_{CC} = 4.5 V	I_{OH} = −3 mA					V
			I_{OH} = −4 mA			3.7		
		V_{CC} = 5.5 V	I_{OH} = −3 mA					
			I_{OH} = −4 mA			4.7		
	PIO, TDO	V_{CC} = 4.5 V	I_{OH} = −11 mA					
			I_{OH} = −16 mA			3.7		
		V_{CC} = 5.5 V	I_{OH} = −11 mA					
			I_{OH} = −16 mA			4.7		
V_{OL}	EQO	V_{CC} = 4.5 V to 5.5 V	I_{OL} = 3 mA					V
			I_{OL} = 4 mA				0.5	
	PIO, TDO	V_{CC} = 4.5 V to 5.5 V	I_{OL} = 11 mA					
			I_{OL} = 16 mA				0.5	
I_I	CLK, D, EQI, TCK	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND				±1	µA
	TDI, TMS	V_{CC} = 5.5 V,	$V_I = V_{CC}$				±1	
	TDI, TMS	V_{CC} = 5.5 V,	V_I = GND			−0.1	−20	
I_{OZ}‡	PIO, TDO	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or GND				±5	µA
I_{CC}	RAM disabled	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND,	I_O = 0			200	µA
	RAM enabled	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND,	I_O = 0			200	mA
ΔI_{CC}		V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1	mA
C_i		$V_I = V_{CC}$ or GND				4*		pF
C_{io}		$V_O = V_{CC}$ or GND				7*		pF
C_o		$V_O = V_{CC}$ or GND				6*		pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O pins, the parameter I_{OZ} includes the input-leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	Any CLK (except during PSARAM instruction)§	0	50	MHz
		TCK (except during PSARAM instruction)§	0	50	
		Any CLK or TCK (during PSARAM instruction)§	0	17	
t_w	Pulse duration	Any CLK or TCK high or low	7		ns
t_{su}	Setup time	TDI before TCK↑	2		ns
		TMS before TCK↑	4		
		Any D before any CLK or TCK	5		
		EQI before any CLK or TCK	4		
		PIO before any CLK or TCK	1		
t_h	Hold time	TDI after TCK↑	5		ns
		TMS after TCK↑	3		
		Any D after any CLK or TCK	3		
		EQI after any CLK or TCK	2		
		PIO after any CLK or TCK	5		
t_d	Delay time	Power up to TCK↑	100		ns

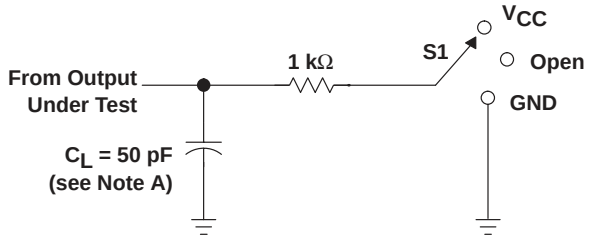
§ The PSARAM instruction performs a parallel-signature analysis on the contents of RAM. This instruction is provided to allow self-test of the RAM.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	Any CLK (except during PSARAM instruction)†		50		MHz
	TCK (except during PSARAM instruction)†		50		
	Any CLK or TCK (during PSARAM instruction)†		17		
t_{PLH}	Any CLK	EQO	7	18	ns
t_{PHL}			7	17	
t_{PLH}	Any CLK	PIO	9	22	ns
t_{PHL}			9	22	
t_{PLH}	Any CLK	TDO	9	20	ns
t_{PHL}			8	19	
t_{PLH}	Any D	EQO	5	17	ns
t_{PHL}			4	15	
t_{PLH}	TCK↓	EQO	5	16	ns
t_{PHL}			5	15	
t_{PLH}	TCK↓	PIO	8	19	ns
t_{PHL}			8	19	
t_{PLH}	TCK↓	TDO	3	12	ns
t_{PHL}			3	11	
t_{PZH}	TCK↓	PIO	5	18	ns
t_{PZL}			5	18	
t_{PZH}	TCK↓	TDO	3	11	ns
t_{PZL}			2	10	
t_{PHZ}	TCK↓	PIO	6	16	ns
t_{PLZ}			5	15	
t_{PHZ}	TCK↓	TDO	9	16	ns
t_{PLZ}			8	15	

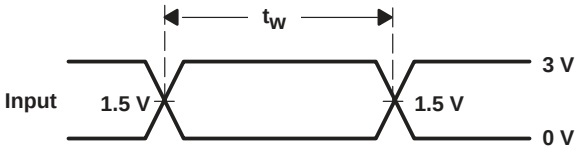
† The PSARAM instruction performs a parallel-signature analysis on the contents of RAM. This instruction is provided to allow self test of the RAM.

PARAMETER MEASUREMENT INFORMATION

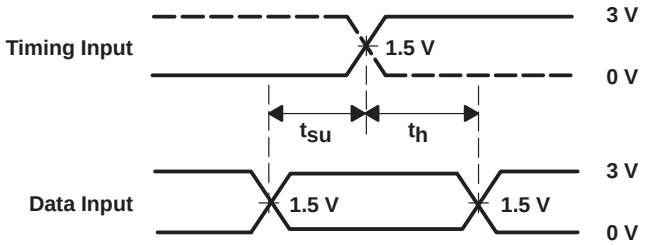


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

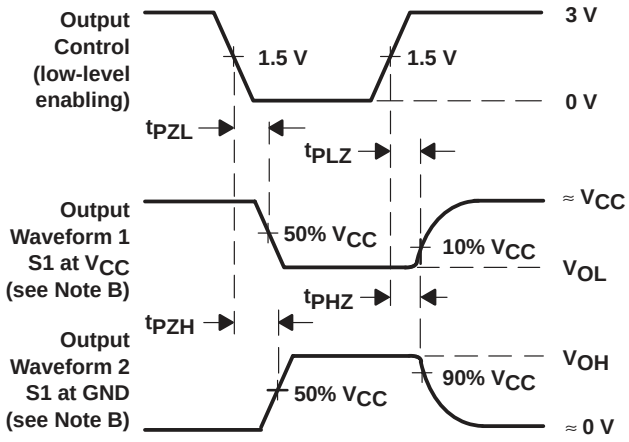
LOAD CIRCUIT



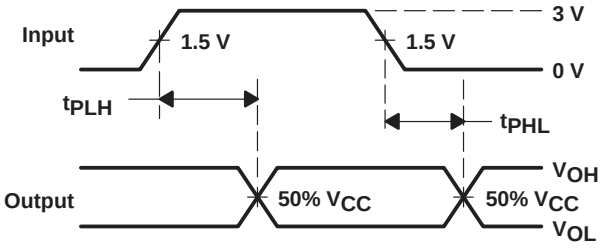
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74ACT8994FN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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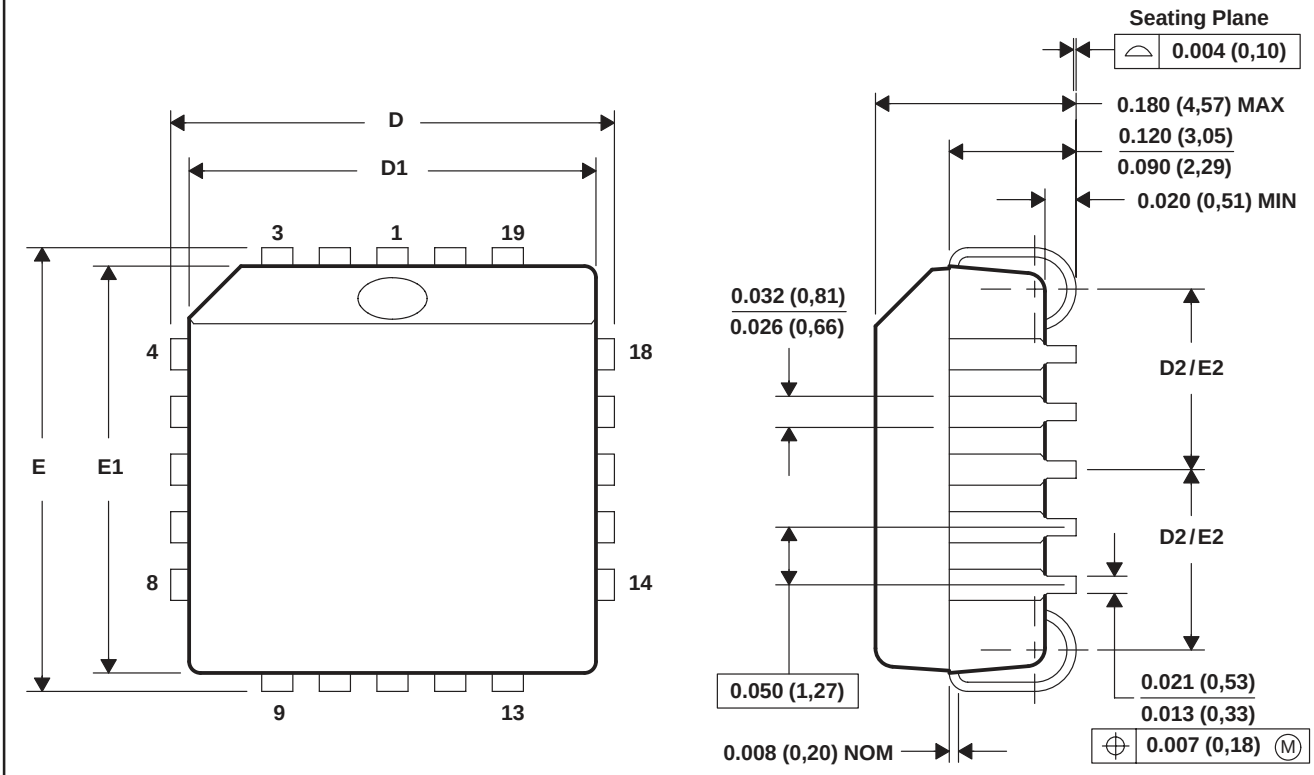
MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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