

Frequency Generator & Integrated Buffers

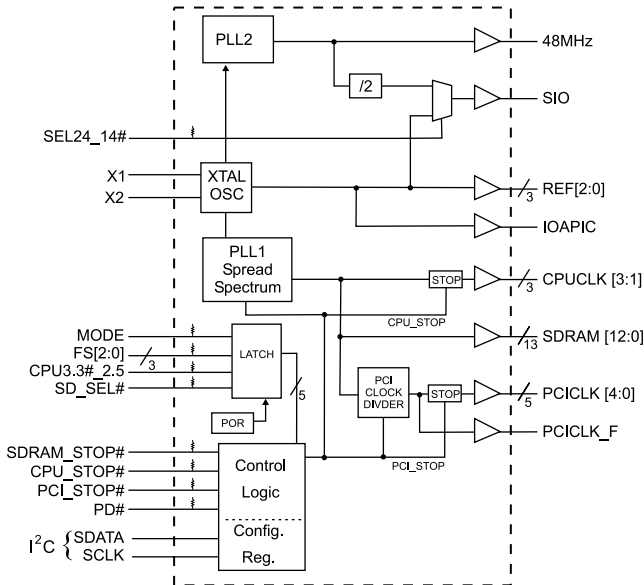
General Description

The **ICS9248-81** is the single chip clock solution for Desktop/ Notebook designs using the SIS style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-81** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I²C interface allows changing functions, stop clock programming and frequency selection. The SD_SEL latched input allows the SDRAM frequency to follow the CPUCLK frequency(SD_SEL=1) or other clock frequencies (SD_SEL=0)

Block Diagram



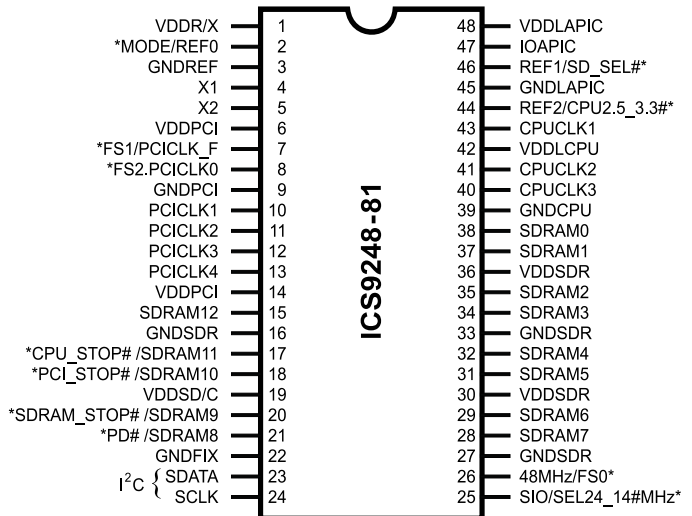
Power Groups

- VDDREF = REF [2:0], X1, X2
- VDDPCI = PCICLK_F, PCICLK [4:0]
- VDDSD/C = SDRAM [11:0], supply for PLL core, 24 MHz, 48MHz
- VDD/CPU = CPUCLK [3:1]
- VDDLAPIC = IOAPIC
- GNDFIX = Ground for fixed clock PLL and output buffers

Features

- Generates the following system clocks:
 - 3 CPU(2.5V/3.3V) up to 133.3MHz.
 - 6 PCI(3.3V) (including 1 free-running)
 - 13 SDRAMs(3.3V) up to 133.3MHz.
 - 3 REF (3.3V) @ 14.318MHz
 - 1 clock @ 24/14.3 MHz selectable output for SIO
 - 1 Fixed clock at 48MHz(3.3V)
 - 1 IOAPIC @ 2.5V/3.3V
- Skew characteristics:
 - CPU – CPU < 175ps
 - SDRAM – SDRAM < 250ps
 - CPU – SDRAM < 500ps
 - CPU(early) – PCI : 1-4ns (typ. 3ns)
 - PCI – PCI < 500ps
- Supports Spread Spectrum modulation ±0.25 & ±0.5% center spread
- Serial I²C interface for Power Management, Frequency Select, Spread Spectrum.
- Efficient Power management scheme through PCI, SDRAM, CPU STOP CLOCKS and PD#.
- Uses external 14.318MHz crystal
- 48 pin 300mil SSOP.

Pin Configuration



48-Pin SSOP

* Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

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Pin Descriptions

| Pin number | Pin name | Type | Description |
|--------------------------------|--------------------------|--------|---|
| 1 | VDDR/X | Power | Isolated 3.3 V power for crystal & reference |
| 2 ^{1,2} | REF0 | Output | 3.3V, 14.318 MHz reference clock output. |
| | Mode | Input | Function select pin, 1=desk top mode, 0=mobile mode. Latched input. |
| 3,9,16,22, 27,33,39 | GND | Power | 3.3 V Ground |
| 4 | X1 | Input | 14.318 MHz crystal input |
| 5 | X2 | Output | 14.318 MHz crystal output |
| 6,14 | VDDPCI | Power | 3.3 V power for the PCI clock outputs |
| 7 ^{1,2} | FS1 | Input | Logic input frequency select bit. Input latched at power-on. |
| | PCICLK_F | Output | 3.3 V free running PCI clock output, will not be stopped by the PCI_STOP# |
| 8 ^{1,2} | PCICLK 0 | Output | 3.3 V PCI clock outputs, generating timing requirements for Pentium II |
| | FS2 | Input | Logic input frequency select bit. Input latched at power-on. |
| 13, 12, 11, 10 | PCICLK [4:1] | Output | 3.3 V PCI clock outputs, generating timing requirements for Pentium II |
| 15,28,29,31,32, 34,35,37,38 | SDRAM 12, SDRAM [7:0] | Output | SDRAM clock outputs. Frequency is selected by SD-Sel latched input. |
| | SDRAM 11 | Output | SDRAM clock outputs. Frequency is selected by SD-Sel latched input. |
| 17 ¹ | CPU_STOP# | Input | Asynchronous active low input pin used to stop the CPUCLK in low state, all other clocks will continue to run. The CPUCLK will have a "Turnon" latency of at least 3 CPU clocks. |
| | SDRAM 10 | Output | SDRAM clock outputs. Frequency is selected by SD-SEL latched input. |
| 18 ¹ | PCI-STOP# | Input | Synchronous active low input used to stop the PCICLK in a low state. It will not effect PCICLK_F or any other outputs. |
| | SDRAM 9 | Output | SDRAM clock outputs. Frequency is selected by SD-Sel latched input. |
| 19 | VDDSD/C | Power | 3.3 V power for SDRAM outputs and core |
| | SDRAM 9 | Output | SDRAM clock outputs. Frequency is selected by SD-Sel latched input. |
| 20 ¹ | SDRAM_STOP# | Input | Asynchronous active low input used to stop the SDRAM in a low state. It will not effect any other outputs. |
| | SDRAM 8 | Output | SDRAM clock outputs. Frequency is selected by SD-Sel latched input. |
| 21 ¹ | PD# | Input | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| | SDATA | Input | Data input for I ² C serial input. |
| 23 | SCLK | Input | Clock input of I ² C input |
| 24 ^{1,2} | SEL24_14# | Input | This input pin controls the frequency of the SIO. If logic 0 at power on SIO=14.318 MHz . If logic 1 at power-on SIO=24MHz. |
| | SIO | Output | Super I/O output. 24 or 14.318 MHz. Selectable at power-up by SEL24_14MHz |
| 26 ^{1,2} | FS0 | Input | Logic input frequency select bit. Input latched at power-on. |
| | 48 MHz | Output | 3.3 V 48 MHz clock output, fixed frequency clock typically used with USB devices |
| 30,36 | VDDSDR | Power | 3.3 V power for SDRAM outputs |
| 40,41,43 | CPUCLK [3:1] | Output | 2.5 V CPU and Host clock outputs |
| 42 | VDDLCPU | Power | 2.5 V power for CPU |
| 44 ^{1,2} | REF2 | Output | 3.3V, 14.318 MHz reference clock output. |
| | CPU3.3#_2.5 | Input | This pin selects the operating voltage for the CPU. If logic 0 at power on CPU=3.3 V and if logic 1 at power on CPU=2.5 V operating voltage. |
| 45 | GNDL | Power | 2.5 V Ground for the IOAPIC or CPU |
| 46 ^{1,2} | REF1 | Output | 3.3V, 14.318 MHz reference clock output. |
| | SD_SEL | Input | This input pin controls the frequency of the SDRAM. |
| 47 | IOAPIC | Output | 2.5V fixed 14.318 MHz IOAPIC clock outputs |
| 48 | VDDLAPIC | Power | 2.5 V power for IOAPIC |

Notes:

- 1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs
- 2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Mode Pin - Power Management Input Control

| MODE, Pin 2 (Latched Input) | Pin 17 | Pin 18 | Pin 20 | Pin 21 |
|--------------------------------|----------------------|----------------------|------------------------|--------------------|
| 0 | CPU_STOP# (INPUT) | PCI_STOP# (INPUT) | SDRAM_STOP# (INPUT) | PD# (INPUT) |
| 1 | SDRAM 11 (OUTPUT) | SDRAM 10 (OUTPUT) | SDRAM9 (OUTPUT) | SDRAM8 (OUTPUT) |

Power Management Functionality

| PD# | CPU_STOP# | PCI_STOP# | SDRAM_STOP | PCICLK (0:4) | SDRAM (0:12) | PCICLK_F | CPUCLK | Crystal OSC | VCO |
|-----|-----------|-----------|------------|-----------------|-----------------|----------------|----------------|----------------|----------------|
| 0 | X | X | X | Stopped Low | Stopped Low | Stopped Low | Stopped Low | Stopped Low | Stopped Low |
| 1 | 1 | 1 | 1 | Running | Running | Running | Running | Running | Running |
| 1 | 1 | 1 | 0 | Running | Stopped Low | Running | Running | Running | Running |
| 1 | 1 | 0 | 1 | Stopped Low | Running | Running | Running | Running | Running |
| 1 | 1 | 0 | 0 | Stopped Low | Stopped Low | Running | Running | Running | Running |
| 1 | 0 | 1 | 1 | Running | Running | Running | Stopped Low | Running | Running |
| 1 | 0 | 1 | 0 | Running | Stopped Low | Running | Stopped Low | Running | Running |
| 1 | 0 | 0 | 1 | Stopped Low | Running | Running | Stopped Low | Running | Running |
| 1 | 0 | 0 | 0 | Stopped Low | Stopped Low | Running | Stopped Low | Running | Running |

CPU 3.3#_2.5V Buffer selector for CPUCLK drivers.

| CPU3.3#_2.5 Input level (Latched Data) | Buffer Selected for operation at: |
|--|--------------------------------------|
| 1 | 2.5V VDD |
| 0 | 3.3V VDD |

Functionality

$V_{DD1, 2, 3, 4} = 3.3V \pm 5\%$, $V_{DDL} = 2.5V \pm 5\%$ or $3.3 \pm 5\%$, $T_A = 0$ to $70^\circ C$
 Crystal (X1, X2) = 14.31818MHz

| SD_SEL | FS2 | FS1 | FS0 | CPU MHZ | SDRAM MHZ | PCI MHZ | REF, IOAPIC MHZ |
|--------|-----|-----|-----|------------|--------------|------------|--------------------|
| 0 | 0 | 0 | 0 | 90.00 | 90.00 | 30.00 | 14.318 |
| 0 | 0 | 0 | 1 | 66.70 | 100.05 | 33.35 | 14.318 |
| 0 | 0 | 1 | 0 | 95.00 | 63.33 | 31.66 | 14.318 |
| 0 | 0 | 1 | 1 | 100.00 | 66.66 | 33.33 | 14.318 |
| 0 | 1 | 0 | 0 | 100.00 | 75.00 | 30.00 | 14.318 |
| 0 | 1 | 0 | 1 | 112.00 | 74.66 | 37.33 | 14.318 |
| 0 | 1 | 1 | 0 | 124.00 | 82.66 | 31.00 | 14.318 |
| 0 | 1 | 1 | 1 | 133.30 | 88.86 | 33.32 | 14.318 |
| 1 | 0 | 0 | 0 | 66.70 | 66.70 | 33.35 | 14.318 |
| 1 | 0 | 0 | 1 | 75.00 | 75.00 | 30.00 | 14.318 |
| 1 | 0 | 1 | 0 | 83.30 | 83.30 | 33.32 | 14.318 |
| 1 | 0 | 1 | 1 | 95.00 | 95.00 | 31.66 | 14.318 |
| 1 | 1 | 0 | 0 | 100.00 | 100.00 | 33.33 | 14.318 |
| 1 | 1 | 0 | 1 | 112.00 | 112.00 | 37.33 | 14.318 |
| 1 | 1 | 1 | 0 | 124.00 | 124.00 | 31.00 | 14.318 |
| 1 | 1 | 1 | 1 | 133.30 | 133.30 | 33.33 | 14.318 |

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

| How to Write: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte 0: Functionality and frequency select register (Default = 0)

| Bit | Description | | | | PWD |
|-----------------|---|--------|--------|--------|----------------|
| Bit 7 | 0 - $\pm 0.25\%$ Center Spread Spectrum | | | | 1 |
| | 1 - $\pm 0.5\%$ Center Spread Spectrum | | | | |
| Bit (2, 6:4) | Bit (2, 6:4) | CPUCLK | SDRAM | PCICLK | XXXX Note 1 |
| | 0000 | 90.00 | 90.00 | 30.00 | |
| | 0001 | 66.70 | 100.05 | 33.35 | |
| | 0010 | 95.00 | 63.33 | 31.66 | |
| | 0011 | 100.00 | 66.66 | 33.33 | |
| | 0100 | 100.00 | 75.00 | 30.00 | |
| | 0101 | 112.00 | 74.66 | 37.33 | |
| | 0110 | 124.00 | 82.66 | 31.00 | |
| | 0111 | 133.30 | 88.86 | 33.32 | |
| | 1000 | 66.70 | 66.70 | 33.35 | |
| | 1001 | 75.00 | 75.00 | 30.00 | |
| | 1010 | 83.30 | 83.30 | 33.32 | |
| | 1011 | 95.00 | 95.00 | 31.66 | |
| | 1100 | 100.00 | 100.00 | 33.33 | |
| | 1101 | 112.00 | 112.00 | 37.33 | |
| | 1110 | 124.00 | 124.00 | 31.00 | |
| 1111 | 133.30 | 133.30 | 33.33 | | |
| Bit 3 | 0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2, 6:4 | | | | 0 |
| Bit 1 | 0 - Normal 1 - Spread spectrum enabled | | | | 1 |
| Bit 0 | 0 - Running 1 - Tristate all outputs | | | | 0 |

Note 1: Default at power-up will be for latched logic inputs to define frequency.

Note 2: PWD = Power-Up Default

Byte 1: CPU, Active/Inactive Register

(1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | 40 | 1 | CPUCLK3 |
| Bit 2 | 41 | 1 | CPUCLK2 |
| Bit 1 | 43 | 1 | CPUCLK1 |
| Bit 0 | - | X | FS0# |

Notes:

- Inactive means outputs are held LOW and are disabled from switching.

Byte 2: PCI Active/Inactive Register

(1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | - | X | FS1# |
| Bit 6 | 7 | 1 | PCICLK_F |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | 13 | 1 | PCICLK4 |
| Bit 3 | 12 | 1 | PCICLK3 |
| Bit 2 | 11 | 1 | PCICLK2 |
| Bit 1 | 10 | 1 | PCICLK1 |
| Bit 0 | 8 | 1 | PCICLK0 |

Notes:

- Inactive means outputs are held LOW and are disabled from switching.

Byte 3: SDRAM Active/Inactive Register

(1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 28 | 1 | SDRAM7 |
| Bit 6 | 29 | 1 | SDRAM6 |
| Bit 5 | 31 | 1 | SDRAM5 |
| Bit 4 | 32 | 1 | SDRAM4 |
| Bit 3 | 34 | 1 | SDRAM3 |
| Bit 2 | 35 | 1 | SDRAM2 |
| Bit 1 | 37 | 1 | SDRAM1 |
| Bit 0 | 38 | 1 | SDRAM0 |

Notes:

- Inactive means outputs are held LOW and are disabled from switching.

Byte 4: SDRAM Active/Inactive Register

(1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | 25 | 1 | 24/14MHz |
| Bit 5 | 26 | 1 | 48MHz |
| Bit 4 | 15 | 1 | SDRAM12 |
| Bit 3 | 17 | 1 | SDRAM11 |
| Bit 2 | 18 | 1 | SDRAM10 |
| Bit 1 | 20 | 1 | SDRAM9 |
| Bit 0 | 21 | 1 | SDRAM8 |

Notes:

- Inactive means outputs are held LOW and are disabled from switching.

Byte 5: Peripheral Active/Inactive
Register (1 = enable, 0 = disable)

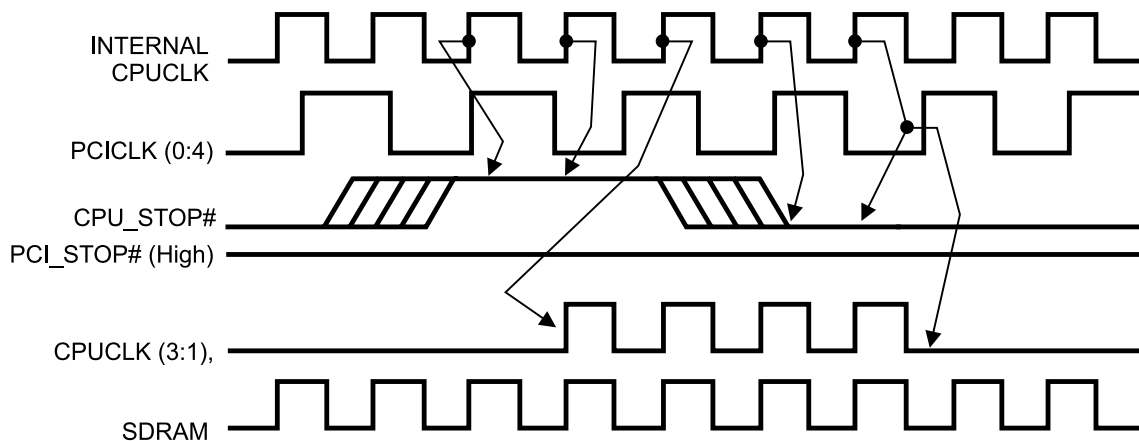
| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | X | FS2# |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | 47 | 1 | IOAPIC |
| Bit 3 | - | X | SD_SEL# |
| Bit 2 | 44 | 1 | REF2 |
| Bit 1 | 46 | 1 | REF1 |
| Bit 0 | 2 | 1 | REF0 |

Notes:

- Inactive means outputs are held LOW and are disabled from switching.

CPU_STOP# Timing Diagram

CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-81**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

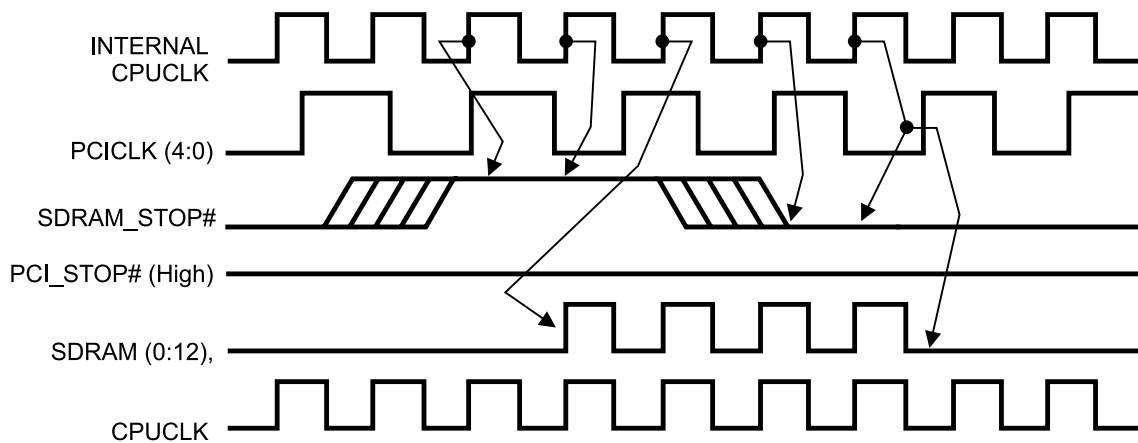


Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-81.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).

SDRAM_STOP# Timing Diagram

SDRAM_STOP# is a synchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. SDRAM_STOP# is synchronized by the ICS9248-81. All other clocks will continue to run while the SDRAM clocks are disabled. The SDRAM clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse.

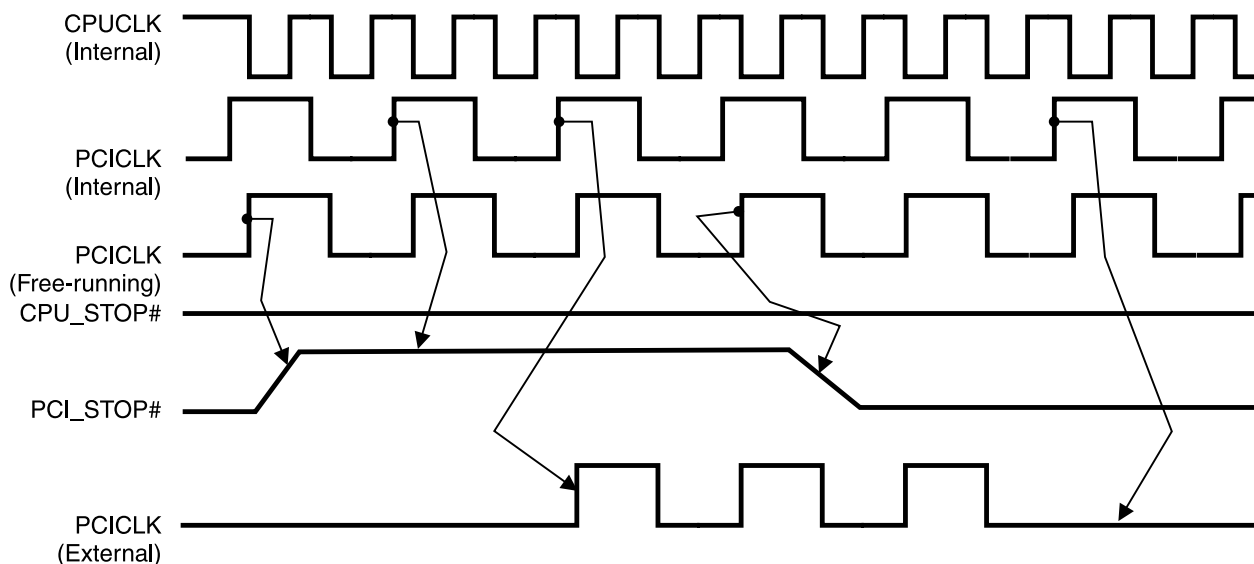


Notes:

1. All timing is referenced to the internal CPU clock.
2. SDRAM is an asynchronous input and metastable conditions may exist. This signal is synchronized to the SDRAM clocks inside the ICS9248-81.
3. All other clocks continue to run undisturbed.

PCI_STOP# Timing Diagram

PCI_STOP# is a synchronous input to the ICS9248-81. It is used to turn off the PCICLK (0:4) clocks for low power operation. PCI_STOP# is synchronized by the ICS9248-81 internally. The minimum that the PCICLK (0:4) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:4) clocks. PCICLK (0:4) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:4) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS9248-81** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper

header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

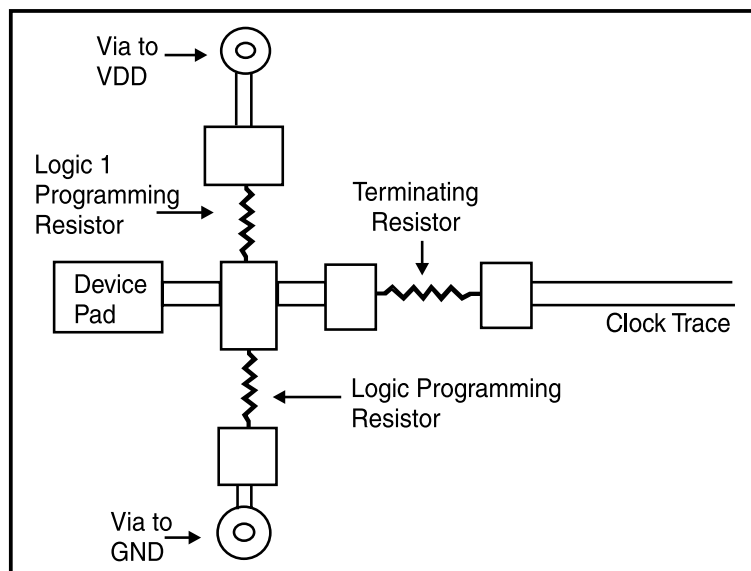


Fig. 1

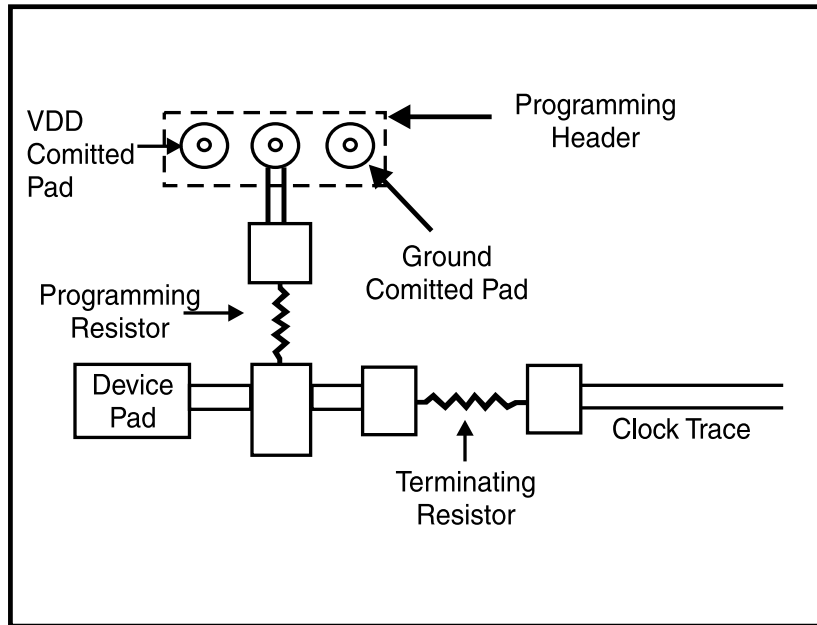


Fig. 2a

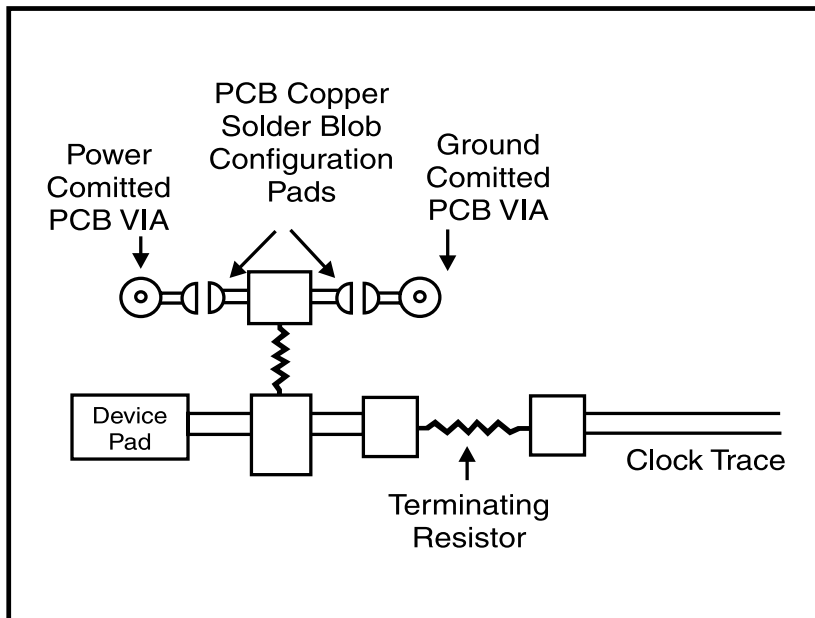


Fig. 2b

Absolute Maximum Ratings

| | |
|-------------------------------|-------------------------------------|
| Supply Voltage | 5.5 V |
| Logic Inputs | GND-0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |
| Case Temperature | 115°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2.0 | | μA |
| Input Low Current | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | -100 | | μA |
| Operating Supply Current | I _{DD3.3OP66} | C _L = 0 pF; Select @ 66MHz | | 60 | 180 | mA |
| | I _{DD3.3OP100} | C _L = 0 pF; Select @ 100MHz | | 66 | 180 | mA |
| Power Down Supply Current | I _{DD3.3PD} | C _L = 0 pF; With input address to V _{DD} or GND | | 70 | 600 | μA |
| Input frequency | F _i | V _{DD} = 3.3 V; | 11 | 14.318 | 16 | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Transition Time ¹ | T _{trans} | To 1st crossing of target Freq. | | | 3 | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |
| Skew ¹ | t _{CPU-SDRAM1} | V _T = 1.5 V | | 200 | 500 | ps |
| | t _{CPU-PCI1} | V _T = 1.5 V | 1 | 3 | 4 | ns |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------------|--|-----|-----|-----|-------|
| Operating Supply Current | I _{DD2.5OP66} | C _L = 0 pF; Select @ 66.8 MHz | | 16 | 72 | mA |
| | I _{DD2.5OP100} | C _L = 0 pF; Select @ 100 MHz | | 23 | 100 | mA |
| Skew ¹ | t _{CPU-SDRAM2} | V _T = 1.5 V; V _{IL} = 1.25 V | | 200 | 500 | ps |
| | t _{CPU-PCI2} | V _T = 1.5 V; V _{IL} = 1.25 V | 1 | 3 | 4 | ns |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$; $C_L = 10 - 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-------------------|--|------|-----|------|-------|
| Output High Voltage | V_{OH1a} | $I_{OH} = -12.0 \text{ mA}$ | 2.4 | 2.6 | | V |
| Output Low Voltage | V_{OL1a} | $I_{OL} = 12 \text{ mA}$ | | 0.2 | 0.4 | V |
| Output High Current | I_{OH1a} | $V_{OH} = 2 \text{ V}$ | | -41 | -19 | mA |
| Output Low Current | I_{OL1a} | $V_{OL} = 0.8 \text{ V}$ | 19 | 37 | | mA |
| Rise Time | t_{r1a}^1 | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | | 1.5 | 2 | ns |
| Fall Time | t_{f1a}^1 | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | | 1.5 | 2 | ns |
| Duty Cycle | d_{t1a}^1 | $V_T = 1.5 \text{ V}$ | 45 | 48 | 55 | % |
| Skew | t_{sk1a}^1 | $V_T = 1.5 \text{ V}$ | | 30 | 175 | ps |
| Jitter, Cycle-to-cycle | $t_{jvc-cyc1a}^1$ | $V_T = 1.5 \text{ V}$ | | 150 | 250 | ps |
| Jitter, One Sigma | t_{j1s1a}^1 | $V_T = 1.5 \text{ V}$ | | 40 | 150 | ps |
| Jitter, Absolute | t_{jabs1a}^1 | $V_T = 1.5 \text{ V}$ | -250 | 140 | +250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 10 - 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-------------------|--|------|------|------|-------|
| Output High Voltage | V_{OH1B} | $I_{OH} = -12.0 \text{ mA}$ | 2 | 2.3 | | V |
| Output Low Voltage | V_{OL1B} | $I_{OL} = 12 \text{ mA}$ | | 0.2 | 0.4 | V |
| Output High Current | I_{OH1B} | $V_{OH} = 1.7 \text{ V}$ | | -41 | -19 | mA |
| Output Low Current | I_{OL1B} | $V_{OL} = 0.7 \text{ V}$ | 19 | 37 | | mA |
| Rise Time | t_{r1B}^1 | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.0 \text{ V}$ | | 1.25 | 1.6 | ns |
| Fall Time | t_{f1B}^1 | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.4 \text{ V}$ | | 1 | 1.6 | ns |
| Duty Cycle | d_{t1B}^1 | $V_T = 1.25 \text{ V}$ | 45 | 48 | 55 | % |
| Skew | t_{sk1B}^1 | $V_T = 1.25 \text{ V}$ | | 30 | 175 | ps |
| Jitter, Cycle-to-cycle | $t_{jvc-cyc1B}^1$ | $V_T = 1.25 \text{ V}$ | | 150 | 250 | ps |
| Jitter, One Sigma | t_{j1s1B}^1 | $V_T = 1.25 \text{ V}$ | | 40 | 150 | ps |
| Jitter, Absolute | t_{jabs1B}^1 | $V_T = 1.25 \text{ V}$ | -250 | 140 | +250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 30 \text{ pF}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|----------------|---|------|-----|-----|-------|
| Output High Voltage | V_{OH2} | $I_{OH} = -11 \text{ mA}$ | 2.4 | 3.1 | | V |
| Output Low Voltage | V_{OL2} | $I_{OL} = 9.4 \text{ mA}$ | | 0.1 | 0.4 | V |
| Output High Current | I_{OH2} | $V_{OH} = 2.0 \text{ V}$ | | -62 | -22 | mA |
| Output Low Current | I_{OL2} | $V_{OL} = 0.8 \text{ V}$ | 16 | 57 | | mA |
| Rise Time ¹ | t_{r2} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | | 1.5 | 2.6 | ns |
| Fall Time ¹ | t_{f2} | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 1.1 | 2 | ns |
| Duty Cycle ¹ | d_{t2} | $V_T = 1.5 \text{ V}$ | 45 | 50 | 55 | % |
| Skew ¹ | t_{sk2} | $V_T = 1.5 \text{ V}$ | | 140 | 500 | ps |
| Jitter, Cycle-to-cycle | $t_{jvc-cvc2}$ | $V_T = 1.25 \text{ V}$ | | 250 | 500 | ps |
| Jitter, One Sigma ¹ | t_{j1s2} | $V_T = 1.5 \text{ V}$ | | 17 | 150 | ps |
| Jitter, Absolute ¹ | t_{jabs2} | $V_T = 1.5 \text{ V}$ | -350 | 70 | 350 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics -SDRAM

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 30 \text{ pF}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|----------------|--|------|-----|-----|-------|
| Output High Voltage | V_{OH3} | $I_{OH} = -11 \text{ mA}$ | 2.4 | 3.1 | | V |
| Output Low Voltage | V_{OL3} | $I_{OL} = 9.4 \text{ mA}$ | | 0.1 | 0.4 | V |
| Output High Current | I_{OH3} | $V_{OH} = 2.0 \text{ V}$ | | -62 | -22 | mA |
| Output Low Current | I_{OL3} | $V_{OL} = 0.8 \text{ V}$ | 16 | 57 | | mA |
| Rise Time ¹ | t_{r3} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | | 1.5 | 2.6 | ns |
| Fall Time ¹ | t_{f3} | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 1.1 | 2.2 | ns |
| Duty Cycle ¹ | d_{t3a} | $V_T = 1.5 \text{ V}$; Divide by 2 selects < 124MHz | 47% | | 57% | |
| | d_{t3b} | $V_T = 1.5 \text{ V}$; Divide by 3 selects | 45 | | 55 | |
| | d_{t3c} | $V_T = 1.5 \text{ V}$; Selects $\geq 124\text{MHz}$ | 43 | 50 | 53 | % |
| Skew ¹ (Window) | t_{sk3a} | $V_T = 1.5 \text{ V}$; SDRAM0,8,9 | | 140 | 250 | ps |
| | t_{sk3b} | $V_T = 1.5 \text{ V}$; All except SDRAM8 and 9 | | 200 | 400 | |
| | t_{sk3c} | $V_T = 1.5 \text{ V}$; All SDRAMs | | 200 | 400 | |
| Jitter, Cycle-to-cycle | $t_{jvc-cvc3}$ | $V_T = 1.25 \text{ V}$ | | 250 | 500 | ps |
| Jitter, One Sigma ¹ | t_{j1s3} | $V_T = 1.5 \text{ V}$ | | 17 | 150 | ps |
| Jitter, Absolute ¹ | t_{jabs3} | $V_T = 1.5 \text{ V}$ | -250 | 70 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF/48MHz/SIO

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------|--|-----|-----|-----|-------|
| Output High Voltage | V_{OH4} | $I_{OH} = -12\text{ mA}$ | 2.4 | 2.6 | | V |
| Output Low Voltage | V_{OL4} | $I_{OL} = 10\text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH4} | $V_{OH} = 2.0\text{ V}$ | | -32 | -22 | mA |
| Output Low Current | I_{OL4} | $V_{OL} = 0.8\text{ V}$ | 16 | 25 | | mA |
| Rise Time ¹ | t_{r4} | $V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$ | | 2 | 4 | ns |
| Fall Time ¹ | t_{f4} | $V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$ | | 1.9 | 4 | ns |
| Duty Cycle ¹ | d_{t4} | $V_T = 1.5\text{ V}$ | 45 | 53 | 55 | % |
| Jitter, One Sigma ¹ | t_{j1s4} | $V_T = 1.5\text{ V}$ | | 500 | 650 | ps |
| Jitter, Absolute ¹ | t_{jabs4} | $V_T = 1.5\text{ V}$ | -1 | | 1 | ns |

¹Guaranteed by design, not 100% tested in production.

General Layout Precautions:

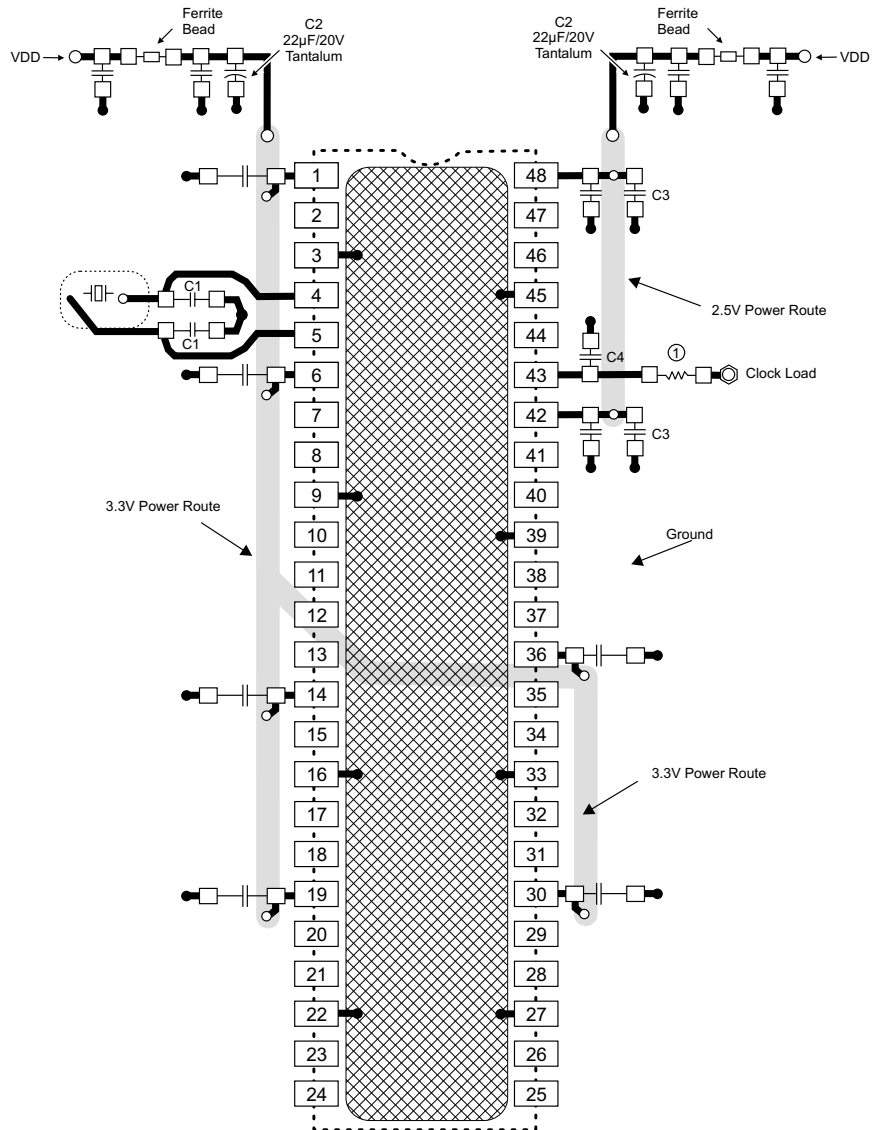
- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and ground traces as wide as the via pad for lower inductance.

Notes:

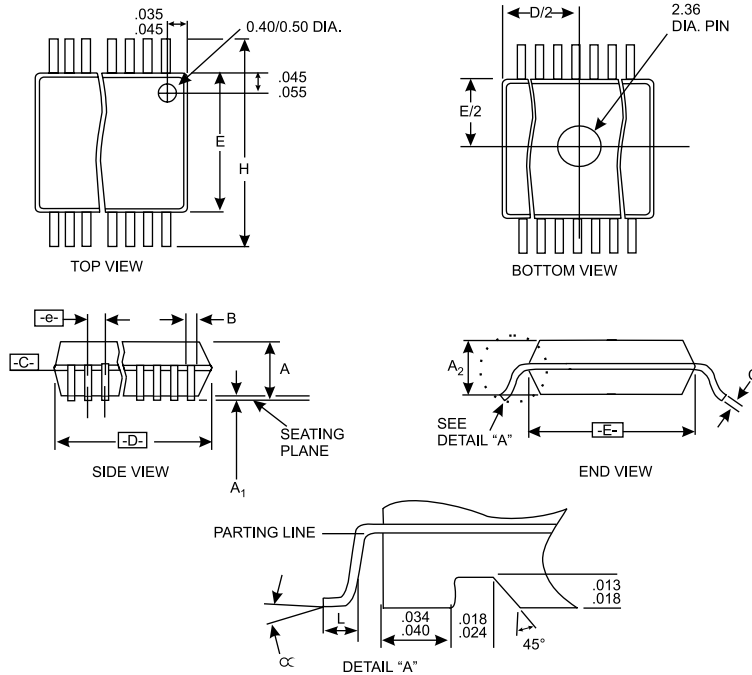
- 1) All clock outputs should have a series terminating resistor, and a 20pF capacitor to ground between the resistor and clock pin. Not shown in all places to improve readability of diagram.
- 2) Optional crystal load capacitors are recommended. They should be included in the layout but not inserted unless needed.

Connections to VDD:

- Best
- Okay
- Avoid
- Avoid



- = Routed Power
- = Ground Connection Key (component side copper)
- = Ground Plane Connection
- = Power Route Connection
- = Solder Pads
- ⊗ = Clock Load



| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | | N |
|--------|-------------------|------|-------|------------|------|------|------|----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .101 | .110 | AC | .620 | .625 | .630 | 48 |
| A1 | .008 | .012 | .016 | | | | | |
| A2 | .088 | .090 | .092 | | | | | |
| B | .008 | .010 | .0135 | | | | | |
| C | .005 | - | .010 | | | | | |
| D | See Variations | | | | | | | |
| E | .292 | .296 | .299 | | | | | |
| e | 0.025 BSC | | | | | | | |
| H | .400 | .406 | .410 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .024 | .032 | .040 | | | | | |
| N | See Variations | | | | | | | |
| ∞ | 0° | 5° | 8° | | | | | |
| X | .085 | .093 | .100 | | | | | |

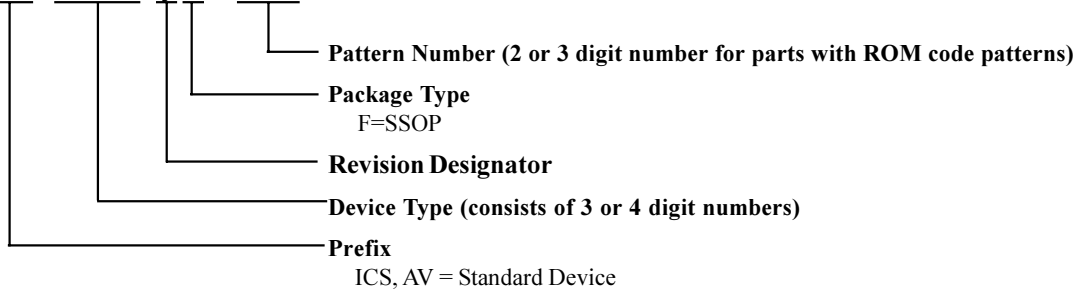
SSOP Package

Ordering Information

ICS9248yF-81

Example:

ICS XXXX y F - PPP



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