



High-Speed CMOS 18-Bit Register

QS74FCT16823T
QS74FCT162823T

ADVANCE
INFORMATION

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <math><1\mu\text{W}</math> typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: $0.5\text{ns } t_{\text{SK(O)}}$
- Flow-through pinout for easy layout
- Power off disable allows hot plugging
- Industrial temperature: -40°C to $+85^{\circ}\text{C}$
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise

FCT16823T

- High drive standard FCT-T outputs:
 $I_{\text{OL}} = +64\text{mA}$, $I_{\text{OH}} = -32\text{mA}$
- Incident switching for driving buses and large loads

FCT162823T

- Balanced output drivers: $\pm 24\text{mA}$
- Reduced switching noise for point to point signals

DESCRIPTION

The FCT16823 family of products are 18-bit registers with three-state outputs that are ideal for driving address and data buses. Two independent 9-bit registers are used with separate controls to permit independent control of data flow in parity-based systems. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for system designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01) and many power and ground pins provide low ground bounce. To accommodate hot-plug or live insertion applications, both versions of this product are designed not to load an active bus when V_{CC} is removed. In applications where bus signals are point-to-point or driving light capacitance loads, the balanced drive FCT162823 is recommended.

Figure 1. Functional Block Diagram

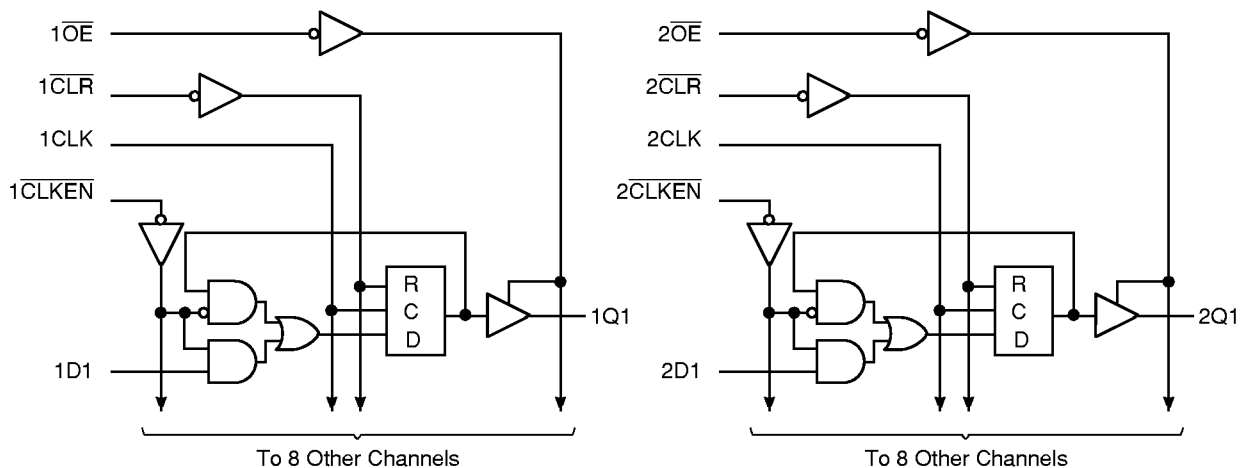


Figure 2. Pin Configuration (All Pins Top View)

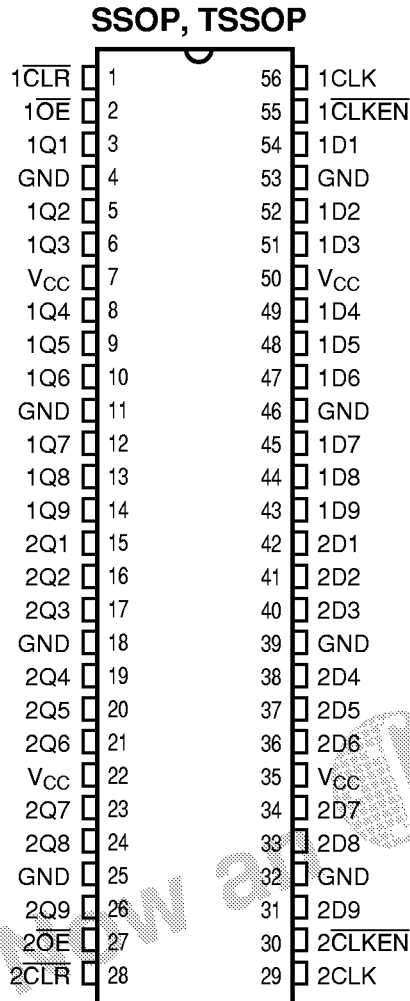


Table 1. Pin Description

Name	I/O	Description
xDx	I	Data Inputs
xQx	O	Data Outputs-Three State
\overline{xOE}	I	Output Enables (Active Low)
xCLK	I	Clock Inputs
\overline{xCLKEN}	I	Clock Enables (Active Low)
\overline{xCLR}	I	Asynchronous Clear

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20mA
DC Output Diode Current with $V_{OUT} < 0$	-50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	1.0W
T_{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 3. Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	Typ	Max	Unit
All	6.0	9.0	pF

Table 4. Function Table

Inputs					Int.	O/P	Function
\overline{OE}	\overline{CLR}	\overline{CLKEN}	Di	CLK	Qi	Yi	
H	X	X	X	X	X	X	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_{OUT}	Voltage Applied to Output or I/O	0	V_{CC}	V
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Temperature	-40	+85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise noted.

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis ⁽⁴⁾	$V_{TLH} - V_{THL}$ for All Inputs	—	100	—	mV
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	1	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{OUT} \leq V_{CC}$	—	—	1	μA
$ I_{OFF} $	Power off leakage ⁽⁵⁾	$V_{CC} = 0V, V_{IN}/V_{OUT} \leq 4.5V$	—	—	1	μA
I_{OS}	Short Circuit Current ^(3,4)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$	-80	-140	-225	mA
I_O	Output Current Drive ⁽³⁾	$V_{CC} = \text{Max.}, V_{OUT} = 2.5V$	-50	—	-180	mA
V_{IK}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V

Notes:

1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values indicate $V_{CC} = 5.0V$ and $T_A = 25^\circ\text{C}$.
3. Not more than one output should be tested at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not tested.
5. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$

Table 7. Output Drive Characteristics for FCT16823T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -3mA	2.5	3.4	—	V
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15mA	2.4	3.2	—	V
			I _{OH} = -32mA ⁽⁴⁾	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64mA	—	0.3	0.55	V

Table 8. Output Drive Characteristics for FCT162823T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit	
I _{ODL}	Output LOW Current ⁽³⁾	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} V _{OUT} = 1.5V	60	115	150	mA	
I _{ODH}	Output HIGH Current ⁽³⁾	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} V _{OUT} = 1.5V	-60	-115	-150	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24mA	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24mA	—	0.3	0.55	V

Notes:

1. For conditions shown as Min. or Max. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
3. Not more than one output should be shorted and the duration is ≤1 second.
4. Duration of the condition should not exceed one second.

Table 9. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽²⁾	Max	Unit	
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$	5	500	μA	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4\text{V}^{(3)}$	0.5	1.5	mA	
Q_{CCD}	Supply Current per Input per MHz ⁽⁴⁾	$V_{CC} = \text{Max.}, \text{Outputs Open One Bit Toggling @ 50\% Duty Cycle } x\overline{\text{DIR}} = x\overline{\text{OE}} = \text{GND}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	75	120	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open One Bit Toggling @ 50\% Duty Cycle } f_I = 5\text{MHz}, f_{CP} = 10\text{MHz (xCLKBA)} x\overline{\text{OE}} = x\overline{\text{CLKEN}} = \text{GND}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	0.8	1.7 ⁽⁵⁾	mA
			$V_{IN} = 3.4\text{ V}$ $V_{IN} = \text{GND}$	1.3	3.2 ⁽⁵⁾	mA
		$V_{CC} = \text{Max.}, \text{Outputs Open Eighteen Bits Toggling @ 50\% Duty Cycle } f_I = 2.5\text{MHz}, f_{CP} = 10\text{MHz (xCLKBA)} x\overline{\text{OE}} = x\overline{\text{CLKEN}} = \text{GND}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	4.2	7.1 ⁽⁵⁾	mA
			$V_{IN} = 3.4\text{ V}$ $V_{IN} = \text{GND}$	9.2	22.1 ⁽⁵⁾	mA

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}, +25^\circ\text{C}$ ambient.
- Per TTL driven Input ($V_{IN} = 3.4\text{V}$). All Other Inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_I N_I)$
 $I_{CCQ} = \text{Quiescent Current (} I_{CCL}, I_{CCH}, \text{ and } I_{CCZ}\text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL-High Input (} V_{IN} = 3.4\text{V)}$
 $D_H = \text{Duty Cycle for TTL High Inputs.}$
 $N_T = \text{Number of TTL High Inputs.}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL).}$
 $f_{CP} = \text{Clock Frequency for Register devices (Zero for Non-Register Devices).}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}\text{.}$
 $f_I = \text{Input Frequency.}$
 $N_I = \text{Number of Inputs at } f_I\text{.}$

Table 10. Switching Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise specified.

Symbol	Parameter ⁽¹⁾	Condition	FCT16823AT		FCT16823BT		FCT16823CT		Unit
			FCT162823AT		FCT162823BT		FCT162823CT		
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCLK to xQX	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C _L = 300pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	
t _{PHL}	Propagation Delay xCLR to xQX	C _L = 50pF R _L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	ns
t _{PZH} t _{PZL}	Output Enable Time xOE to xQX	C _L = 50pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	ns
		C _L = 300pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ xOE to xQX	C _L = 5pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		C _L = 50pF R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	
t _{SU}	Set-up Time HIGH or LOW xDx to xCLK	C _L = 50pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	
t _H	Hold Time HIGH or LOW xDx to xCLK		2.0	—	1.5	—	0.0	—	ns
t _{SU}	Set-up Time HIGH or LOW xCLKEN to xCLK		4.0	—	3.0	—	3.0	—	ns
t _H	Hold Time HIGH or LOW xCLKEN to xCLK		2.0	—	0	—	0	—	ns
t _w	xCLK Pulse Width HIGH or LOW		7.0	—	6.0	—	6.0	—	ns
t _w	xCLR Pulse Width LOW		6.0	—	6.0	—	6.0	—	ns
t _{REM}	Recovery Time xCLR to xCLK		6.0	—	6.0	—	6.0	—	ns
t _{SK(O)}	Output skew ⁽²⁾		—	0.5	—	0.5	—	0.5	ns

Notes:

1. Minimums are guaranteed but not production tested. See test circuit and waveforms.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization.
3. This condition is guaranteed by characterization but not production tested.