

## TMP302-Q1 Automotive Grade, Easy-to-Use, Low-Power, Temperature Switch in MicroPackage

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Low Power:  $15\ \mu\text{A}$  (Maximum)
- SOT563 Package:  $1.6\ \text{mm} \times 1.6\ \text{mm} \times 0.6\ \text{mm}$
- Trip-Point Accuracy:  $\pm 0.2^{\circ}\text{C}$  (Typical) From  $40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Pin-Selectable Trip Points
- Open-Drain Output, Active Low
- Selectable Hysteresis:  $5^{\circ}\text{C}$  or  $10^{\circ}\text{C}$
- Low Supply Voltage Range:  $1.4$  to  $3.6\ \text{V}$

### 2 Applications

- Infotainment
- Climate Control
- Engine Control Unit
- Automotive Black Box
- Central Body Control Module
- Airbag Control Unit
- Thermal Monitoring
- Electronic Protection Systems

### 3 Description

The TMP302-Q1 family of devices is a temperature switch in a micropackage (SOT563). The TMP302-Q1 family of devices offers low power ( $15\ \mu\text{A}$  maximum) and ease-of-use through pin-selectable trip points and hysteresis.

These devices require no additional components for operation; they can function independent of microprocessors or microcontrollers.

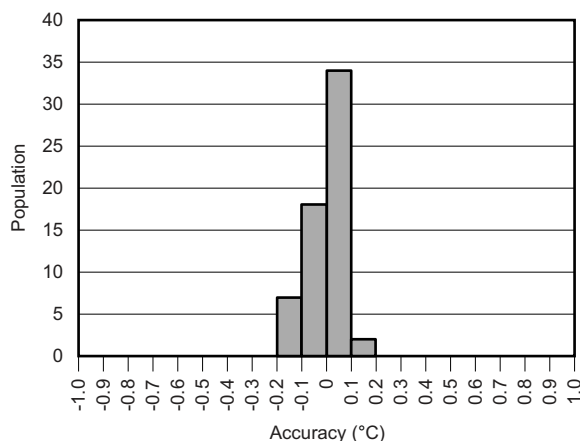
The TMP302-Q1 family of devices is available in several different versions with trip points from  $50^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  in increments of  $5^{\circ}\text{C}$  (see the [Device Comparison Table](#)).

#### Device Information

PART NUMBER	PACKAGE	
TMP302-Q1	SOT563 (6)	$1.60\ \text{mm} \times 1.20\ \text{mm}$

1. For all available packages, see the orderable addendum at the end of the data sheet.

**Trip Threshold Accuracy**



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## 4 Revision History

<b>Changes from Revision B (July 2015) to Revision C</b>	<b>Page</b>
• Changed the supply voltage maximum value from: 3.6 V to: 4 V .....	4
• Changed the input pin supply voltage maximum value from: $V_S + 0.5$ V to: $V_S + 0.3$ and $\leq 4$ V.....	4
• Changed the output pin voltage maximum value from: 3.6 V to: 4 V.....	4
• Added the specified temperature to the <i>Recommended Operating Conditions</i> table .....	4
• Updated junction-to-ambient thermal resistance from 200 to 210.3 .....	4
• Updated junction-to-case (top) thermal resistance from 73.7 to 105.0 .....	4
• Updated junction-to-board thermal resistance from 34.4 to 87.5 .....	4
• Updated junction-to-top characterization parameter from 3.1 to 6.1 .....	4
• Updated junction-to-board characterization parameter from 34.2 to 87.0 .....	4
• Changed the <i>Design Requirements</i> section .....	10
• Added the <i>Receiving Notification of Documentation Updates</i> section .....	12

<b>Changes from Revision A (November 2014) to Revision B</b>	<b>Page</b>
• Changed the <i>Handling Ratings</i> table to <i>ESD Ratings</i> and moved storage temperature to the <i>Absolute Maximum Ratings</i> table .....	4

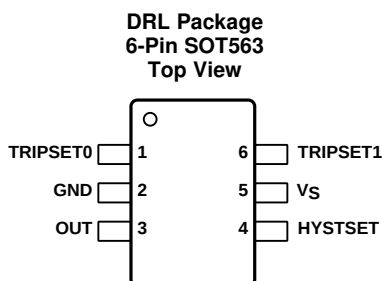
<b>Changes from Original (October 2014) to Revision A</b>	<b>Page</b>
• Changed device status From: Product Preview To: Production.....	1

## 5 Device Comparison Table

DEVICE	SELECTABLE TRIP POINTS (°C) <sup>(1)</sup>
TMP302A-Q1	50, 55, 60, 65
TMP302B-Q1	70, 75, 80, 85
TMP302C-Q1	90, 95, 100, 105
TMP302D-Q1	110, 115, 120, 125

(1) For other available trip points, please contact a TI representative.

## 6 Pin Configuration and Functions



### Pin Functions

NO.	PIN		TYPE	DESCRIPTION
	NAME			
1	TRIPSET0		Digital Input	Used in combination with TRIPSET1 to select the temperature at which the device trips
2	GND		Ground	Ground
3	$\overline{\text{OUT}}$		Digital Output	Open drain, active-low output
4	HYSTSET		Digital Input	Used to set amount of thermal hysteresis
5	$V_S$		Power Supply	Power supply
6	TRIPSET1		Digital Input	Used in combination with TRIPSET0 to select the temperature at which the device trips

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply		4	V
	Input pin (TRIPSET0, TRIPSET1, HYSTSET)	-0.5	$V_S + 0.3$ and $\leq 4$	
	Output pin ( $\overline{\text{OUT}}$ )	-0.5	4	
Current	Output pin ( $\overline{\text{OUT}}$ )		10	mA
Temperature	Operating	-55	130	°C
	Junction		150	
	Storage	-60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{\text{ESD}}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	$\pm 2000$
		Charged device model (CDM), per AEC Q100-011	$\pm 1000$

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_S$	Power supply voltage	1.4	3.3	3.6	V
$R_{\text{pullup}}$	Pullup resistor connected from $\overline{\text{OUT}}$ to $V_S$	10		100	k $\Omega$
$T_A$	Specified temperature	-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMP302-Q1	UNIT
		DRL (SOT563)	
		6 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	210.3	°C/W
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	105.0	°C/W
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	87.5	°C/W
$\Psi_{\text{JT}}$	Junction-to-top characterization parameter	6.1	°C/W
$\Psi_{\text{JB}}$	Junction-to-board characterization parameter	87.0	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

## 7.5 Electrical Characteristics

At  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $V_S = 1.4$  to  $3.6$  V (unless otherwise noted). 100% of all units are production tested at  $T_A = 25^{\circ}\text{C}$ ; overtemperature specifications are specified by design.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TEMPERATURE MEASUREMENT</b>					
Trip point accuracy			$\pm 0.2$	$\pm 2$	$^{\circ}\text{C}$
Trip point accuracy versus supply			$\pm 0.2$	$\pm 0.5$	$^{\circ}\text{C}/\text{V}$
Trip point hysteresis	HYSTSET = GND		5		$^{\circ}\text{C}$
	HYSTSET = $V_S$		10		$^{\circ}\text{C}$
<b>TEMPERATURE TRIP POINT SET</b>					
Temperature trip point set	TRIPSET1 = GND, TRIPSET0 = GND		Default		$^{\circ}\text{C}$
	TRIPSET1 = GND, TRIPSET0 = $V_S$		Default + 5		$^{\circ}\text{C}$
	TRIPSET1 = $V_S$ , TRIPSET0 = GND		Default + 10		$^{\circ}\text{C}$
	TRIPSET1 = $V_S$ , TRIPSET0 = $V_S$		Default + 15		$^{\circ}\text{C}$
<b>HYSTERESIS SET INPUT</b>					
$V_{IH}$ Input logic level high		$0.7 \times V_S$		$V_S$	V
$V_{IL}$ Input logic level low		-0.5		$0.3 \times V_S$	V
$I_I$ Input current	$0 < V_I < 3.6$ V			1	$\mu\text{A}$
<b>DIGITAL OUTPUT</b>					
$V_{OL}$ Output logic level low	$V_S > 2$ V, $I_{OL} = 3$ mA	0		0.4	V
	$V_S < 2$ V, $I_{OL} = 3$ mA	0		$0.2 \times V_S$	V
<b>POWER SUPPLY</b>					
Operating Supply Range		1.4		3.6	V
$I_Q$ Quiescent Current	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		8	15	$\mu\text{A}$
	$V_S = 3.3$ V, $T_A = 50^{\circ}\text{C}$		7		$\mu\text{A}$

## 7.6 Typical Characteristics

At  $T_A = 25^{\circ}\text{C}$  and  $V_S = 3.3$  V, unless otherwise noted.

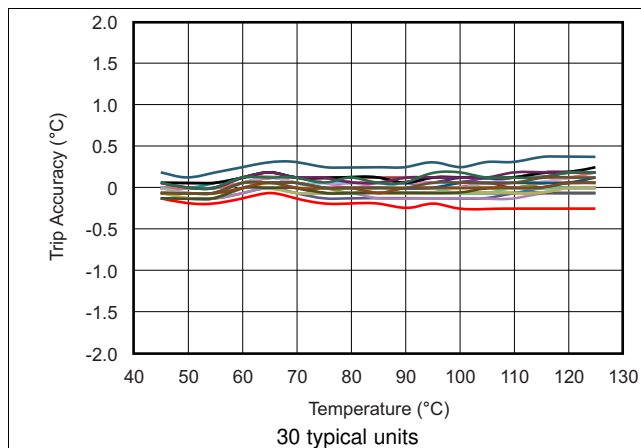


Figure 1. Trip Accuracy Error vs Temperature

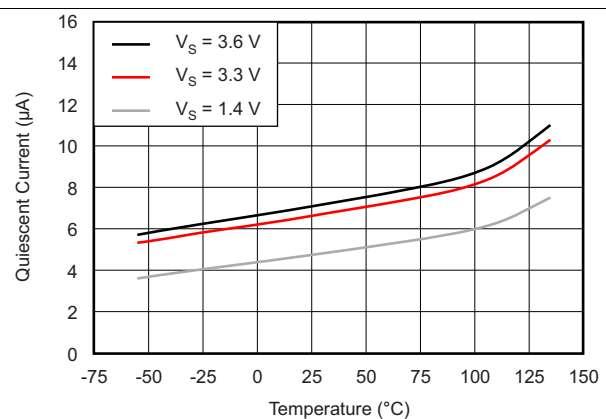


Figure 2. Quiescent Current vs Temperature

### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$  and  $V_S = 3.3\text{ V}$ , unless otherwise noted.

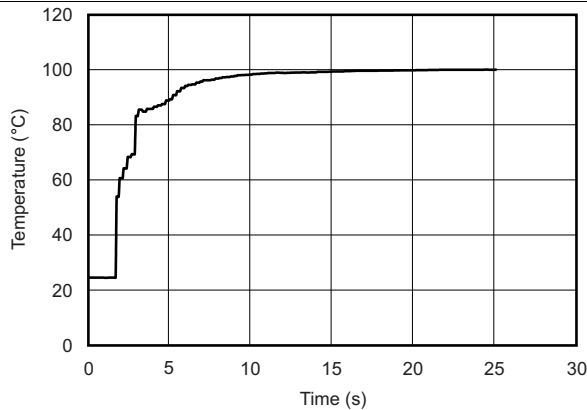


Figure 3. Temperature Step Response in Perfluorinated Fluid at 100°C vs Time

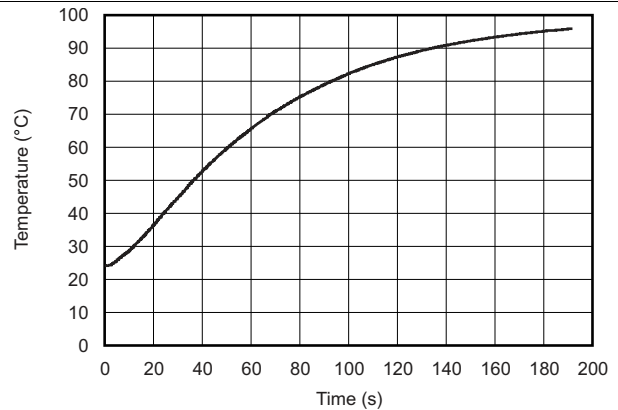


Figure 4. Thermal Step Response in Air at 100°C vs Time

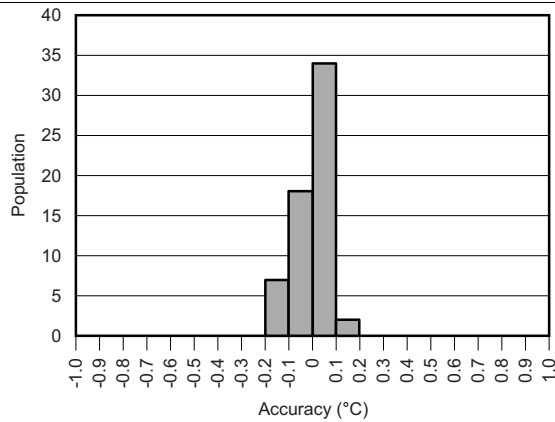


Figure 5. Trip Threshold Accuracy

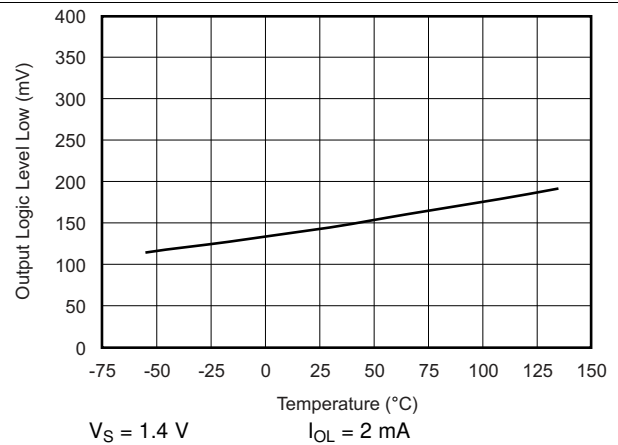


Figure 6. Output Logic-Level Low  $V_{OL}$  vs Temperature

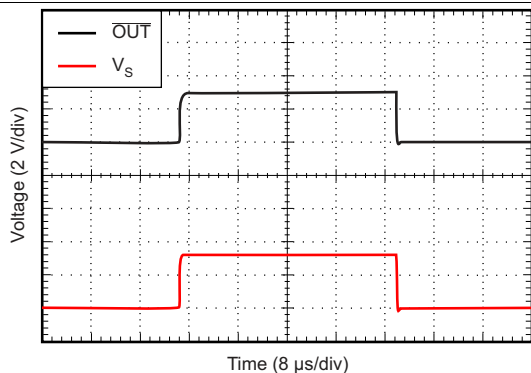
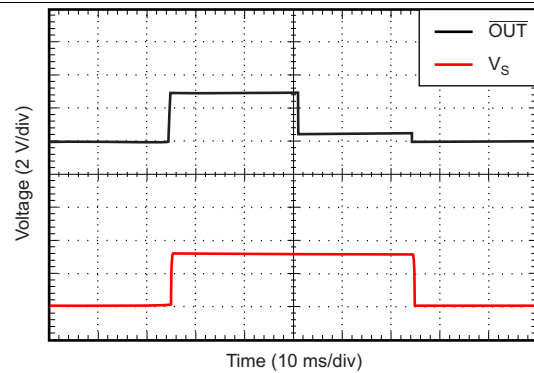


Figure 7. Power-Up and Power-Down Response



TMP302A-Q1,  $T_A = 55^\circ\text{C}$  TRIPSET1 = TRIPSET0 = GND

Figure 8. Power-Up, Trip, and Power-Down Response

## 8 Detailed Description

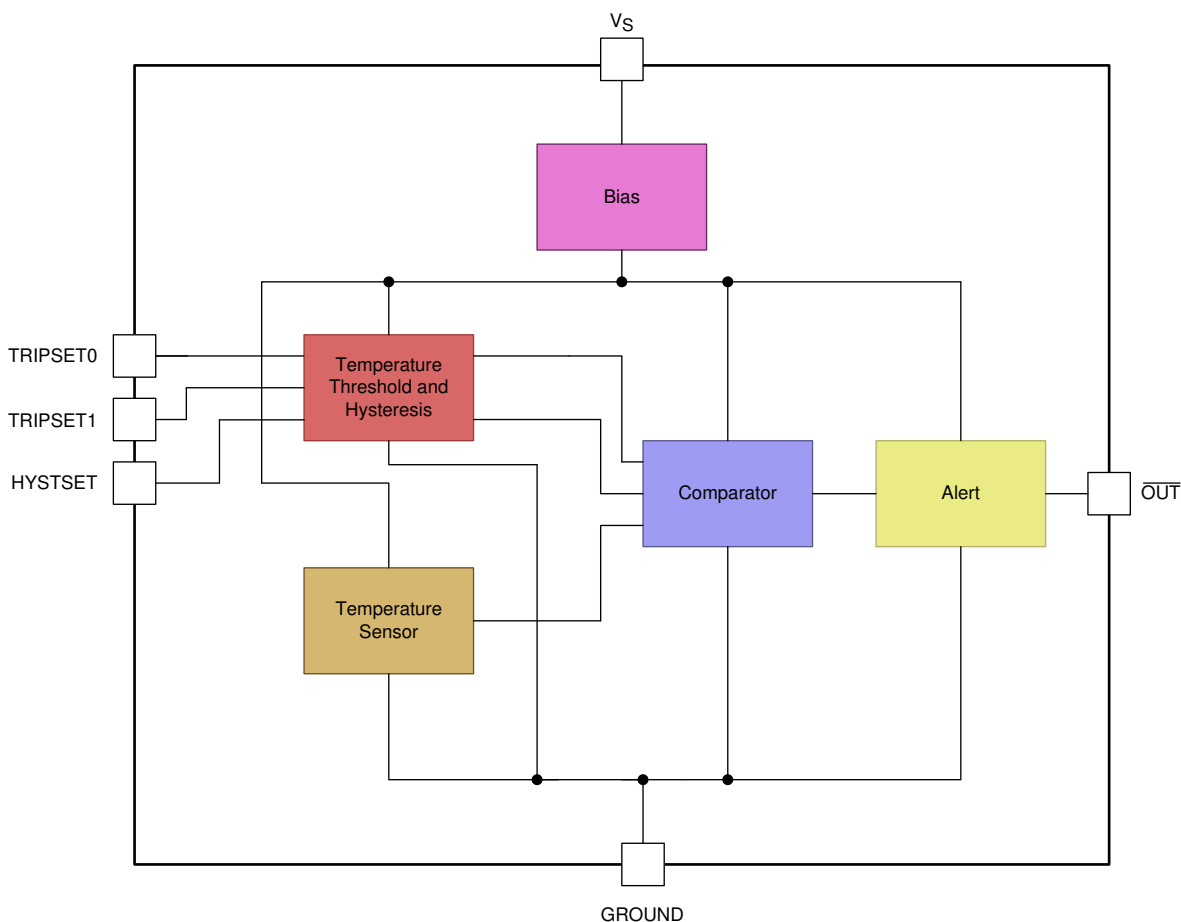
### 8.1 Overview

The TMP302-Q1 temperature switch is optimal for ultra low-power applications that require accurate trip thresholds. A temperature switch is a device that issues an alert response when a temperature threshold is reached or exceeded. The trip thresholds are programmable to four different settings using the TRIPSET1 and TRIPSET0 pins. Table 1 lists the pin settings versus trip points.

**Table 1. Trip Point versus TRIPSET1 and TRIPSET0**

TRIPSET1	TRIPSET0	TMP302A-Q1	TMP302B-Q1	TMP302C-Q1	TMP302D-Q1
GND	GND	50°C	70°C	90°C	110°C
GND	V <sub>S</sub>	55°C	75°C	95°C	115°C
V <sub>S</sub>	GND	60°C	80°C	100°C	120°C
V <sub>S</sub>	V <sub>S</sub>	65°C	85°C	105°C	125°C

### 8.2 Functional Block Diagram



## 8.3 Feature Description

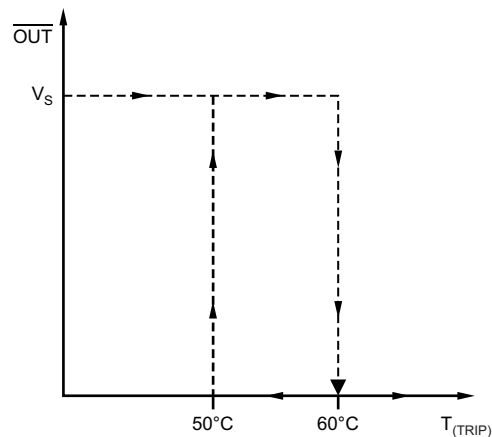
### 8.3.1 HYSTSET

If the temperature trip threshold is crossed, the open-drain, active low output ( $\overline{\text{OUT}}$ ) goes low and does not return to the original high state (that is,  $V_S$ ) until the temperature returns to a value within a hysteresis window set by the HYSTSET pin. The HYSTSET pin allows the user to choose between a 5°C and a 10°C hysteresis window. [Table 2](#) lists the hysteresis window that corresponds to the HYSTSET setting.

**Table 2. HYSTSET Window**

HYSTSET	THRESHOLD HYSTERESIS
GND	5°C
$V_S$	10°C

For the specific case of the device, if the HYSTSET pin is set to 10°C (that is, connected to  $V_S$ ) and the device is configured with a 60°C trip point ( $\text{TRIPSET1} = V_S$ ,  $\text{TRIPSET0} = \text{GND}$ ), when this threshold is exceeded the output does not return to the original high state until it reaches 50°C. This case is more clearly shown in [Figure 9](#).



**Figure 9. TMP302A-Q1: HYSTSET =  $V_S$ , TRIPSET1 =  $V_S$ , TRIPSET0 = GND**

## 8.4 Device Functional Modes

The TMP302-Q1 family of devices has a single functional mode. Normal operation for the TMP302-Q1 family of devices occurs when the power-supply voltage applied between the  $V_S$  pin and GND is within the specified operating range of 1.4 to 3.6 V. The temperature threshold is selected by connecting the TRIPSET0 and TRIPSET1 pins to either the GND or  $V_S$  pins (see [Table 1](#)). Hysteresis is selected by connecting the HYSTSET pin to either the GND or  $V_S$  pins (see [Table 2](#)). The output pin,  $\overline{\text{OUT}}$ , remains high when the temperature is below the selected temperature threshold. The  $\overline{\text{OUT}}$  pin remains low when the temperature is at or above the selected temperature threshold. The  $\overline{\text{OUT}}$  pin returns from a low state back to the high state based upon the amount of selected hysteresis (see the [HYSTSET](#) section).



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Configuring the TMP302-Q1

The TMP302-Q1 family of devices is simple to configure. The only external components that the device requires are a bypass capacitor and pullup resistor. Power-supply bypassing is strongly recommended. Use a 0.1- $\mu$ F capacitor placed as close as possible to the supply pin. To minimize the internal power dissipation of the TMP302-Q1 family of devices, use a pullup resistor value greater than 10 k $\Omega$  from the  $\overline{\text{OUT}}$  pin to the  $V_S$  pin. Refer to Table 1 for trip-point temperature configuration. The TRIPSET pins can be toggled dynamically; however, the voltage of these pins must not exceed  $V_S$ . To ensure a proper logic high, the voltage must not drop below  $0.7 V \times V_S$ .

### 9.2 Typical Application

Figure 10 shows the typical circuit configuration for the TMP302-Q1 family of devices. The TMP302-Q1 family of devices is configured for the default temperature threshold by connecting the TRIPSET0 and TRIPSET1 pins directly to ground. Connecting the HYSTSET pin to ground configures the device for 5°C of hysteresis. Place a 10-k $\Omega$  pullup resistor between the  $\overline{\text{OUT}}$  and  $V_S$  pins. Place a 0.1- $\mu$ F bypass capacitor between the  $V_S$  pin and ground, close to the TMP302-Q1 device.

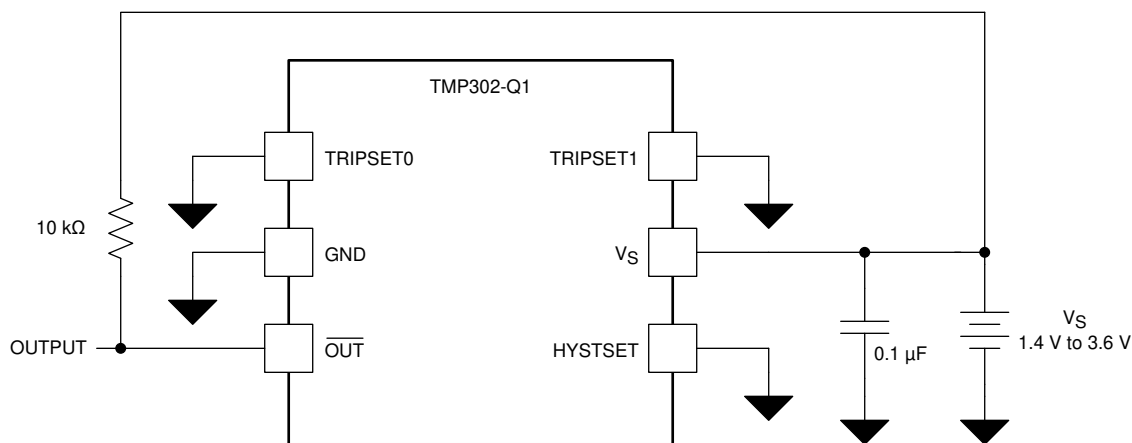
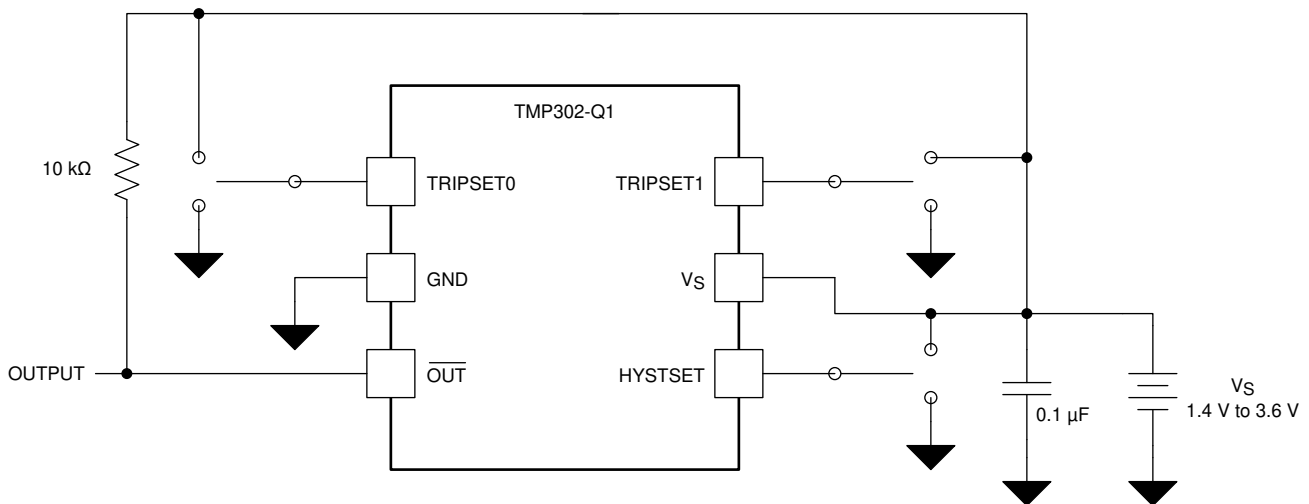


Figure 10. TMP302-Q1 Typical Application Schematic

Figure 11 shows the most generic implementation of the TMP302-Q1 family of devices. Switches are shown connecting the TMPSET0, TMPSET1 and HYSTSET pins to either  $V_S$  or ground. The use of switches is not strictly required; the switches are shown only to illustrate the various pin connection combinations. In practice, connecting the TMPSET0, TMPSET1 and HYSTSET pins to ground or directly to the  $V_S$  pin is sufficient and minimizes space and cost. If additional flexibility is desired, connections from the TMPSET0, TMPSET1 and HYSTSET pins can be made through 0- $\Omega$  resistors which can be either populated or not populated depending upon the desired connection.

## Typical Application (continued)



**Figure 11. TMP302-Q1 Generic Application Schematic**

### 9.2.1 Design Requirements

Designing with the TMP302-Q1 family of devices is simple. The TMP302-Q1 family of devices is a temperature switch commonly used to signal a microprocessor in the event of an over temperature condition. The temperature at which the TMP302-Q1 family of devices issues an active low alert is determined by the configuration of the TRIPSET0 and TRIPSET1 pins. These two pins are digital inputs and must be tied either high or low, according to Table 1. The TMP302-Q1 family of devices issues an active low alert when the temperature threshold is exceeded. The device has built-in hysteresis to avoid the device from signaling the microprocessor as soon as the temperature drops below the temperature threshold. The amount of hysteresis is determined by the HYSTSET pin. This pin is a digital input and must be tied either high or low, according to Table 2.

See Figure 10 and Figure 11 for typical circuit configurations.

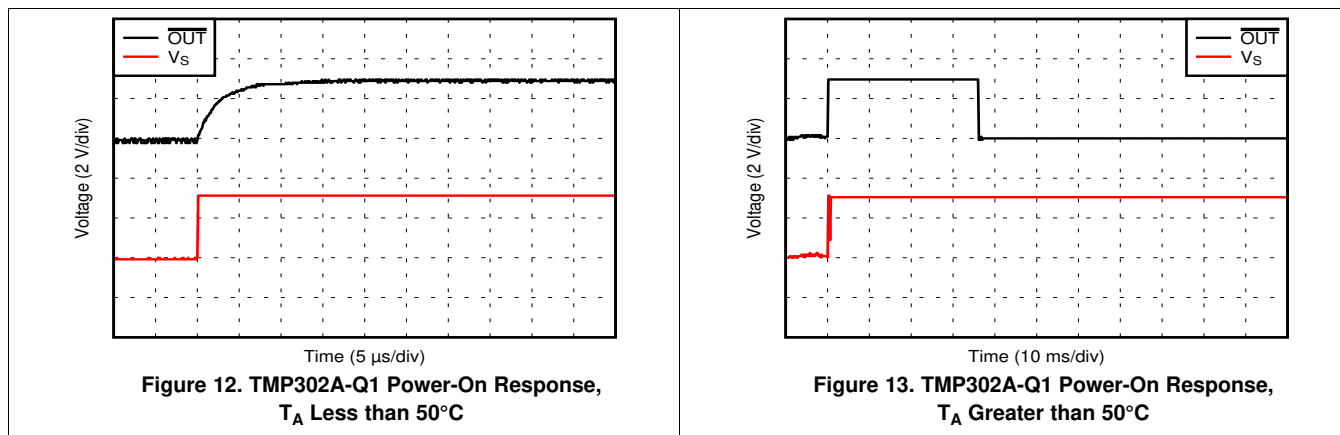
### 9.2.2 Detailed Design Procedure

Determine the threshold temperature and hysteresis required for the application. Connect the TRIPSET0, TRIPSET1, and HYSTSET pins according to the design requirements. Refer to Table 1 and Table 2. Use a 10-kΩ pullup resistor from the  $\overline{\text{OUT}}$  pin to the  $V_S$  pin. To minimize power, a larger-value pullup resistor can be used but must not exceed 100 kΩ. Place a 0.1-μF bypass capacitor close to the TMP302-Q1 device to reduce noise coupled from the power supply.

### 9.2.3 Application Curves

Figure 12 and Figure 13 show the TMP302A-Q1 power-on response with the ambient temperature less than 50°C and greater than 50°C respectively. The TMP302A-Q1 was configured with trip point set to 50°C. The TMP302B-Q1, TMP302C-Q1, and TMP302D-Q1 devices behave similarly with regards to power on response with  $T_A$  below or above the trip point. Note that the  $\overline{\text{OUT}}$  signal typically requires 35 ms following power on to become valid.

Typical Application (continued)



10 Power Supply Recommendations

The TMP302-Q1 family of devices is designed to operate from a single power supply within the range 1.4 V and 3.6 V. No specific power supply sequencing with respect to any of the input or output pins is required. The TMP302-Q1 family of devices is fully functional within 35 ms of the voltage at the  $V_S$  pin reaching or exceeding 1.4 V.

11 Layout

11.1 Layout Guidelines

Place the power supply bypass capacitor as close as possible to the  $V_S$  and GND pins. The recommended value for this bypass capacitor is 0.1- $\mu\text{F}$ . Additional bypass capacitance can be added to compensate for noisy or high-impedance power supplies. Place a 10-k $\Omega$  pullup resistor from the open drain  $\overline{\text{OUT}}$  pin to the power supply pin  $V_S$ .

11.2 Layout Example

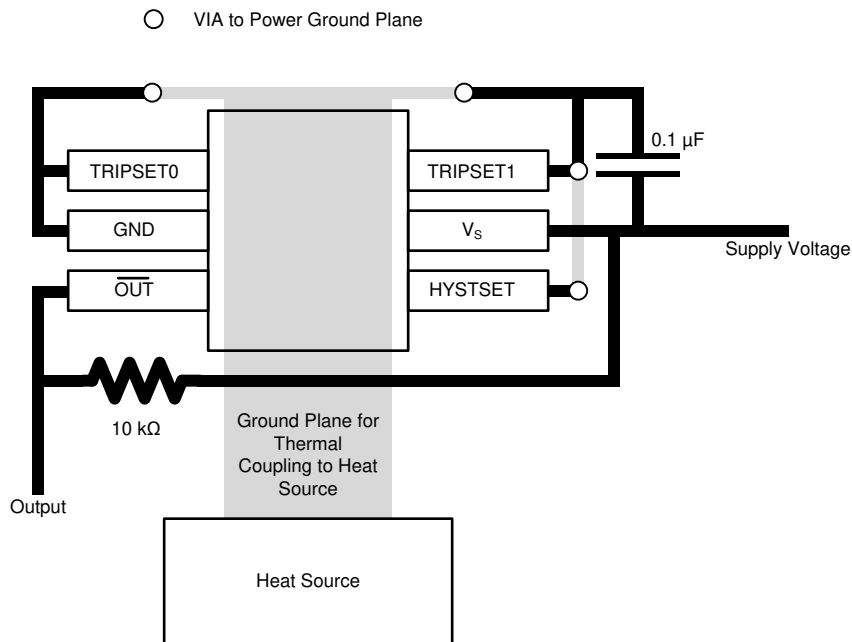


Figure 14. Layout Example

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP302AQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHQ	<a href="#">Samples</a>
TMP302BQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHR	<a href="#">Samples</a>
TMP302CQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHS	<a href="#">Samples</a>
TMP302DQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHT	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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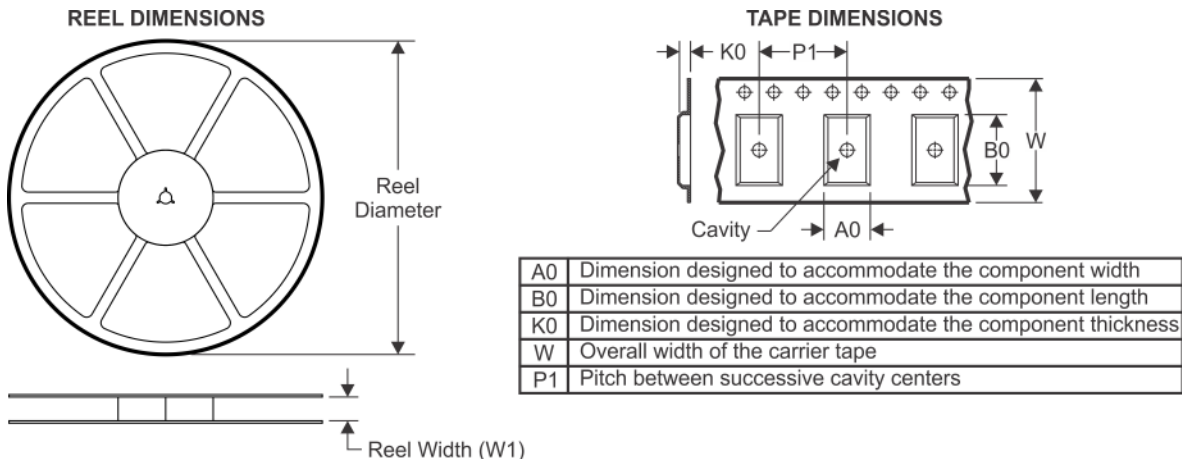
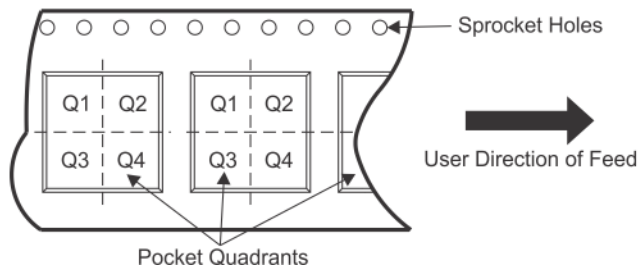
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TMP302-Q1 :**

- Catalog: [TMP302](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP302AQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302BQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302CQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302DQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

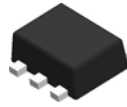
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP302AQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0
TMP302BQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0
TMP302CQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0
TMP302DQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0



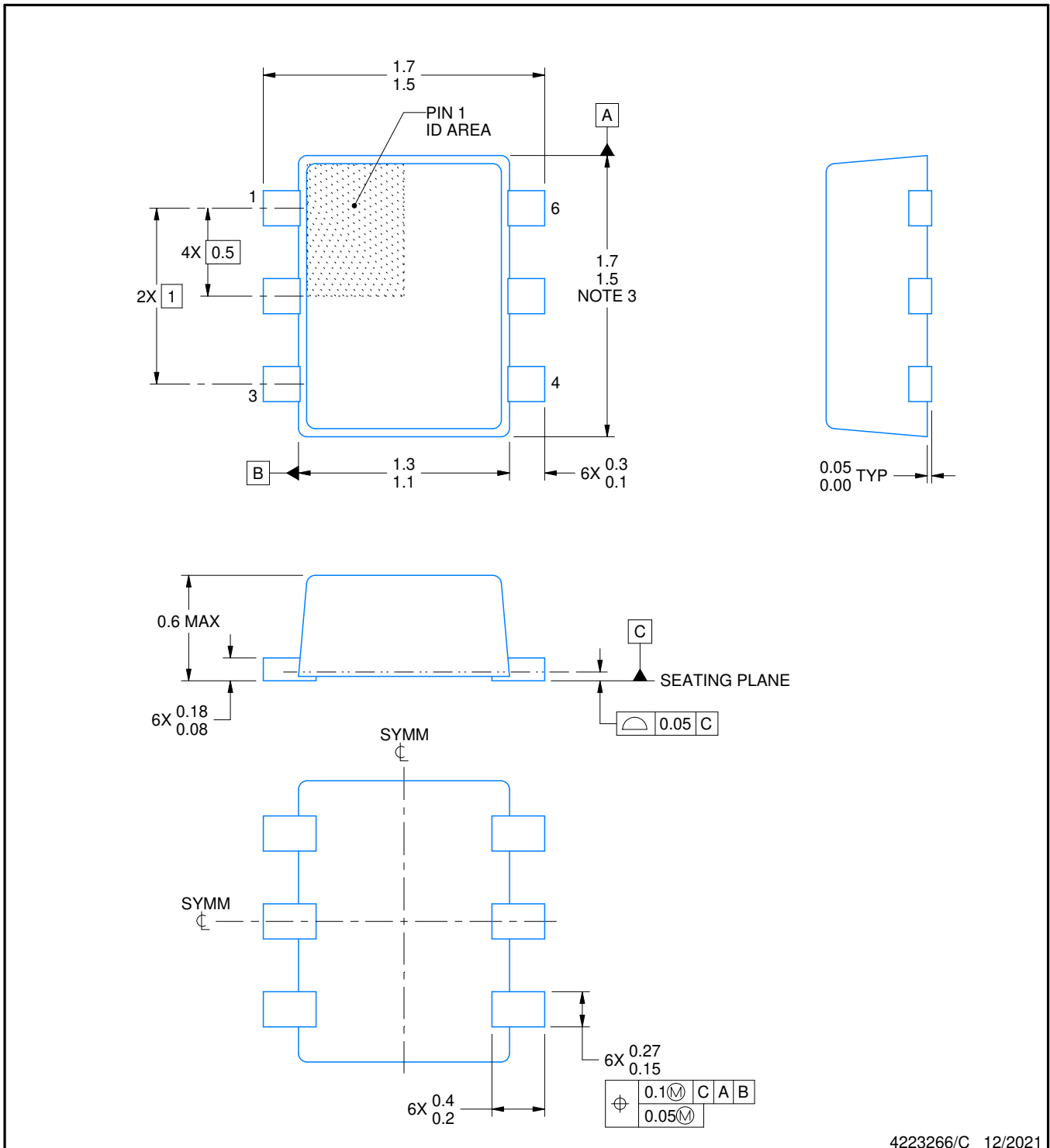
DRL0006A



# PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

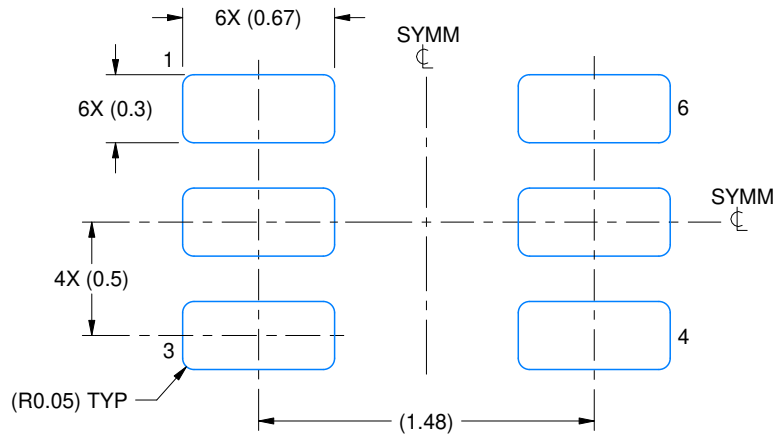
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

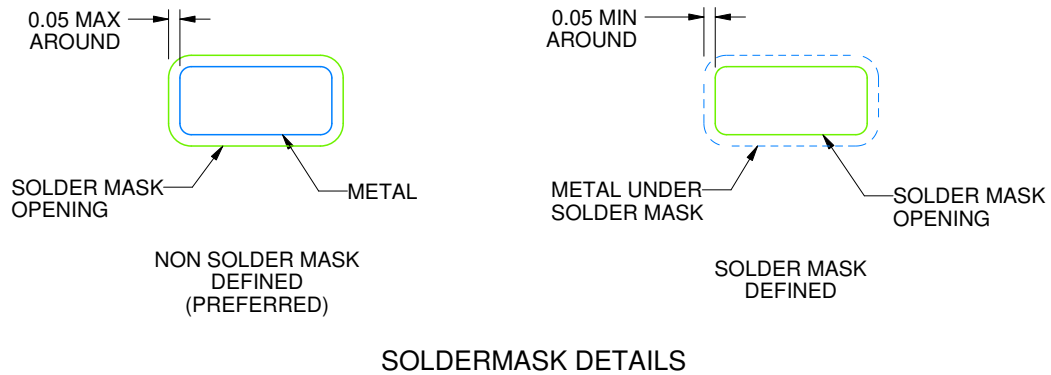
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

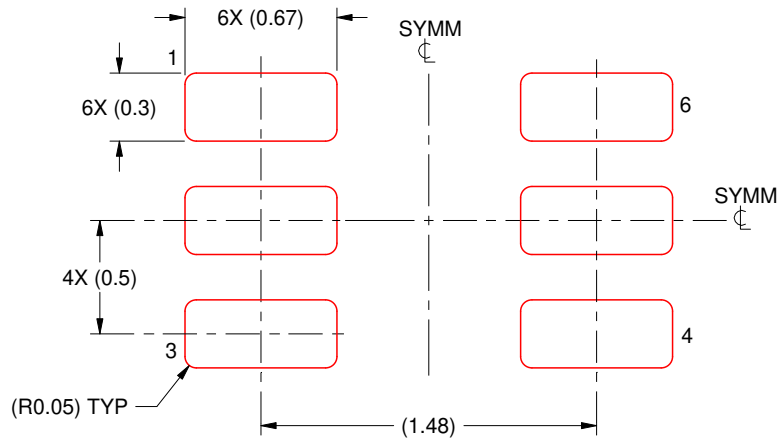
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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