Description

The F1240 is a dual channel IF variable gain amplifier for diversity basestation receivers. Each channel has 31.5dB of total attenuation and a 0.5dB attenuation step. The device offers significantly better noise and distortion performance than currently available devices. It is packaged in a compact 5mm x 5mm QFN with 200Ω differential input and output impedances for ease of integration into the receiver lineup.

Competitive Advantage

The F1240 IF VGA improves system signal-to-noise (SNR), especially at lower gain settings. With IDT's proprietary *FlatNoise™* technology both OIP3 and noise figure are kept virtually flat while gain is backed off, enhancing SNR significantly under high level interferer conditions, and greatly benefiting 2G/3G/4G Multi-Carrier IF sampling receivers.

The fast settling time, less than 15ns, gain step of 0.5dB coupled with the excellent differential linearity allow for signal to noise ratio (SNR) to be maximized further by targeting the minimum necessary gain in small, accurate increments.

The matched output does not require a terminating resistor, thus the gain and distortion performance are preserved when driving bandpass anti-alias filters.

See the Applications Information section for more details and benefits of the F1240 in IF sampling receivers.

Typical Applications

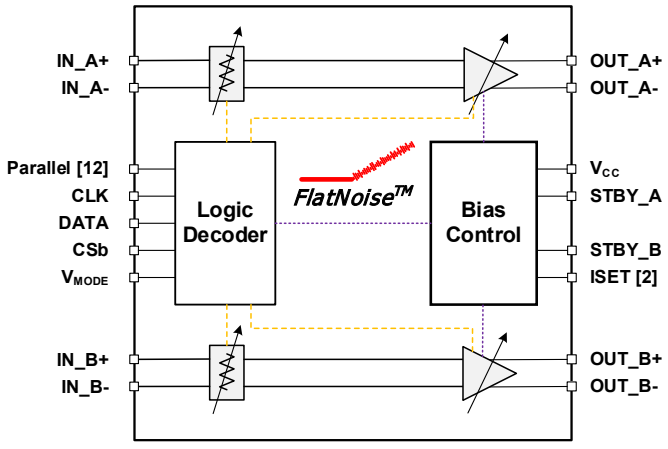
- Base Station 2G, 3G, 4G, TDD radio cards
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure

Features

- Ideal for systems with high SNR requirements
- 20dB typical Maximum Gain
- 31.5dB gain control range
- 6 bit control via serial or parallel control
- 0.5dB Gain Steps
- Excellent Noise Figure : 4.0dB
- NF degrades just 1.3dB @ 10dB below Max Gain
- 200Ω Differential Matched Input
- 200Ω Differential Matched Output
- No termination resistors required
- 10MHz – 500MHz frequency range
- Ultra-Linear: OIP3 +47dBm typical
- Excellent 2nd Harmonic Rejection
- External current setting resistors
- Very fast settling < 15ns
- Individual Power Down Modes
- Extremely Low Power: 80mA / Chan
- 5 × 5 32-QFN package

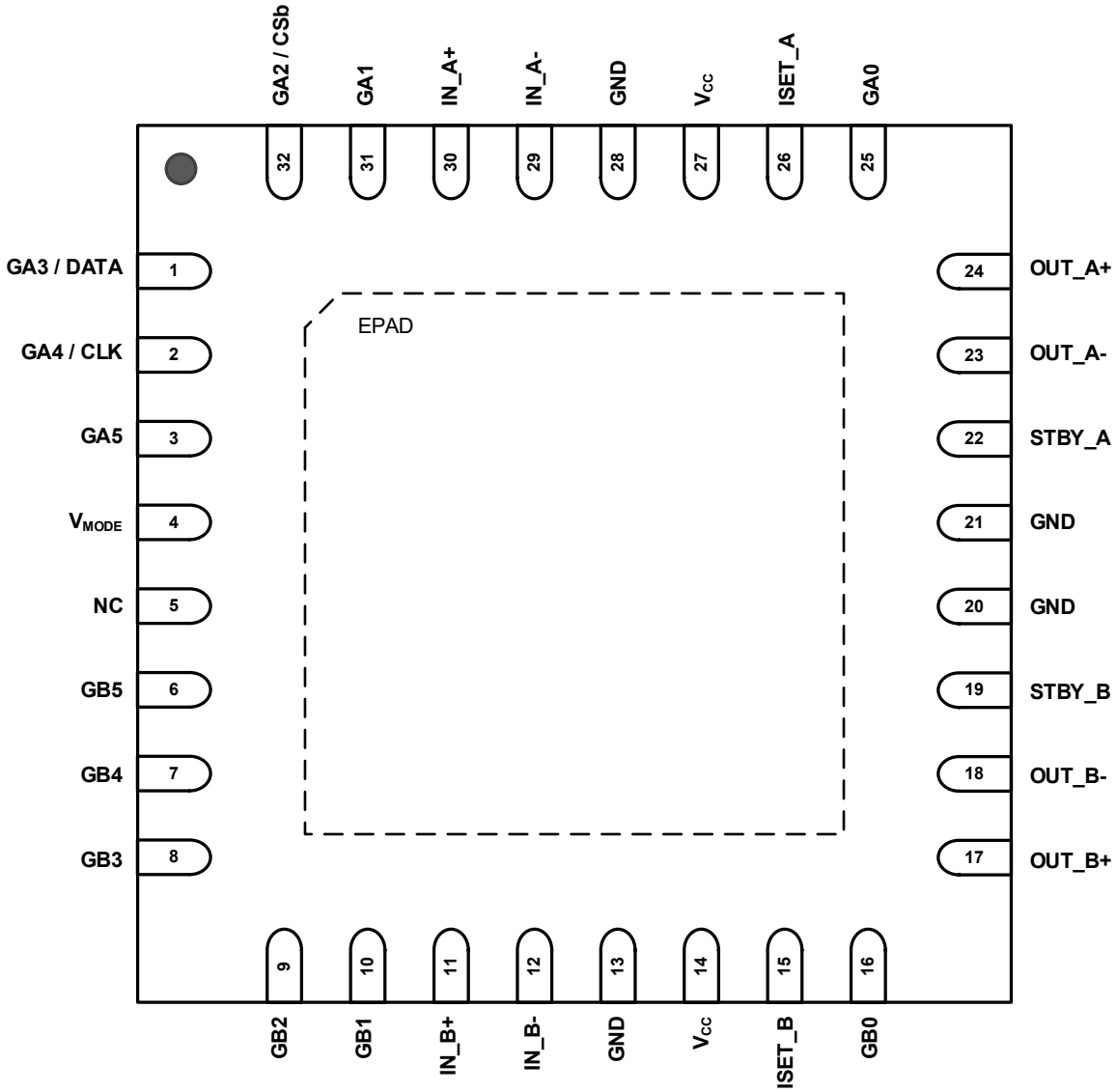
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 5 x 5 x 0.75 mm QFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	GA3 / DATA	4dB Attenuation control bit for Channel A (Parallel Mode) or DATA (Serial Mode).
2	GA4 / CLK	8dB Attenuation control bit for Channel A (Parallel Mode) or CLK (Serial Mode).
3	GA5	16dB Attenuation control bit for Channel A.
4	V_{MODE}	For the parallel mode set for logic HIGH or float (internal pullup resistor) Set for logic Low for the serial mode.
5, 13, 20, 21, 28	GND	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
6	GB5	16dB Attenuation control bit for Channel B.
7	GB4	8dB Attenuation control bit for Channel B.
8	GB3	4dB Attenuation control bit for Channel B.
9	GB2	2dB Attenuation control bit for Channel B.
10	GB1	1dB Attenuation control bit for Channel B.
11	IN_B+	Channel B Differential Input +. Pin is AC coupled.
12	IN_B-	Channel B Differential Input -. Pin is AC coupled.
14	V_{CC}	Power supply input. Bypass to ground with capacitors as close as possible to pin.
15	ISET_B	Channel B I_{CC} set: Use the recommended value from the BOM section.
16	GB0	0.5dB Attenuation control bit for Channel B.
17	OUT_B+	Channel B Differential Output+. Pull up to V_{CC} through an inductor. An external series capacitor is required.
18	OUT_B-	Channel B Differential Output-. Pull up to V_{CC} through an inductor. An external series capacitor is required.
19	STBY_B	Pull low to Power Down Channel B. Float or Pull HIGH to enable Channel B.
22	STBY_A	Pull low to Power Down Channel A. Float or Pull HIGH to enable Channel A.
23	OUT_A-	Channel A Differential Output -. Pull up to V_{CC} through an inductor. An external series capacitor is required.
24	OUT_A+	Channel A Differential Output +. Pull up to V_{CC} through an inductor. An external series capacitor is required.
25	GA0	0.5dB Attenuation control bit for Channel A.
26	ISET_A	Channel A I_{CC} set: Use the recommended value from the BOM section.
27	V_{CC}	Connect this pin to the 5V DC Power Bus. Bypass capacitor is required.
29	IN_A-	Channel A Differential Input -. Pin is AC coupled.
30	IN_A+	Channel B Differential Input +. Pin is AC coupled.
31	GA1	1dB Attenuation control bit for Channel A.
32	GA2 / CSb	2dB Attenuation control bit for Channel A (Parallel Mode) or Chip Select, CSb (Serial Mode).
	– EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1240 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Power Supply	V_{CC}	-0.3	+5.5	V
GA[5-0], GB[5-0], DATA, CSb, CLK, V_{MODE}, STBY_A, STBY_B	V_{LOGIC}	-0.3	V_{CC} + 0.25	V
IN_A+, IN_A-, IN_B+, IN_B-	V_{RFIN}	-0.3	+2.2	V
OUT_A+, OUT_A-, OUT_B+, OUT_B-	V_{RFOUT}	+2.56	V_{CC} + 0.25	V
Maximum RF Input Power (IN_A+, IN_A-, IN_B+, IN_B-) at maximum gain	P_{MAX}		+15	dBm
Continuous Power Dissipation	P_{DISS}		1.5	W
Junction Temperature	T_{JMAX}		+150	°C
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		500 (Class 1B)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		1000 (Class C3)	V

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power supply voltage	V_{CC}		+4.75		+5.25	V
Operating Temperature Range	T_{EPAD}	Exposed paddle	-40		+100	°C
RF Frequency Range	f_{RF}	Low Distortion Range Maximum Gain Setting OIP3 > 40 dBm, P_{OUT} = +3dBm/Tone	50		400	MHz
		Operating Range Gain > 17dB L1=L2=L3=L4=1500nH	10		560	
Input Port Impedance	Z_{IN_A}, Z_{IN_B}	Differential		200		Ω
Output Port Impedance	Z_{OUT_A}, Z_{OUT_B}	Differential		200		Ω

Electrical Characteristics

See the F1240 Typical Application Circuit. Specifications apply when operated at V_{CC} = +5.0V, f_{RF} = 200MHz, T_{EPAD} = +25°C, Parallel Mode (V_{MODE} is logic HIGH), STBY_A=STBY_B=is logic HIGH, $Z_S = Z_L = 200\Omega$ differential, maximum gain setting, tone spacing = 0.8MHz, P_{OUT} = +3dBm/tone, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Table 4. Electrical Characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}		2.0 [a]			V
Logic Input Low Threshold	V_{IL}		0.0		0.8	V
Logic Current	I_{IH}, I_{IL}	GA[5-0], GB[5-0]	***-2***		***+2***	µA
		V_{MODE}, STBY_A, STBY_B	***-10***		***+1***	
DC Current	I_{CC}	STBY_A=STBY_B set for logic HIGH		160	***176***	mA
	I_{STBY}	STBY_A=STBY_B set for logic LOW		2.3	***5***	
Minimum Gain Step	LSB			0.5		dB
Attenuation Range				31.5		dB
Maximum Gain	G_{MAX}	Gain Setting = 20dB, or Attenuator Setting = 0dB	***18***	20		dB
Minimum Gain	G_{MIN}	Gain Setting = -11.5dB, or Attenuator Setting = 31.5dB		-11.5	***-9***	dB
Return Loss	RL			15		dB
Relative Phase Between the Minimum and Maximum Attenuation	Φ_{Δ}	f_{RF}=200MHz		7		deg
		f_{RF}=350MHz		14		
		f_{RF}=450MHz		20		
Relative Phase over any 8 dB Attenuation Range	$\Phi_{\Delta 8}$	f_{RF}=200MHz		3		deg
		f_{RF}=350MHz		5		
		f_{RF}=450MHz		8		
Step Error	DNL			0.08		dB
Absolute Attenuation Error (Attenuation = 20 – Gain State)	INL	Over 50MHz to 300MHz and temperature	±(0.3+5%ATT) Typical			dB
		Over 300MHz to 500MHz and temperature	±(0.5+5%ATT) Typical			
1dB Gain Rolloff	BW	Frequency with a 1 dB gain reduction compared to gain at 100MHz at the maximum gain setting		350		MHz
Channel Isolation	ISOL	OUT_B referenced to OUT_A with power applied at IN_A at maximum gain setting	60	69		dBc

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Electrical Characteristics

See the F1240 Typical Application Circuit. Specifications apply when operated at V_{CC} = +5.0V, f_{RF} = 200MHz, T_{EPAD} = +25°C, Parallel Mode (V_{MODE} is logic HIGH), STBY_A=STBY_B=is logic HIGH, $Z_S = Z_L = 200\Omega$ differential, maximum gain setting, tone spacing = 0.8MHz, P_{OUT} = +3dBm/tone, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Table 5. Electrical Characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output Third Order Intercept Point	$OIP3_{20A}$	Gain Setting = 20.0dB, or Attenuator Setting = 0dB	42	46.5		dBm
	$OIP3_{20B}$	Gain Setting = 20.0dB, or Attenuator Setting = 0dB Tone Spacing= 20MHz		45		
	$OIP3_{10}$	Gain Setting = 10dB, or Attenuator Setting = 10dB	42	44.5		
	$OIP3_{20C}$	Gain Setting = 20dB, or Attenuator Setting = 0dB f_{RF} = 350MHz		41		
	$OIP3_{20D}$	Gain Setting = 20dB, or Attenuator Setting = 0dB f_{RF} = 450MHz		41		
Output Second Order Intercept Point	OIP2	Gain Setting = 10dB, or Attenuator Setting = 10dB f_1 = 190MHz, f_2 = 210MHz, $f_M = f_2 - f_1$		76		dBm
Second Harmonic	H2	Gain Setting = 10dB, or Attenuator Setting = 10dB Output Power = + 3dBm		-90		dBc
Maximum spurious level on any RF port	$SPUR_{MAX}$	No RF Power applied			-135	dBm
Noise Figure	NF	Gain Setting = 20dB, or Attenuator Setting = 0dB		4.0	4.5	dB
		Gain Setting = 10.0dB, or Attenuator Setting = 10.0dB		5.3	5.8	
Output 1dB Compression	OP1dB	Gain Setting = 20dB, or Attenuator Setting = 0dB	***16***	19.7		dBm

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Electrical Characteristics

See the F1240 Typical Application Circuit. Specifications apply when operated at V_{CC} = +5.0V, f_{RF} = 200MHz, T_{EPAD} = +25°C, Parallel Mode (V_{MODE} is logic HIGH), STBY_A=STBY_B=is logic HIGH, $Z_S = Z_L = 200\Omega$ differential, maximum gain setting, tone spacing = 0.8MHz, P_{OUT} = +3dBm/tone, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Table 6. Electrical Characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Amplifier Switching Time [b]	t_{OFF}	50% control signal to 30dBc of initial output power. STBY is switched from logic HIGH to Logic LOW.		100		ns
	t_{ON}	50% control signal to 0.5dBc of final output power. STBY is switched from logic LOW to Logic HIGH.		200		
Settling Time [b]	t_{1dB}	Any two Adjacent 1dB Steps and settled to within +/-0.1dB of the final power level		12		ns
Maximum Glitch		Only 1 transition has a glitch greater than 0.4dB (8.5dB to 8.0dB)		0.4	1.5	dB
Clock to CSb Setup	t_{EN}	CSb must be pulled low this minimum interval BEFORE the next rising clock edge	***8***			ns
Clock Pulse Width	t_W	Minimum clock interval from rising to falling edge		20		ns

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Speeds are measured after SPI programming is completed (data latched with CSb = HIGH).

Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance.	θ_{JA}	40	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	3	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- V_{cc} = 5.0V
- $Z_L = Z_S$ = 100Ω Single Ended or 200Ω Differential
- f_{RF} = 200MHz
- T_{EPAD} = +25°C
- STBY = HIGH
- P_{out} = 3dBm/Tone
- 0.8MHz or 20MHzTone Spacing
- Gain setting = Maximum Gain
- All temperatures are referenced to the exposed paddle
- Linear parameters have the Evaluation Kit traces and connector losses de-embedded.
- Non-linear parameters (IP3, P1dB, NF, switching) are measured using the single ended evaluation board with scalar correction.

Typical Performance Characteristics

Figure 3. Gain versus Frequency [All States]

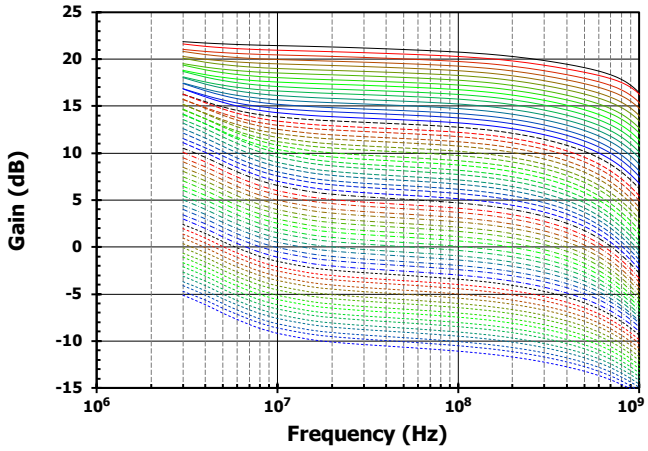


Figure 4. Gain versus Gain Setting

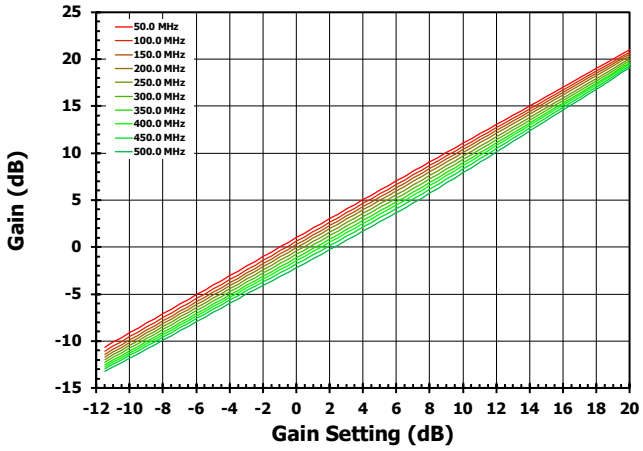


Figure 5. Input Return Loss versus Frequency [All States]

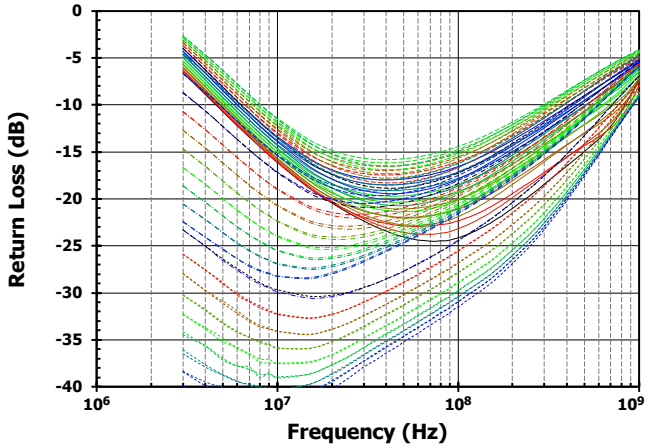


Figure 6. Input Return Loss versus Gain Setting

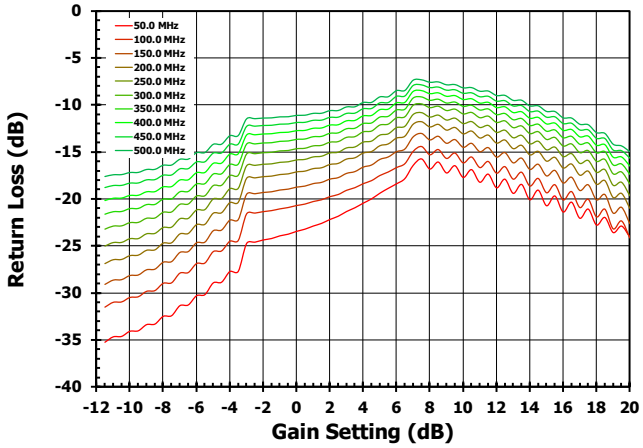


Figure 7. Output Return Loss versus Frequency [All States]

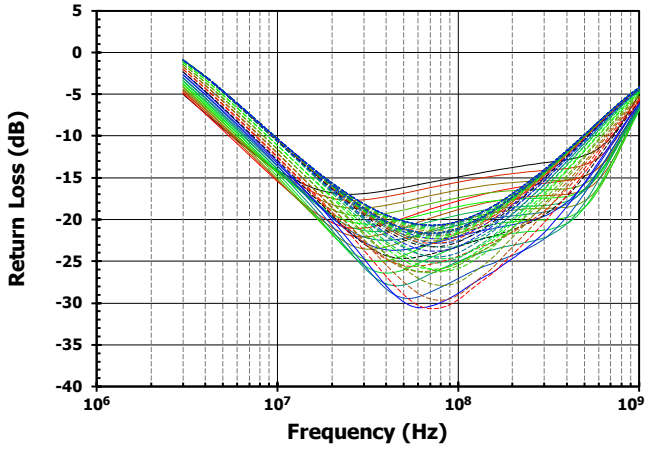
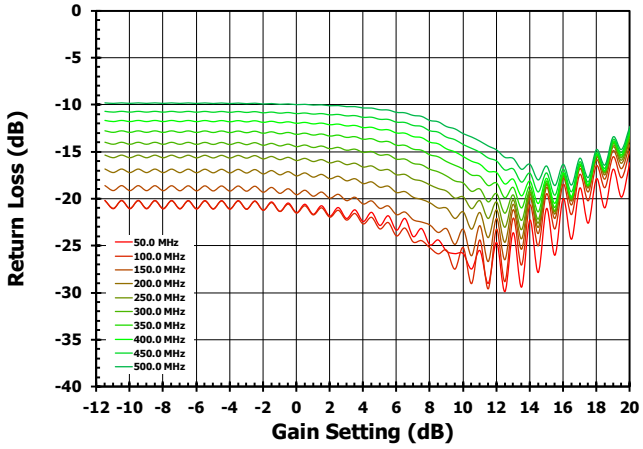


Figure 8. Output Return Loss versus Gain Setting



Typical Performance Characteristics

Figure 9. Relative Insertion Phase versus Frequency [All States]

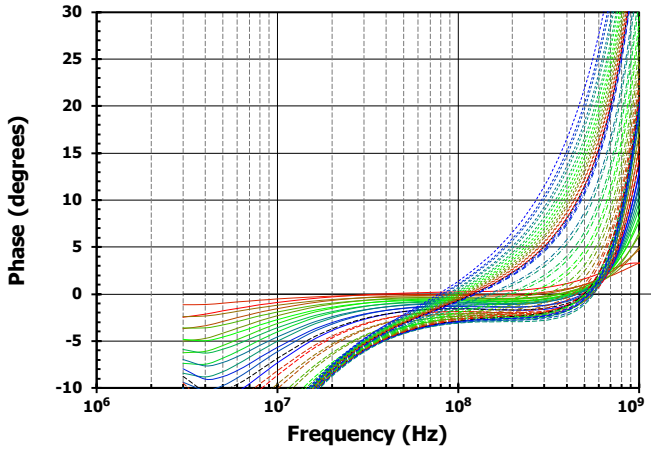


Figure 10. Relative Insertion Phase versus Gain Setting

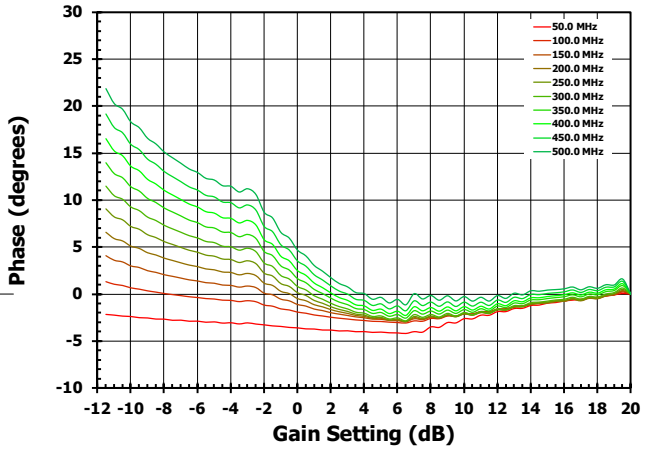


Figure 11. Relative Insertion Phase over any 8dB Range versus Frequency

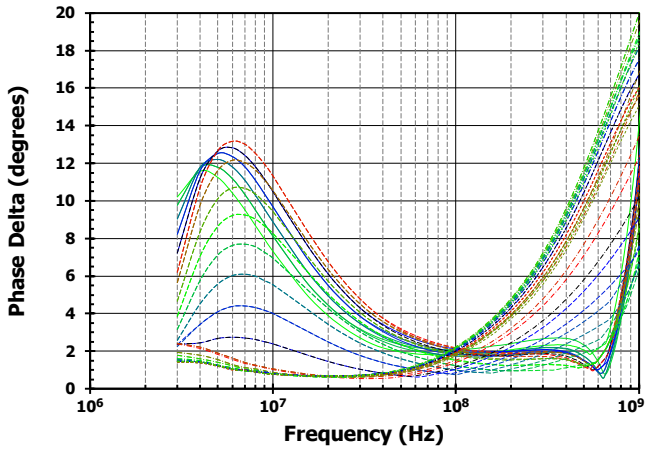


Figure 12. Relative Insertion Phase over any 8dB Range versus Gain Setting

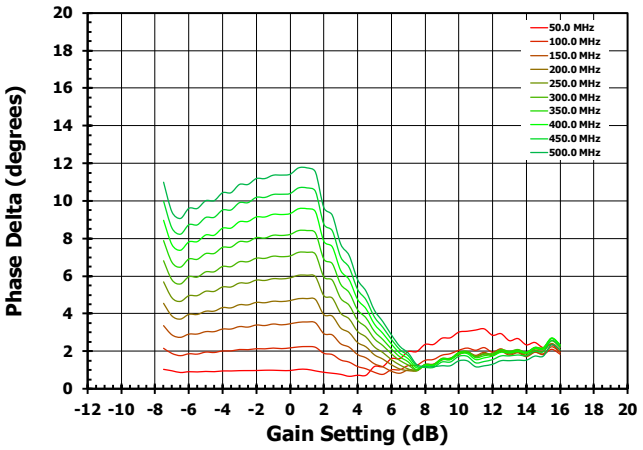
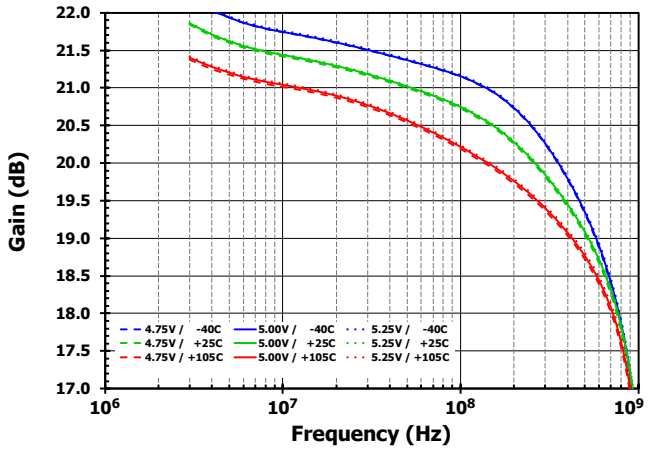


Figure 13. Maximum Gain versus Frequency



Typical Performance Characteristics

Figure 14. Reverse Isolation versus Frequency [All States]

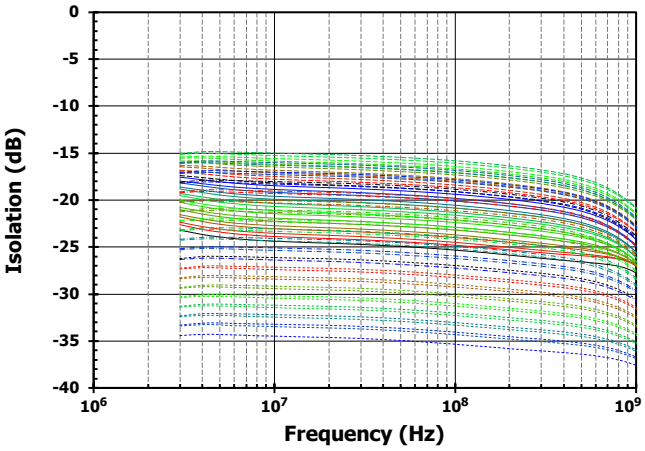


Figure 15. Reverse Isolation versus Gain Setting

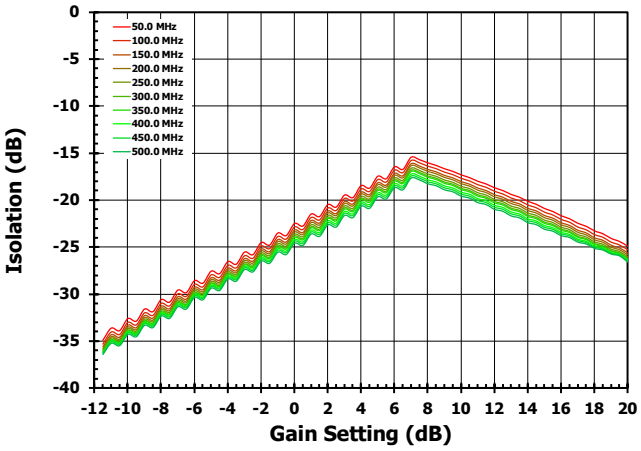


Figure 16. Worse Case Gain Accuracy versus Frequency

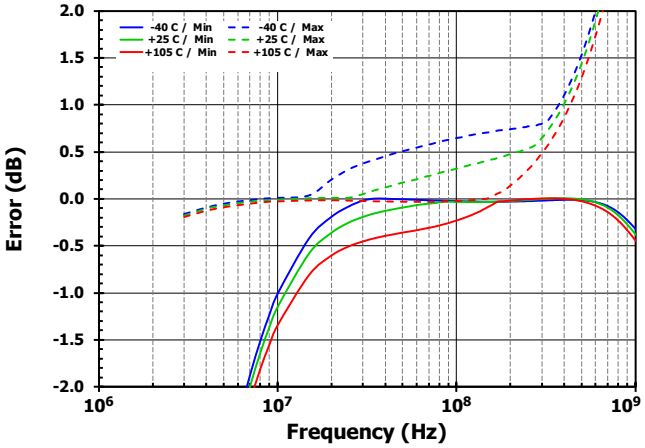


Figure 17. Gain Accuracy versus Gain Setting

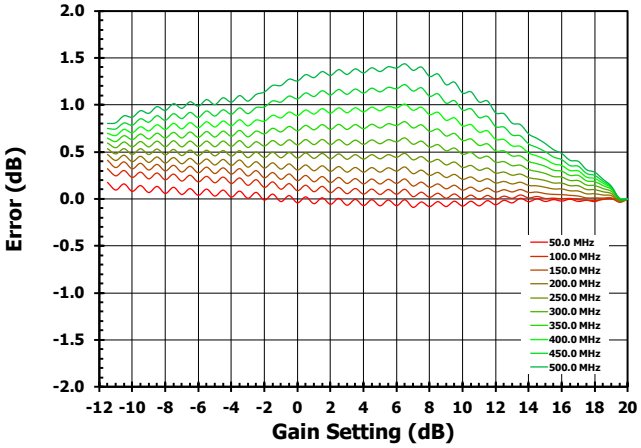


Figure 18. Worse Case Step Error versus Frequency

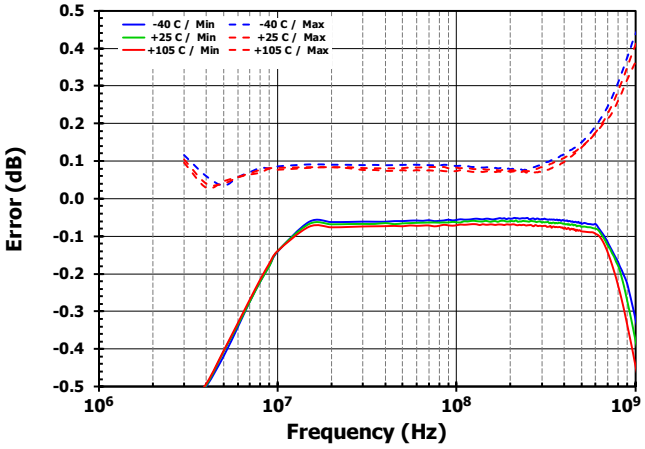
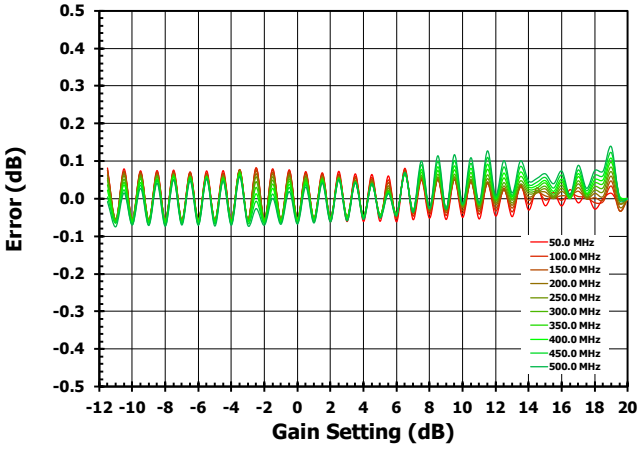


Figure 19. Step Error versus Gain Setting



Typical Performance Characteristics

Figure 20. Output IP3 versus Frequency [Maximum Gain]

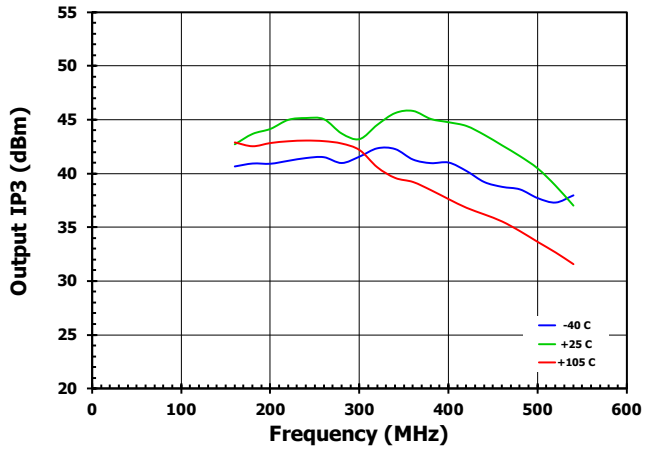


Figure 21. Second Harmonic versus Frequency [Maximum Gain]

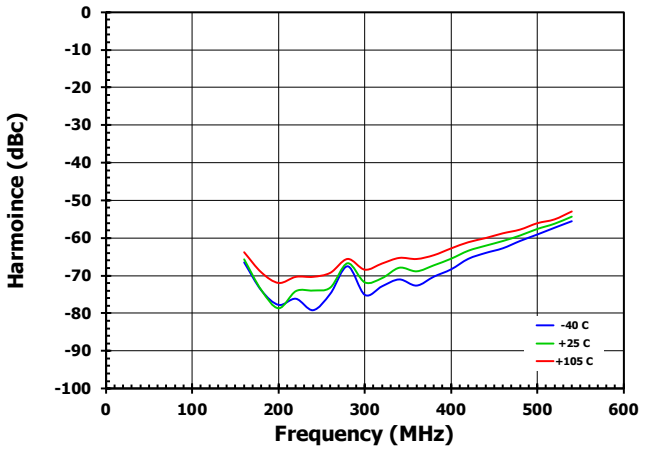


Figure 22. Output P1B Compression versus Frequency [Maximum Gain]

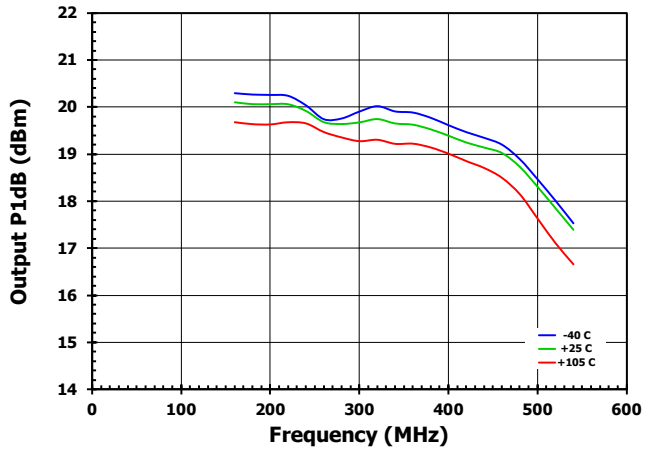
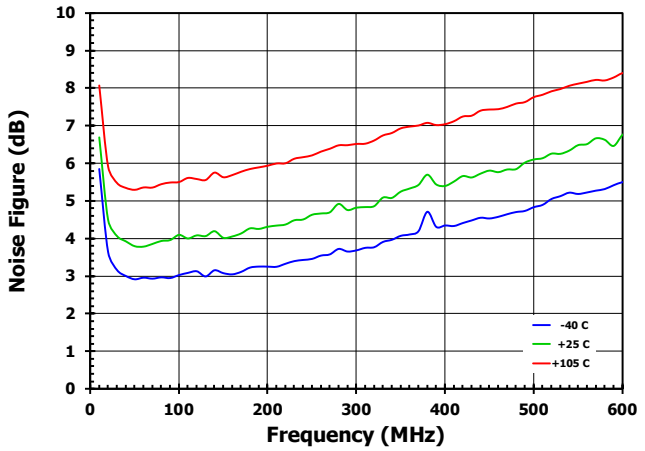


Figure 23. Noise Figure versus Frequency [Maximum Gain]



Typical Performance Characteristics

Figure 24.Output IP3 versus Gain State [200MHz]

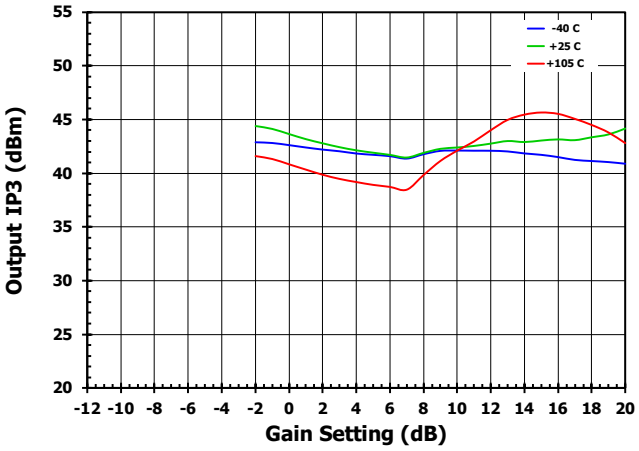


Figure 25.Output P1dB versus Gain State [200MHz]

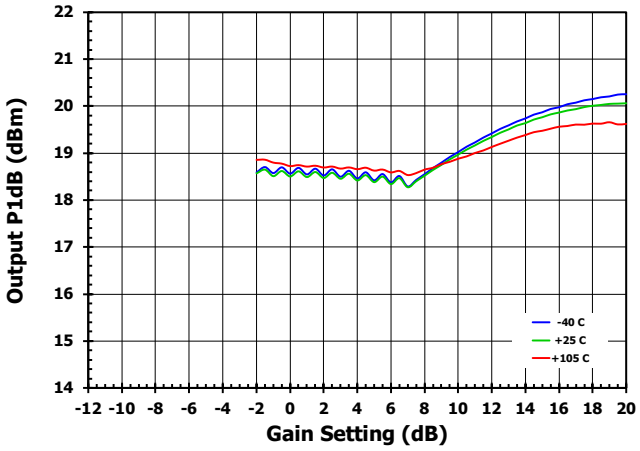


Figure 26.Output IP3versus Gain State [350MHz]

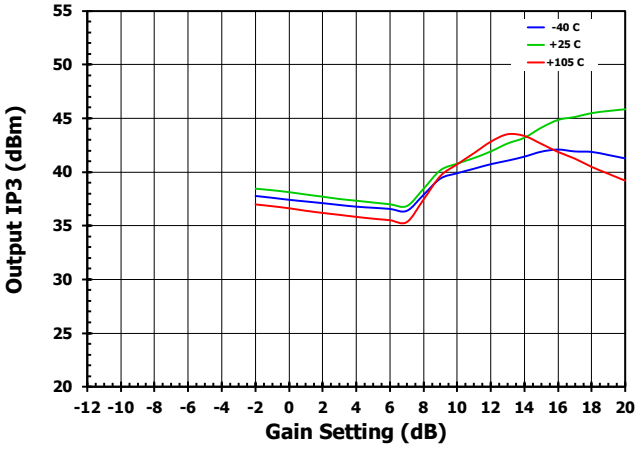


Figure 27.Output P1dB versus Gain State [350MHz]

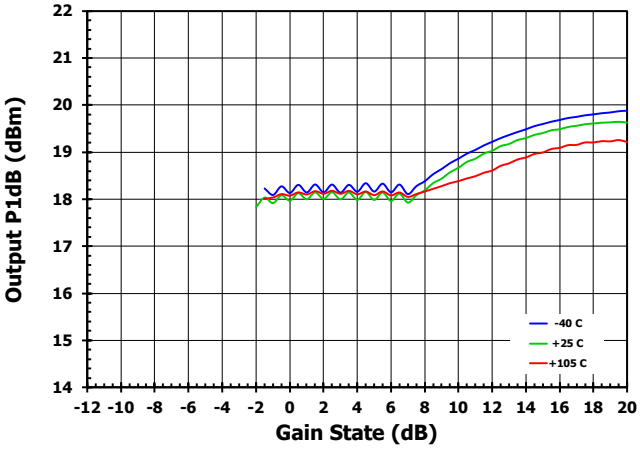


Figure 28.Output IP3 versus Gain State [450MHz]

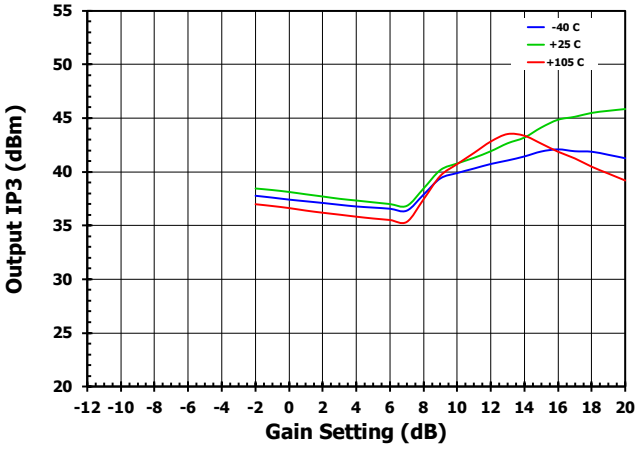
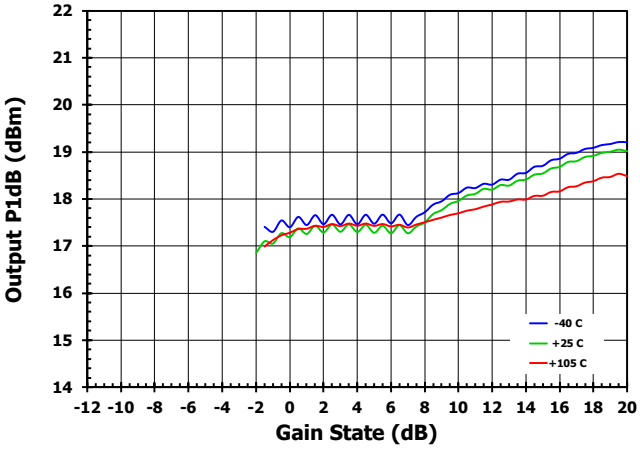


Figure 29.Output P1dB versus Gain State [450MHz]



Typical Performance Characteristics

Figure 30. 2nd Harmonic versus Gain State [200MHz]

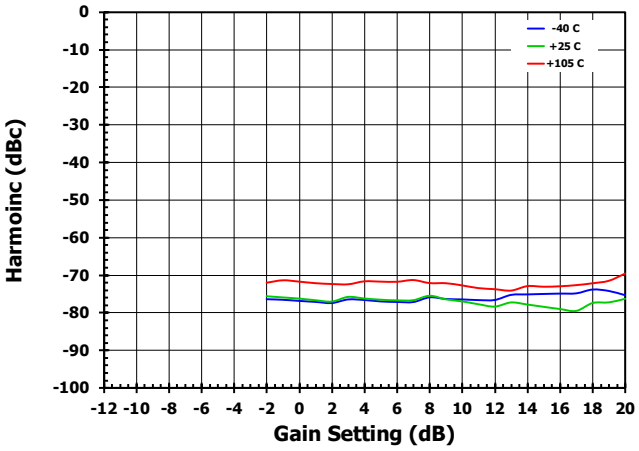


Figure 31. Noise Figure versus Gain State [200MHz]

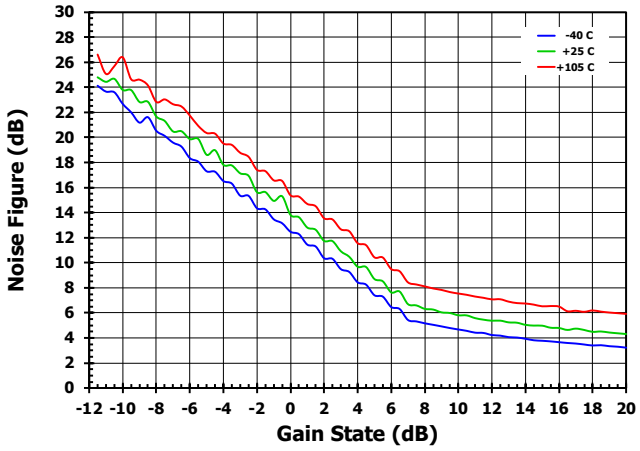


Figure 32. 2nd Harmonic versus Gain State [350MHz]

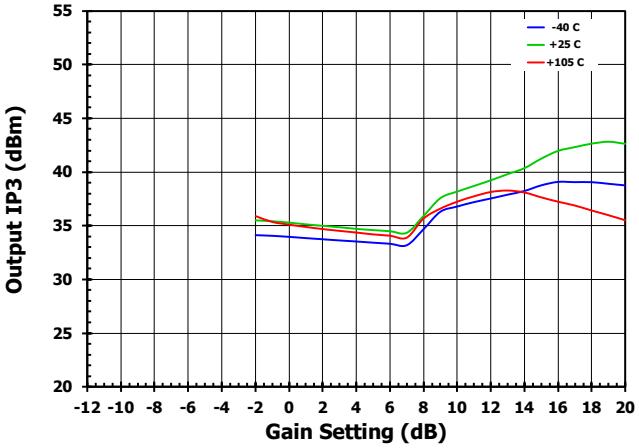


Figure 33. Noise Figure versus Gain State [350MHz]

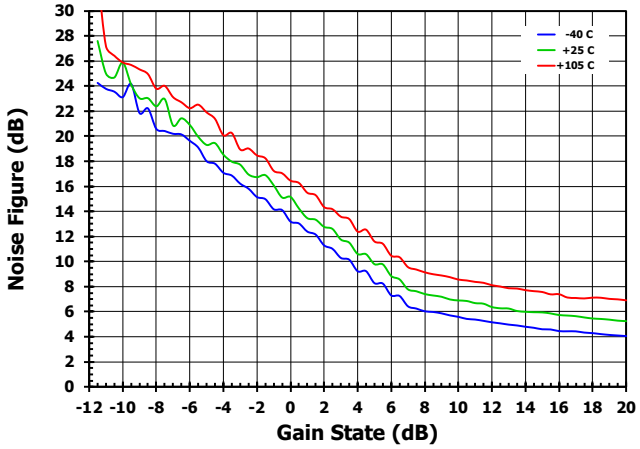


Figure 34. 2nd Harmonic versus Gain State [450MHz]

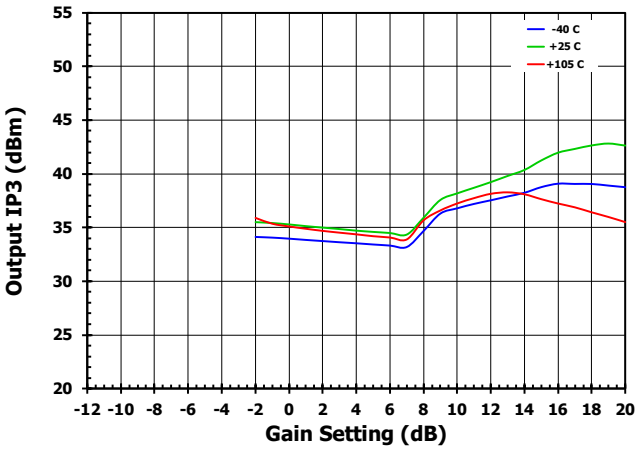
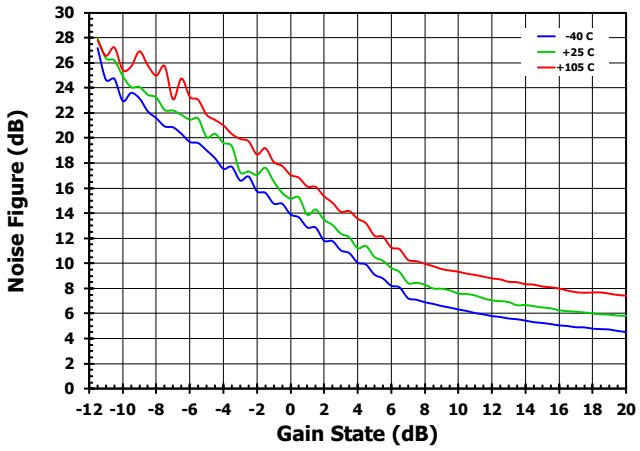


Figure 35. Noise Figure versus Gain State [450MHz]



Typical Performance Characteristics

Figure 36. Channel Isolation versus Frequency [Maximum Gain]

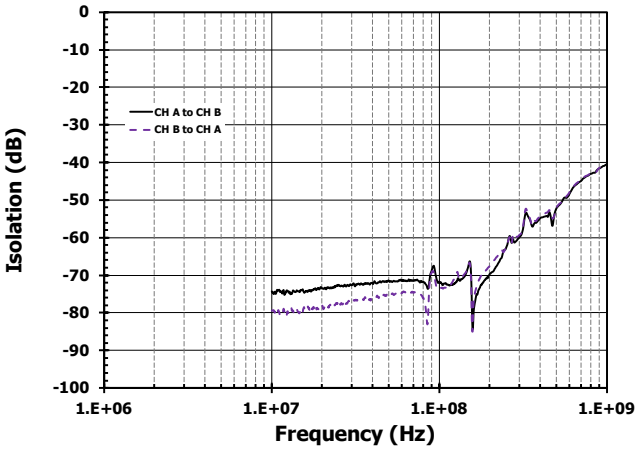


Figure 37. Current versus Power Supply

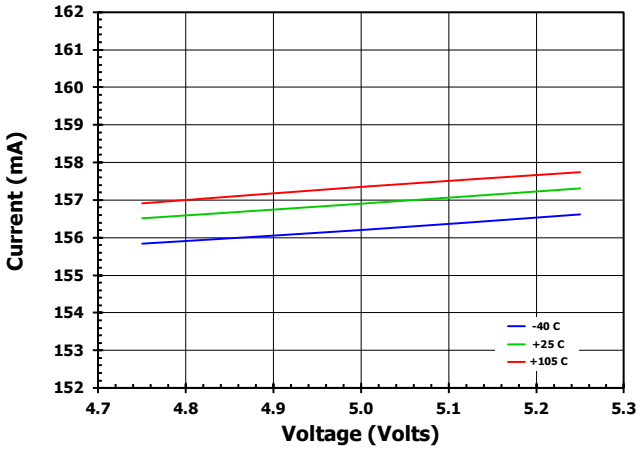


Figure 38. Typical Standby OFF to ON Switching

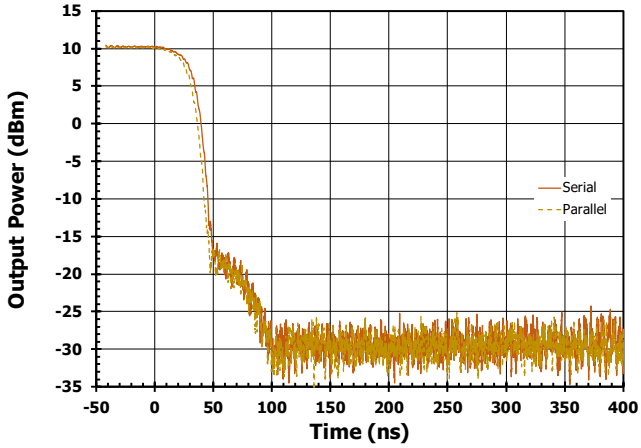


Figure 39. Typical Standby ON to OFF Switching

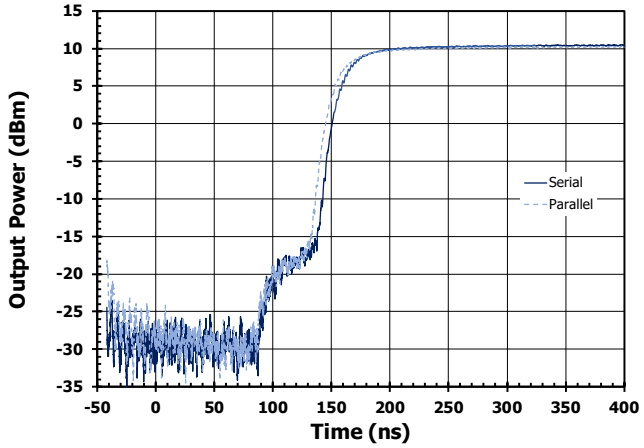


Figure 40. Typical Switching Characteristics

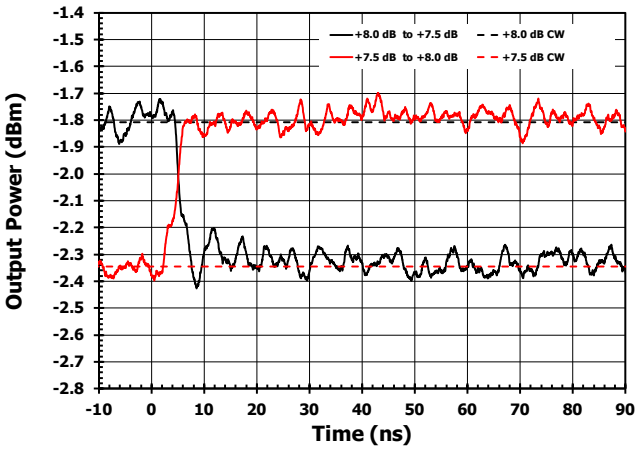
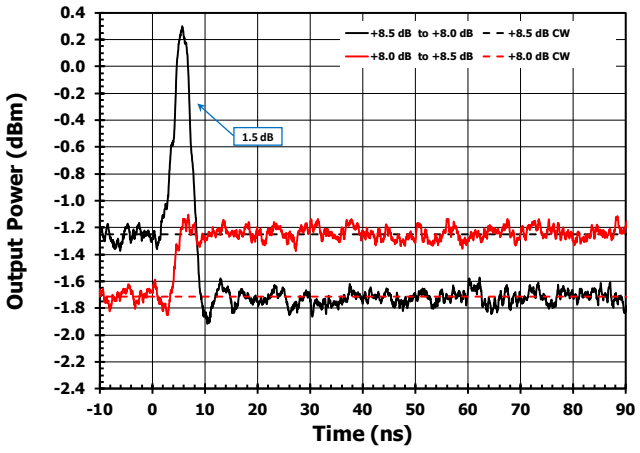


Figure 41. Worse Case Switching Characteristics (8.5 to 8.0 dB)



Programming

F1240 can be programmed using either the parallel or serial interface which is selectable via V_{MODE} (pin 4). The serial mode is selected by setting V_{MODE} to a logic LOW and the parallel mode by floating V_{MODE} or by setting V_{MODE} to a logic HIGH.

Serial Mode

F1240 Serial Mode is selected by setting V_{MODE} to a logic LOW. The serial interface is a 16 bit shift register made up of two words. The first word is the address or channel word, which uses only 1 of 8 bits to select the channel that will be programmed. The second 8 bit word is the Gain (or attenuation) word, which uses 6 bits to control the DSA state and one bit to enable or disable the channel.

When serial programming is used, all of the other parallel control input pins (3, 6-10, 25, 31, 32) can be left floating.

Table 8. 8-Bit SPI Address (Channel) Word Sequence

Data Bit	Symbol
A7	Not Used
A6	Not Used
A5	Not Used
A4	Not Used
A3	Not Used
A2	Not Used
A1	Not Used
A0	Channel Selection

Table 9. Truth Table for Address (Channel) Control Word

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	Program Channel
0	0	0	0	0	0	0	0	A
0	0	0	0	0	0	0	1	B

Table 10. 8-Bit SPI Gain (Attenuation) Word Sequence

Data Bit	Symbol
D7	Enable Bit
D6	Attenuation 16 dB Control Bit
D5	Attenuation 8 dB Control Bit
D4	Attenuation 4 dB Control Bit
D3	Attenuation 2 dB Control Bit
D2	Attenuation 1 dB Control Bit
D1	Attenuation 0.5 dB Control Bit
D0	Not Used

Table 11. Truth Table for Serial Gain (Attenuation) Control Word

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Gain Setting Target (dB)	Attenuation (dB)
E	0	0	0	0	0	0	0	20	0
E	0	0	0	0	0	1	0	19.5	0.5
E	0	0	0	0	1	0	0	19	1
E	0	0	0	1	0	0	0	18	2
E	0	0	1	0	0	0	0	16	4
E	0	1	0	0	0	0	0	12	8
E	1	0	0	0	0	0	0	4	16
E	1	1	1	1	1	1	0	-11.5	31.5

[a] To enable the specified channel set E to a logic HIGH. To disable (or set for standby) the specific channel set E for logic LOW. For this bit to work properly the standby pins (19, 22) must be floating or set to logic HIGH.

In the Serial Mode, the F1240 is programmed via the serial port on the rising edge of Chip Select bar (CSb). It is required that CSb be kept logic LOW until all data bits are clocked into the shift registers. The F1240 will change attenuation state after the data word is latched into the active register. Refer to Figure 42.

Figure 42. Serial Register Timing Diagram

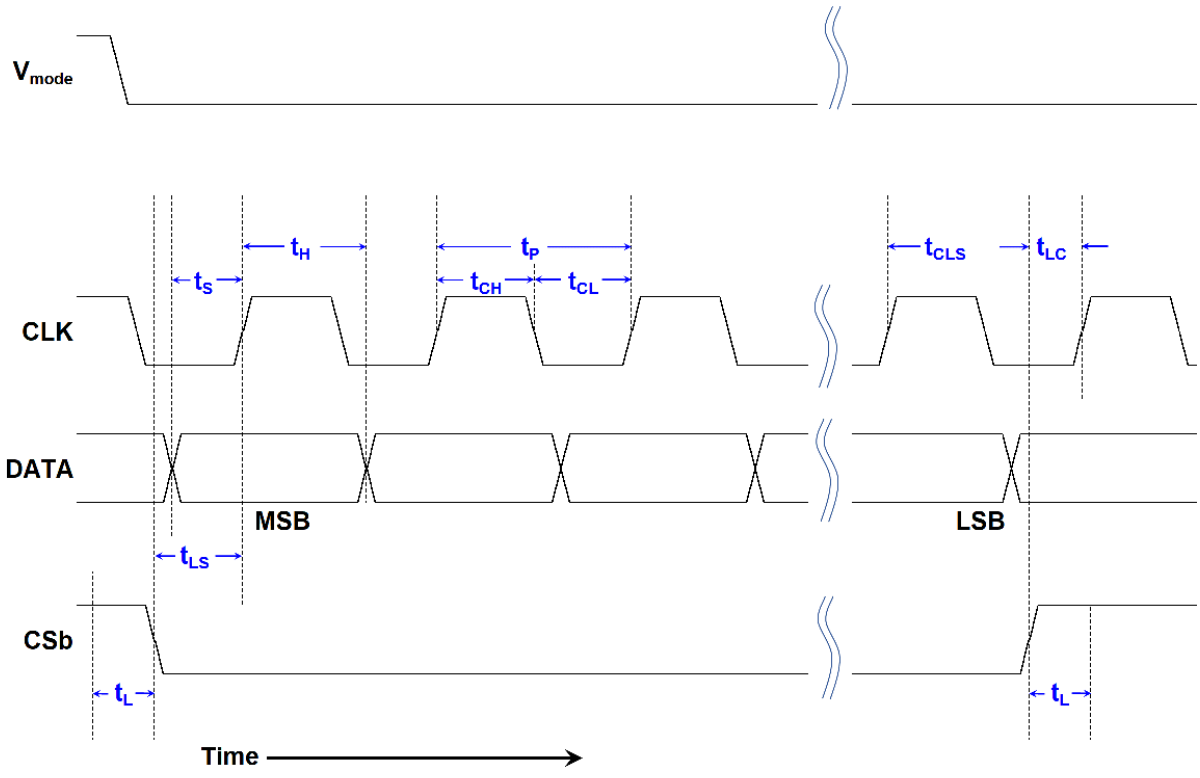


Table 12. SPI Timing Diagram Values for the Serial Mode

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
CLK Frequency	f_C			20	50	MHz
CLK HIGH Duration Time	t_{CH}		20			ns
CLK LOW Duration Time	t_{CL}		20			ns
DATA to CLK Setup Time	t_S		10			ns
CLK Period [b]	t_P		40			ns
CLK to Data Hold Time	t_H		10			ns
Final CLK Rising Edge to LE Rising Edge	t_{CLS}		10			ns
LE to CLK Setup Time	t_{LS}		10			ns
LE Trigger Pulse Width	t_L		10			ns
LE Trigger to CLK Setup Time [c]	t_{LC}		10			ns

[a] $(t_{CH} + t_{CL}) \geq 1/f_C$.

[b] Once all desired data has been clocked in, CSb must transition from LOW to HIGH after the minimum setup time t_{LC} and before any further CLK signals.

Serial Mode Enable Functions and Standby Pins

There are two pins, STBY_A (pin 22) and STBY_B (pin 19) which can be used in the serial or parallel mode for fast switching of the two channels. These pins float HIGH and should be left disconnected or set for logic HIGH for serial operation.

Using the Serial Mode for Standby

- Each channel must be programmed separately using the Enable bit (Bit 7) of the Data word.
- The gain setting is determined by the gain bits (D6-D1) are set for during the channel programming.

Parallel Control Mode

Parallel Mode is selected when V_{MODE} (Pin 4) is floating or set to a logic HIGH. In this mode, the device will immediately react to any voltage changes on the parallel control pins (1-3, 5-10, 16, 25, 31, 32). Use the Parallel Mode for the fastest settling time. This also allows both channels to be programmed simultaneously.

The truth table for the Parallel Mode is identical for bits D6 to D0 as shown in the Serial Mode truth table; see Table 11.

Using the Standby Pins for Standby

- Both channels can be switch at the same time by setting the standby pins simultaneously
- The gain setting is determined by the gain bits (D6-D1) set during the last serial programming or by the existing parallel pins setting.

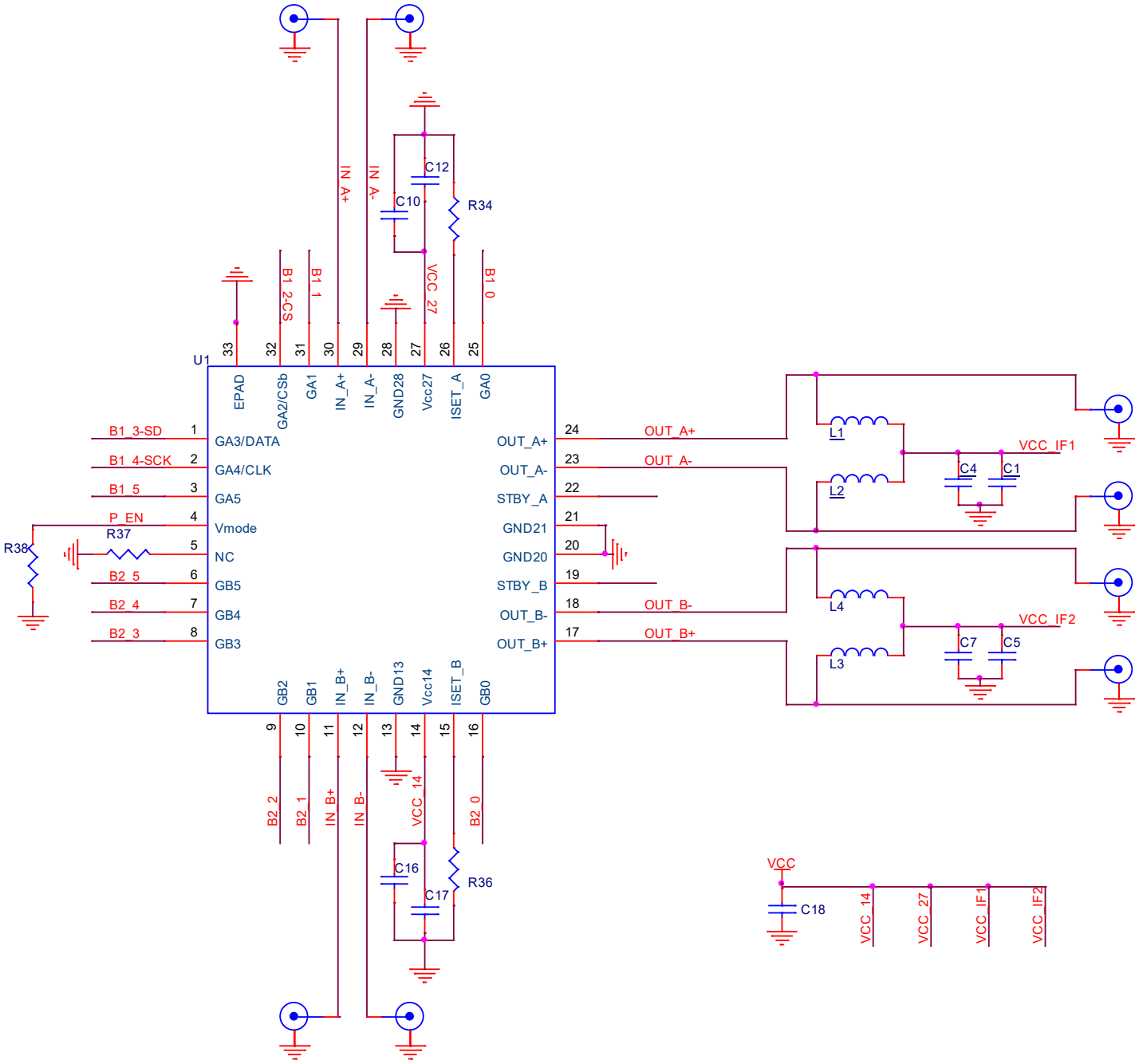
Default Startup Condition

When the device is first powered up, it will default to the maximum gain (minimum attenuation) of 20 dB (0 dB) and both channels will be enabled independent of the V_{MODE} and parallel pin [D6:D0] conditions.

Typical Application Circuit

Figure 43 is a typical minimum circuit design needed for the F1240.

Figure 43. Electrical Schematic



Evaluation Kit Picture

Figure 44. Top View

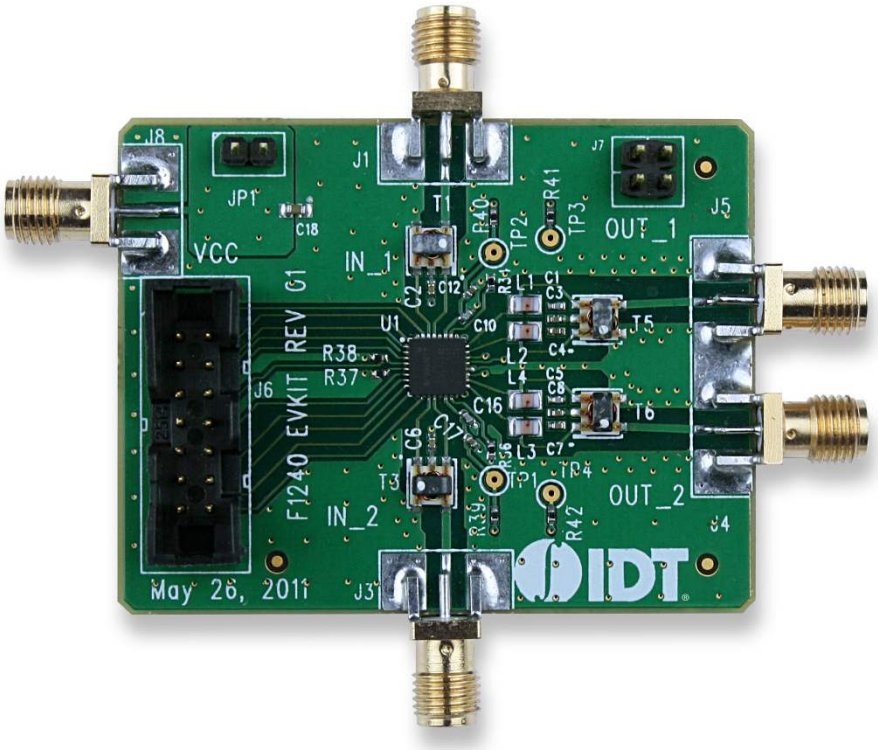
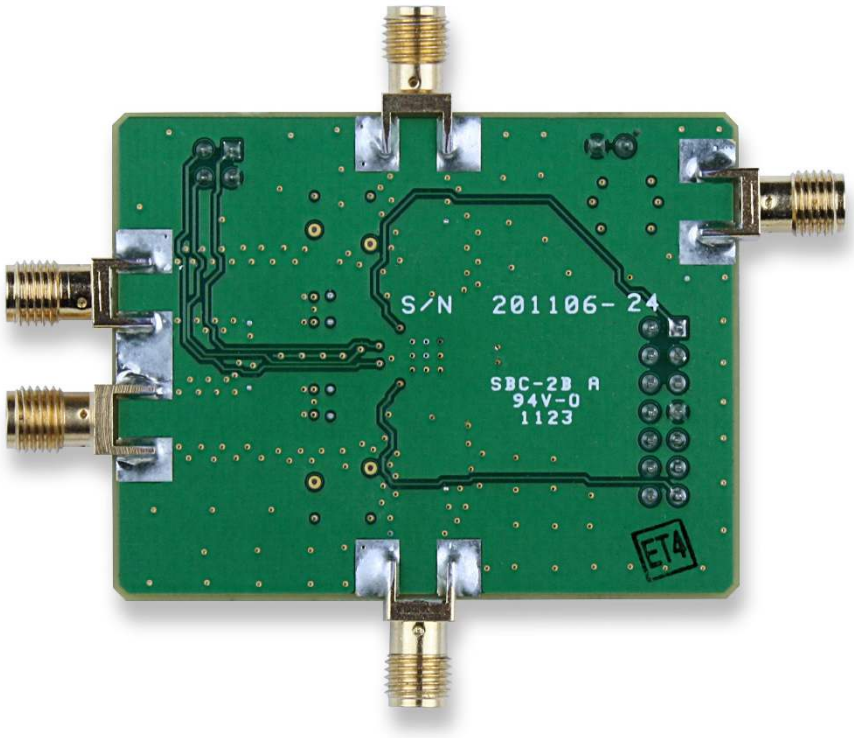


Figure 45. Bottom View



Evaluation Kit / Applications Circuit

Figure 46 shows the electrical schematic for the evaluation board used for customer evaluation.

Figure 46. Electrical Schematic

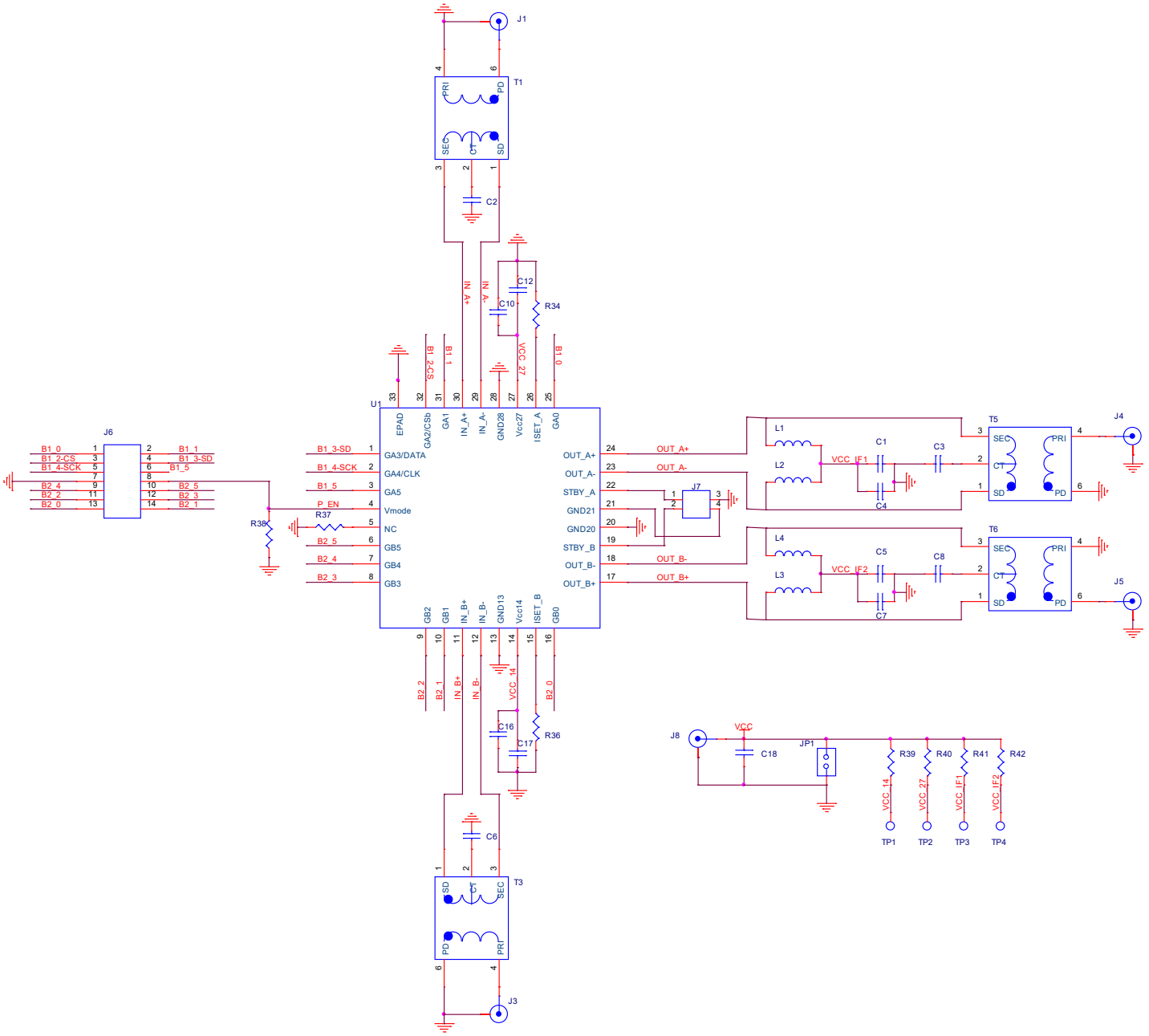


Table 13. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1, C5, C10, C16	4	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
C2, C3, C6 C,8	4	10nF ±5%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H103J	MURATA
C4, C7, C12, C17	4	100nF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	MURATA
C18	1	10uF ±20%, 6.3V, X5R Ceramic Capacitor (0603)	GRM188R60J106M	MURATA
R37, R39, R40, R41, R42	5	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
R34, R36	2	3.83kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3831X	PANASONIC
JP1	1	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
J7	1	CONN HEADER VERT DBL 2 X 2 POS GOLD	90131-0762	Molex
J6	1	CONN HEADER VERT DBL 7 X 2 POS GOLD	N2514-6002-RB	3M
J1, J3, J4, J5, J8	5	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
L1, L2, L3, L4	4	390nH ±5%, 0.290A, Ferrite Ceramic Chip Inductor (0805)	0805CS-391XJL	CoilCraft
T1, T3, T5, T6	4	3MHz - 800MHz 50Ω, RF Transformer (4:1)	TC4-1WG2+	Mini Circuits
U1	1	VGA	F1240	IDT
	1	Printed Circuit Board	F1240 EVKIT REV 01	IDT

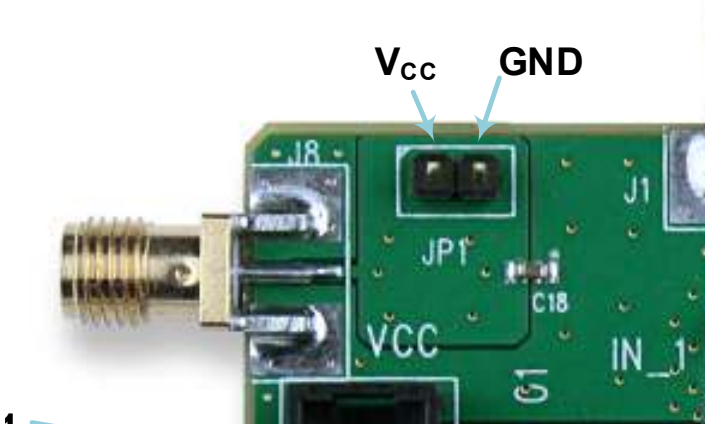
Evaluation Kit Operation

Power Supply Setup

Set up a power supply in the voltage range of 4.75V to 5.25V with the power supply output disabled. The voltage can be applied via one of the following connections (see Figure 47).

- Directly to J8 connector
- JP1 header connection (note the polarity of the GND pin on this connector)

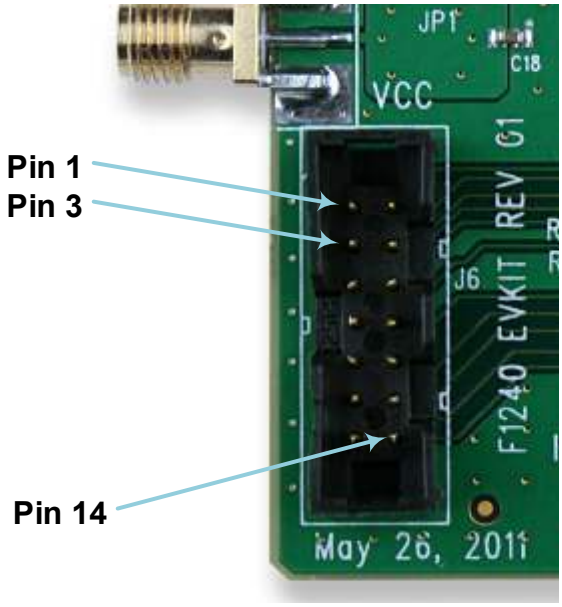
Figure 47. Power Supply Connections



Logic Control Setup

The Evaluation Board has the ability to control the F1240 in the Parallel or Serial Mode. The logic voltages can be applied through the J4 connector (see Figure 48). For both the parallel and serial mode see Table 14 for the connections.

Figure 48. Logic Connections



Logic Control

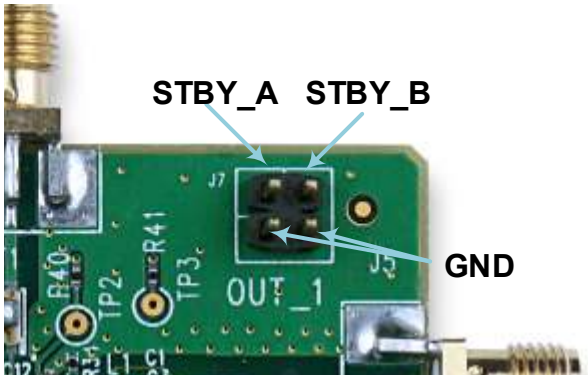
Table 14. Parallel and Serial Logic Pins

J6 Pin	Parallel Function	Serial Function	F1240 Pin
1	GA0	Not used	25
2	GA1	Not used	31
3	GA2	CSb	32
4	GA3	DATA	1
5	GA4	CLK	2
6	GA5	Not used	3
7	GND	GND	
8	V_{MODE}	V_{MODE}	4
9	GB4	Not used	7
10	GB5	Not used	6
11	GB2	Not used	9
12	GB3	Not used	8
13	GB0	Not used	16
14	GB1	Not used	10

Standby Pins

The evaluation board allows for setting the standby pins on connector J5. By default the standby pins are logic HIGH which allows the device to be enable. By setting the pin to logic LOW (ground) the device will not draw very little current.

Figure 49. Standby Pins



Power-On Procedure

1. Set up the voltage supplies and Evaluation Board as described in the “Power Supply Setup” section and the “Logic Control Setup” section above.
2. Enable the V_{CC} supply. The F1240 should default to the maximum gain state.
3. Enable the proper gain (attenuation) setting according to Table 7-10 for Serial Mode or Table 11 for the Parallel Mode.

Power-Off Procedure

1. Set the logic control pins to a logic LOW.
2. Disable the V_{CC} supply.

Application Information

The F1240 has been optimized for use in high performance IF sub-sampling applications. High absolute attenuator accuracy and low switching time make the F1240 ideal for these very demanding applications.

Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Digital Pin Voltage and Resistance Values

Table 15 provides open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

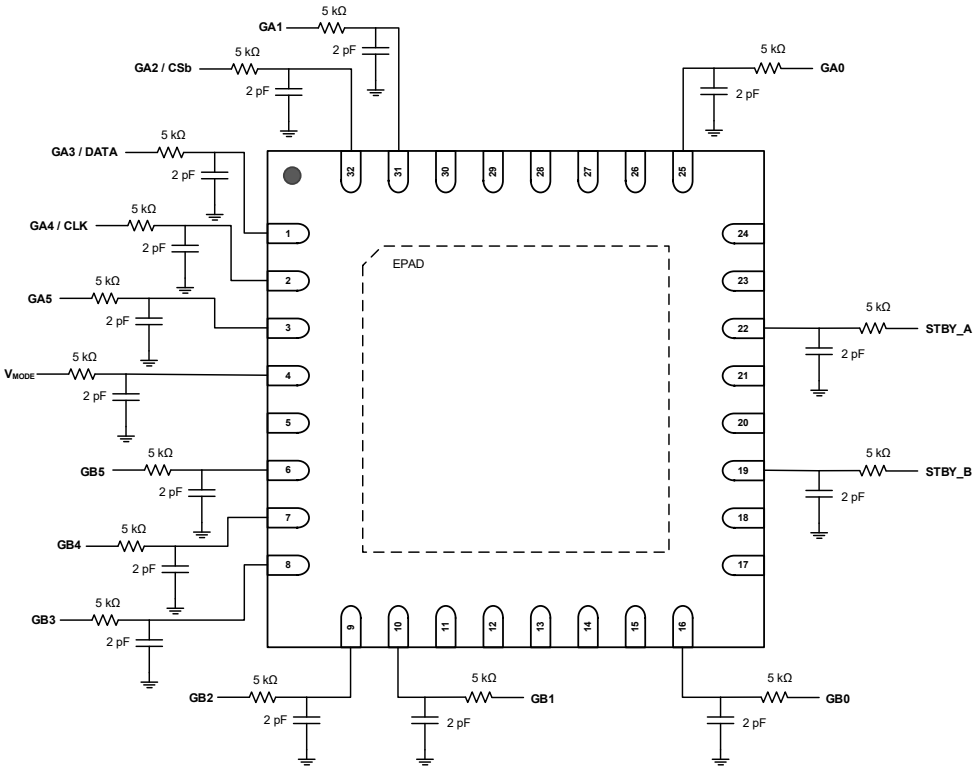
Table 15. Digital Pin Voltages and Resistance

Pin	Name	Open Circuit DC Voltage	Internal Connection
1 - 3, 6 - 10, 16, 25, 31, 32	Gain Control Bits	0V	> 10MΩ
4	V_{MODE}	V_{CC}	1.8MΩ
19, 22	STBY_B, STB_A	V_{CC}	.80MΩ

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 1 - 4, 6 - 10, 16, 19, 22, 25, 31, and 32 as shown below.

Figure 50. Signal Integrity Schematic



Matched Output

Unlike competing devices the F1240 features a matched 200Ω differential output. All of the datasheet parameters are specified as such. For instance, the Gain of 20dB is a true Transducer Power gain (Power delivered to the matched load minus Power available from the source). This is in contrast to competing devices that usually have a high or low impedance output and must be terminated with resistors to operate properly. In IF sampling applications, the IF VGA usually drives a bandpass anti-alias filter which precedes the ADC. These filters typically need to 'see' matched terminations. Only the F1240's performance is preserved in this environment. See directly below for a comparison to popular VGA styles.

Figure 51. VGA Output Amplifier - Voltage Mode Schematic

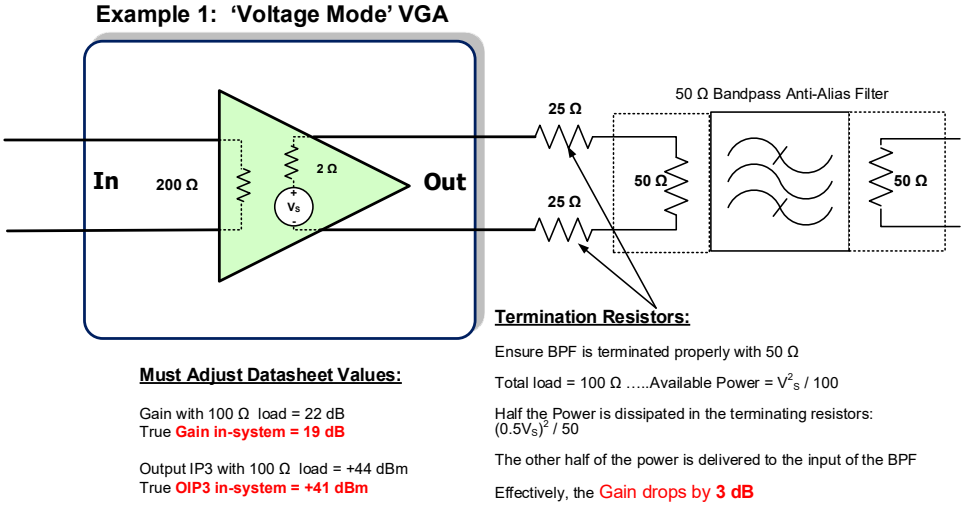


Figure 52. VGA Output Amplifier - Current Mode Schematic

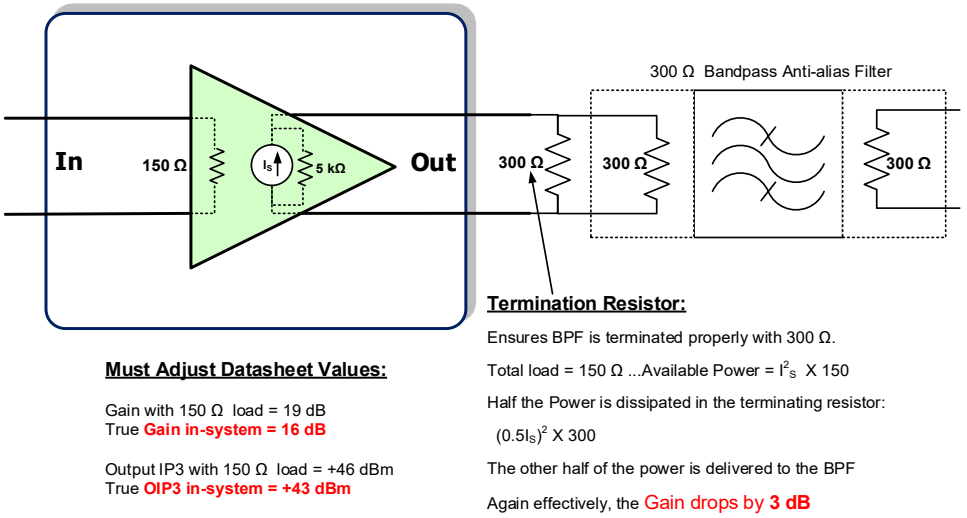
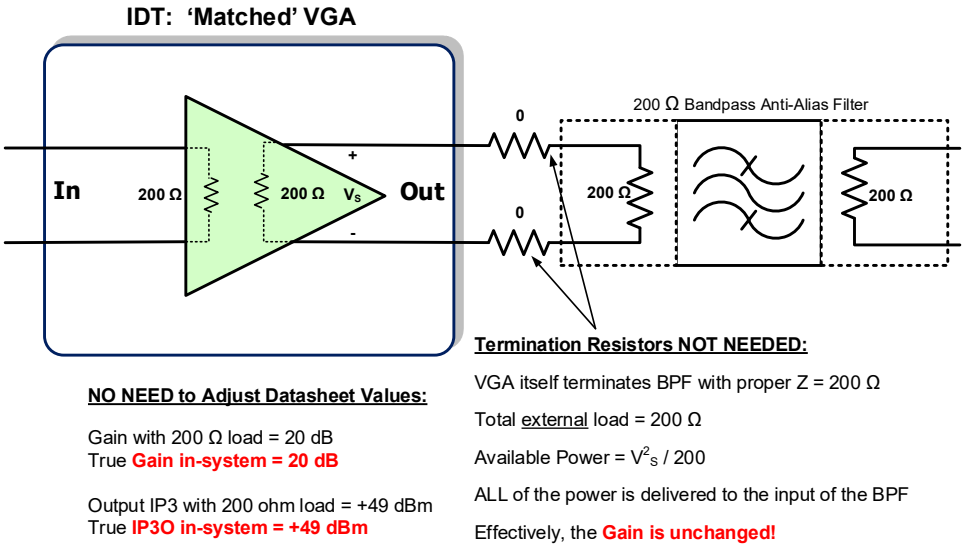


Figure 53. VGA Output Amplifier - Matched Output Schematic

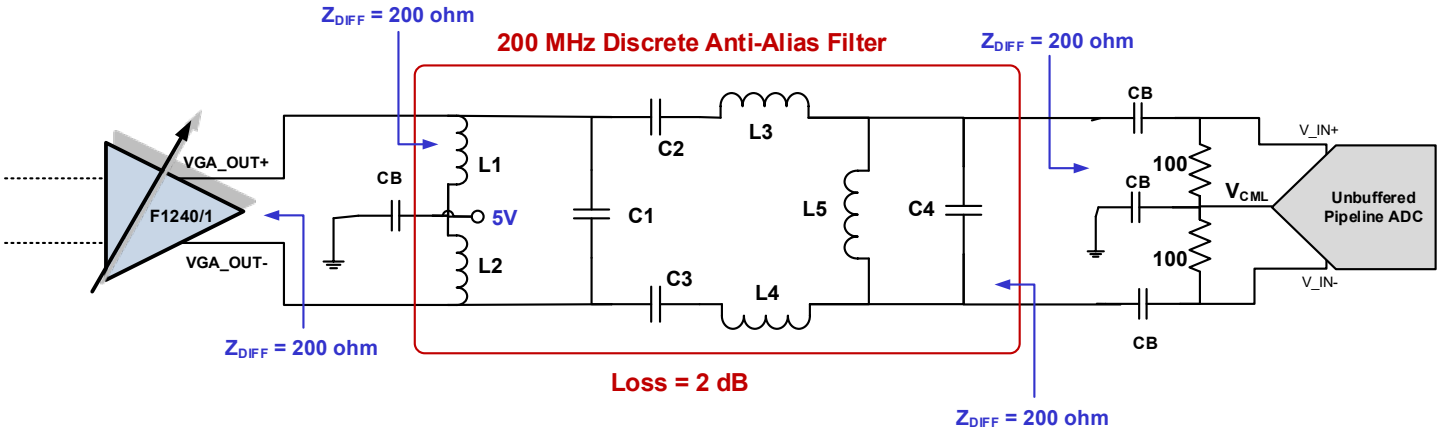


Noise Contour

The remarkable *FlatNoise™* feature of the device (see first four graphs on page 10) has great benefits when implemented in wideband multi-carrier systems. For the first 13 dB of attenuation range, the device has only 2.3dB degradation in noise figure. This is in stark contrast to standard VGAs like the voltage or current mode devices described earlier. These devices have a linear dB-for-dB degradation in Noise Figure with increasing attenuation.

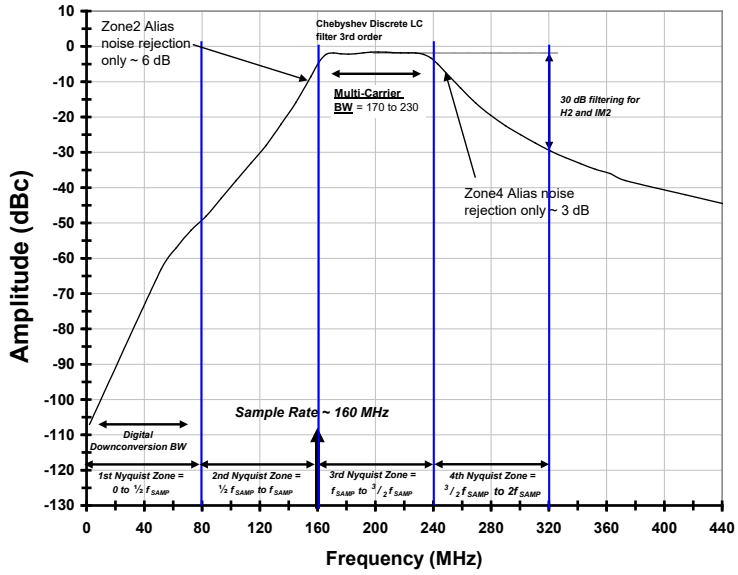
Refer to the figure below. It depicts the F1240 driving a matched Anti-Alias Filter which is followed by an ADC with a differential resistive 200 ohm termination. Note that at each point in the system the matching is preserved.

Figure 54. VGA Output Amplifier – Anti-Alias Filter Schematic



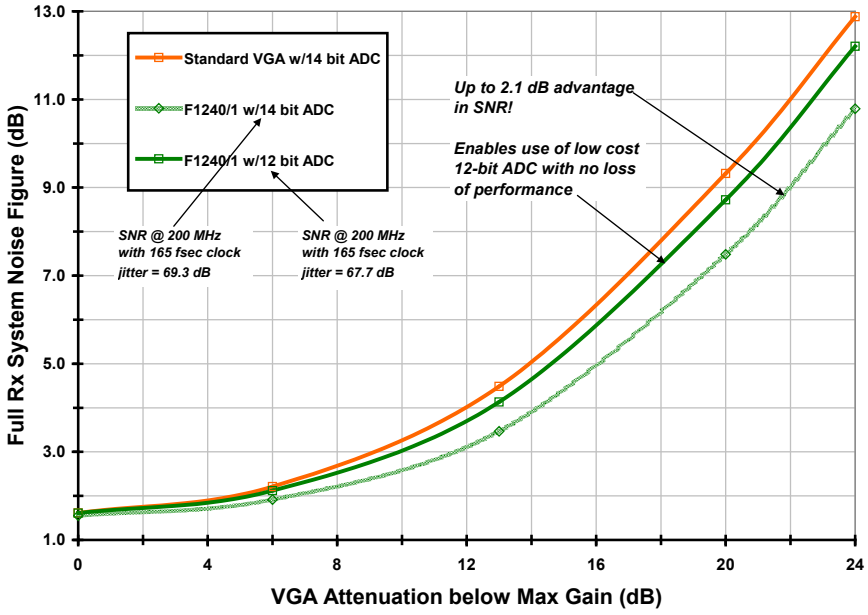
A discrete realization of a 3rd order Anti-Alias filter is shown below. Sampling occurs in Nyquist Zone3 for a 60 MHz multi-carrier signal. Noise just 20 MHz above and below the signal band edges will alias from either Zone4 or Zone2 and show up as added noise in the desired band at the digital output of the ADC.

Figure 55. VGA Output Amplifier – Anti-Alias Filter Schematic



The result is that the F1240 with its unique noise contour will improve SNR significantly in this multi-carrier instance. Note in the graph below: SNR improves over 2dB at high attenuation settings which potentially allows for the use of a lower cost 12-bit ADC in the Rx path.

Figure 56. VGA Output Amplifier – Anti-Alias Filter Schematic



Current Setting Resistors

The F1240 already offers the best IM3 distortion performance over the widest power range when driving a matched load with 160mA total current for both channel. The user has the option to reduce the current even further at the expense of Output IP3.

Settling Time

The F1240 has been optimized to settle quickly and smoothly without any glitching when changing gain between ANY adjacent steps. Glitching is defined as the power increase over the maximum power from either of the two states being switched. Most states show no glitching at all. A few states have less than 0.4dB. Only one state was found with a 1.5 dB glitch. See Figure 40 and Figure 41 glitch Even for 1 dB steps that involve MSB transitions, the settling time is less than 15 ns.

Gain Control Software

To control the F1240, IDT can supply a total solution, F1240EVS, to test the device. The software can be downloaded from RF Digital Control Software Installer, and the user manual from AN-896 RF Products EVS Digital Control Software Guide.

Operation into a 100Ω Load

The F1240 can be dropped directly into a 100Ω termination environment without any topology changes, so no board redesign is necessary. The example schematic below is for a 153MHz IF center frequency. Simply replace the pullup inductors already on the board with 91nH and replace the series AC coupling capacitors already on the board with 18pF. The F1240 in this case will then drive a 100Ω filter with approximately 16dB return loss. See schematic and measured results when matched to 100Ω below.

Figure 57. 153MHz Output Filter to ADC Schematic

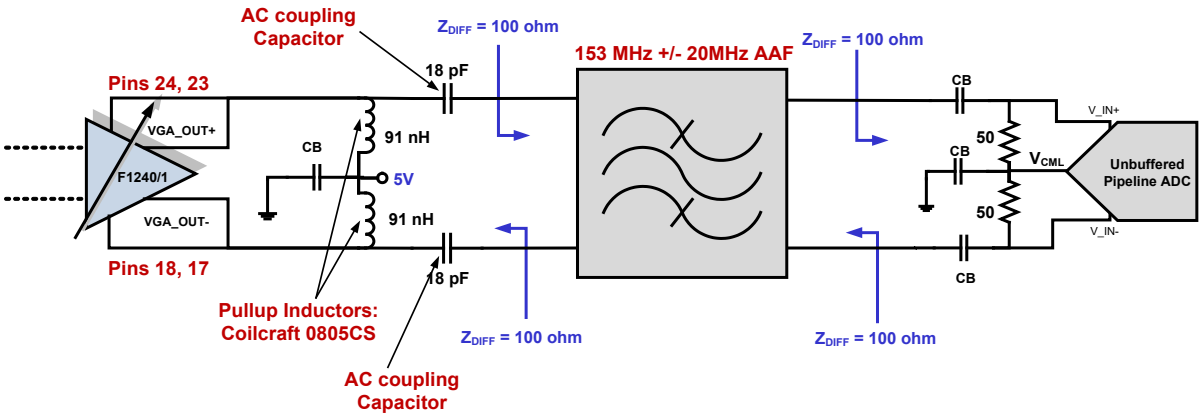


Figure 58. Measure Performance for 153MHz Output Filter vs Frequency

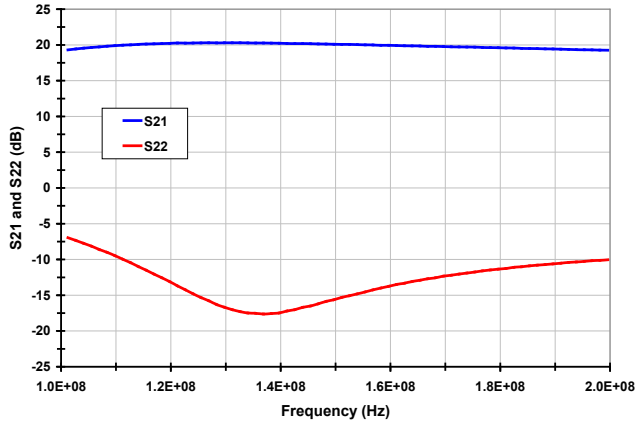


Figure 59. Measure OIP3 Performance for 153MHz Output Filter vs Gain Setting

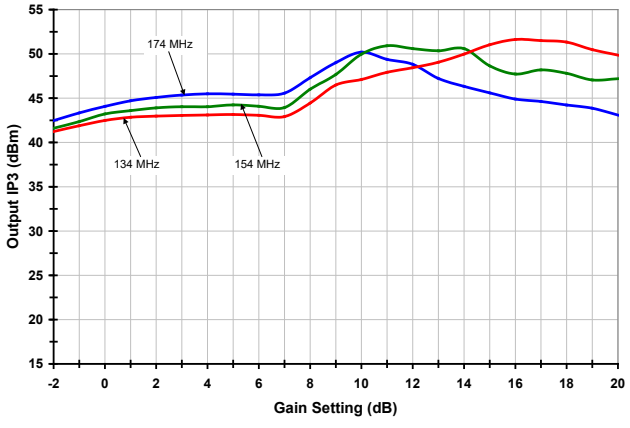


Figure 60. Measured Harmonic Performance for 153MHz Output Filter vs Gain Setting

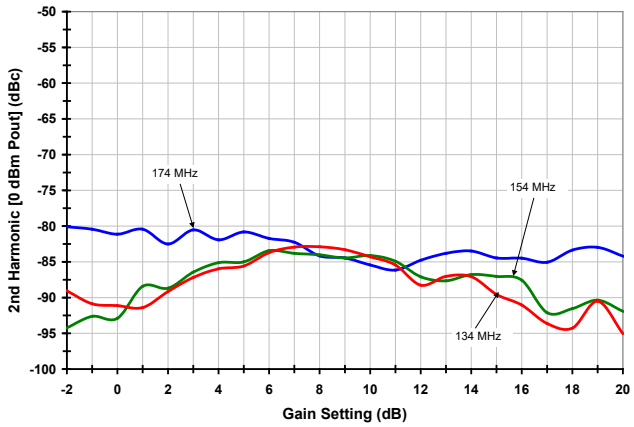
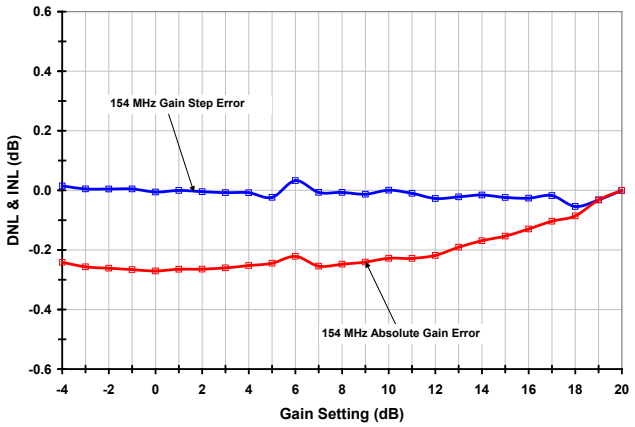


Figure 61. Measure Error Performance for 153MHz Output Filter vs Gain Setting



Package Outline Drawings

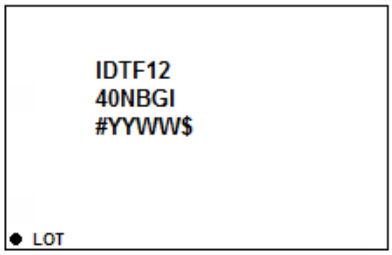
The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nbnbg32-package-outline-50-x-50-mm-body-epad-330mm-sq-050-mm-pitch-qfn

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F1240NBGI	5 × 5 × 0.75 mm 32-QFN	1	Tray	-40° to +100°C
F1240NBGI8	5 × 5 × 0.75 mm 32-QFN	1	Reel	-40° to +100°C
F1240EVBI	Evaluation Board			
F1240EVS	Evaluation Solution			

Marking Diagram

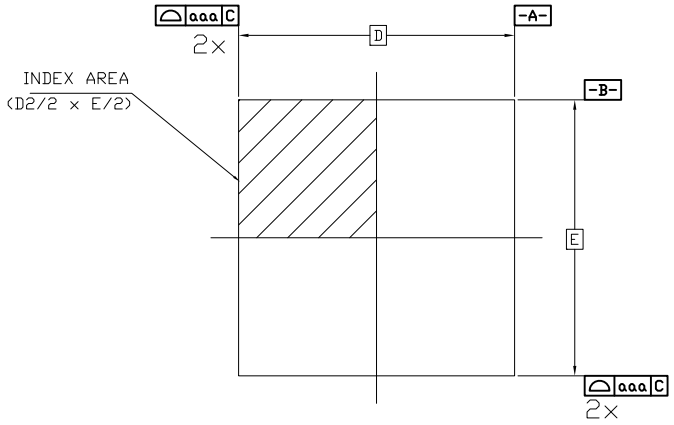


- Lines 1 and 2 are the part number.
- Line 3 indicates the following:
  - "#" denotes stepping.
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.
- Line 4 is the assembly lot number.

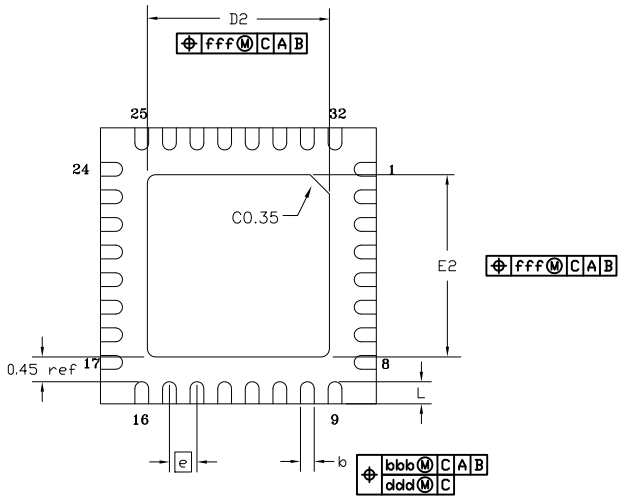
Revision History

Revision Date	Description of Change
September 11, 2018	• Added spurs specification • Linked the package outline drawings • Updated the marking diagram • Updated the document formatting
February 9, 2018	Added power supply and control pin paragraphs in Application section. Corrected Absolute Maximum Rating section. Corrected pin table. Addition of “Revision History” table. Addition of contacts and disclaimer table. Revision of package drawing and addition of land pattern. Minor edits.
March 31, 2012	Initial release.

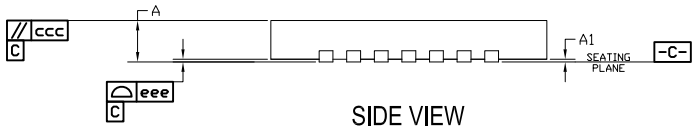
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	DIMENSION		
	MIN	NOM	MAX
L	0.30	0.40	0.50
D		5.00 BSC	
E		5.00 BSC	
D2	3.20	3.30	3.40
E2	3.20	3.30	3.40
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

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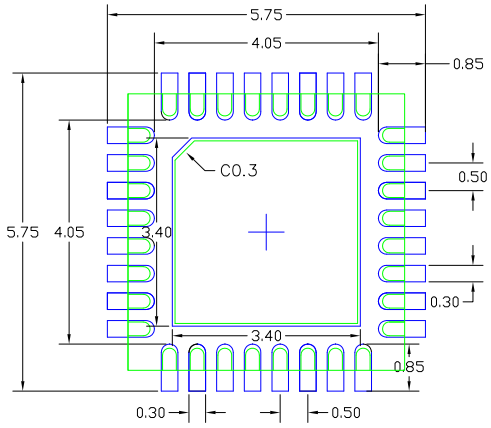
APPROVALS DATE DRAWN RAC 5/11/16 CHECKED	TITLE NB/NBG32 PACKAGE OUTLINE 5.0 x 5.0 mm BODY, EPAD 3.30mm SQ 0.50 mm PITCH QFN
	SIZE C · DRAWING No. PSC–4348–02 · REV 00
	DO NOT SCALE DRAWING · SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

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CHECKED			
		SIZE C / DRAWING No. PSC-4348-02	REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

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