6A, 23V, 500kHz, ACOT® Synchronous Buck Converter

General Description

The RT6230 is a synchronous Buck converter with Advanced Constant On-Time (ACOT®) mode control, which provides a very fast transient response with no external compensators. The RT6230 operates from 6V to 23V input voltage, and provides complete protection functions including over-current protection (OCP), under-voltage protection (UVP) and over-voltage protection (OVP). This IC also provides a 1.5ms internal soft-start function and an open-drain power good indicator.

Ordering Information

RT6230□□□

- Package Type
  QUF : UQFN-16L 3x3 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- PWM Operation / VOUT Protection
  A: Automatic PSM/Latch
  AH: Automatic PSM/Hiccup
  BL: Forced PWM/Latch
  BH: Forced PWM/ Hiccup

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

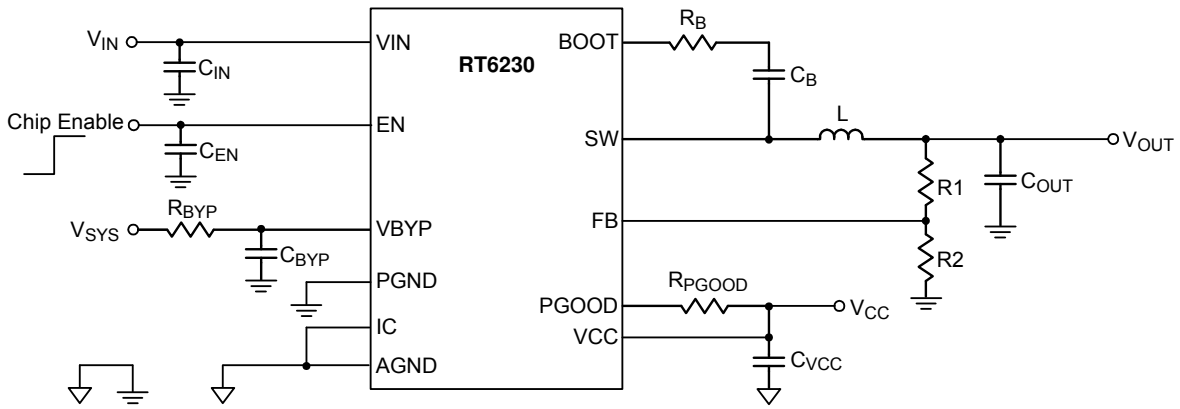
Features

- **6V to 23V Input Voltage Range**
- **Adjustable from 5V to 12V Output Range**
- **500kHz Switching Frequency**
- **ACOT® Mode Performs Fast Transient Response**
- **Integrated MOSFETs**
  - **31mΩ of High-Side MOSFET**
  - **20mΩ of Low-Side MOSFET**
- **Supports MLCC Output Capacitors**
- **Internal Soft-Start (1.5ms typ)**
- **Built-in OVP/UVP/OCP**
- **Power Good Indicator**
- **Thermal Shutdown**

Applications

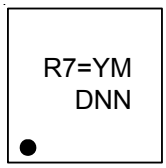
- Laptop Computers
- Tablet PCs
- Networking Systems
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

Simplified Application Circuit



Marking Information

RT6230AGQUF



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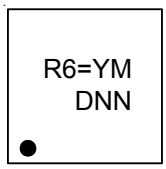
RT6230AHGQUF



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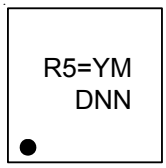
RT6230BHGQUF



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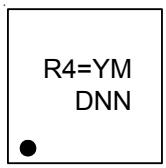
RT6230BLGQUF



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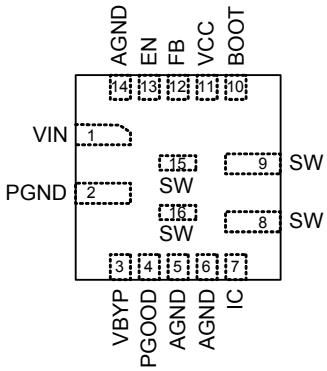
Pin Configuration

(TOP VIEW)

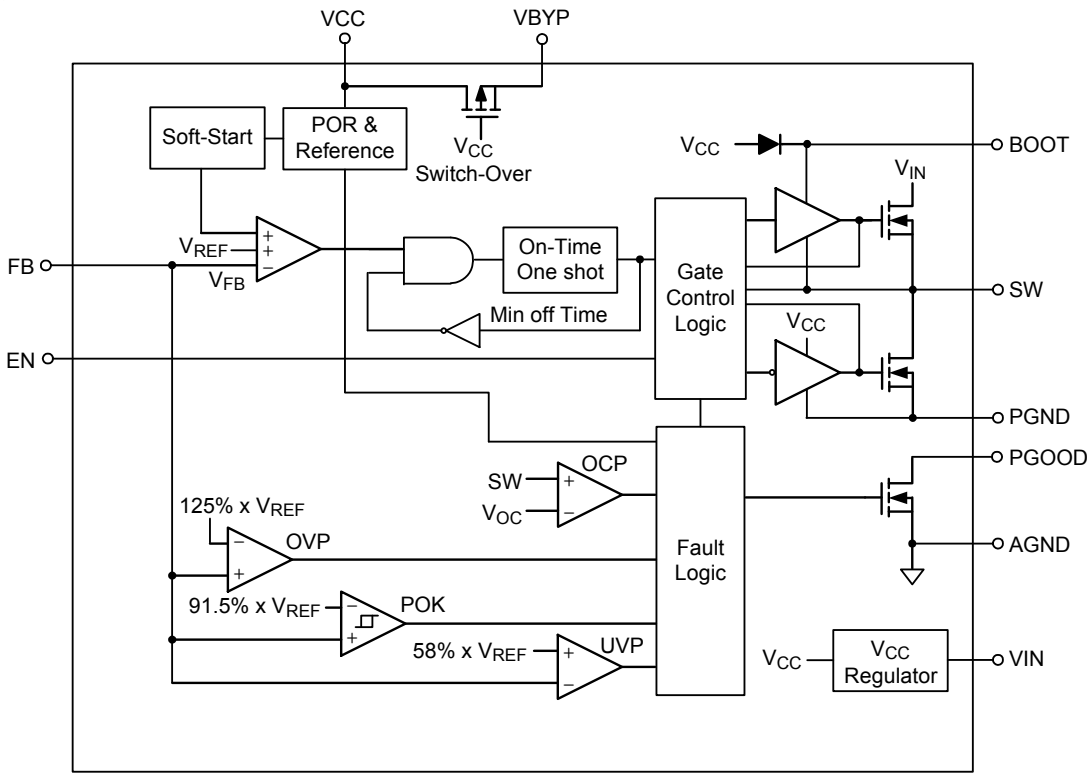


UQFN-16L 3x3 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Connect power input to high-side MOSFET drain. Place 2pcs 10μF MLCC decoupling capacitors near input pin.
2	PGND	Power ground. Connect power ground pin with wide and thick trace, adding thermal vias for better heat dissipation.
3	VBYP	Switch over input supply voltage for V_{CC}. A low pass filter should be connected to AGND if V_{BYP} is applied. The recommended RC filter value is R_{BYP} = 5.1Ω and C_{BYP} = 2.2μF. If V_{BYP} is not used, then connect this pin to AGND. Do not connect to VCC pin.
4	PGOOD	Open-drain power good indicator output. This pin should be connected to a pull high voltage with a 100kΩ resistor.
5, 6, 14	AGND	Analog ground.
7	IC	Internally connected. Connect this pin to PGND or AGND and “DO NOT” connect this pin to any of the circuit connections.
8, 9, 15, 16	SW	Switch node.
10	BOOT	Bootstrap supply for high-side gate driver. A capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BOOT pins to form a floating supply across the power switch driver. The recommended design value is R_{BOOT} = 2.2Ω and C_{BOOT} = 0.1μF.
11	VCC	5V linear regulator output for internal control circuit. Bypass V_{CC} to AGND with a 2.2μF capacitor. V_{CC} can only supply internal circuits. Do not connect to external loads.
12	FB	Feedback voltage input.
13	EN	Enable control input. Do not leave this pin floating. The slew rate of EN is recommended to be slower than 4.8V/μs. Users should add a RC circuit to avoid the glitch signal.

Functional Block Diagram



Operation

The RT6230 is high-performance 500kHz 6A step-down regulators with internal power switches and synchronous rectifiers. It features an Advanced Constant On-Time (ACOT®) control architecture that provides stable operation for ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 6V to 23V, and the output voltage is adjustable from 5V to 12V.

ACOT® (Advanced COT) Control Mechanism

The RT6230 adopts ACOT® control mechanism. In order to achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors. However, making the on-time proportional to VOUT and inversely proportional to VIN is not sufficient to achieve good constant-frequency behavior for following reasons. The voltage drops across MOSFET and inductor make equivalent conversion ratio to be smaller than ideal duty ratio. That is, the switching frequency is not fixed at different output load conditions. Frequency is increasing at higher loading and junction temperature as compared to smaller loading and junction temperature.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. The ACOT® uses the frequency locked loop, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

The RT6230 control algorithm is simple to understand as depicted in Figure 1. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage, V_{REF}. When the combined signal is less than the reference, the on-time one-shot is triggered as long as

the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

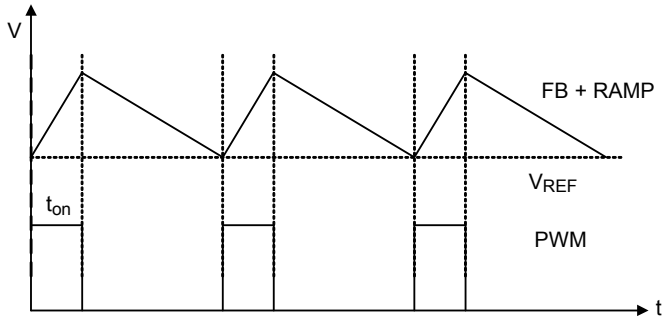


Figure 1. ACOT® PWM Control Diagram

DEM (Diode Emulation Mode) at Light Load

In diode emulation mode, the RT6230A/AH automatically reduces switching frequency at light load conditions to maintain high efficiency. The reduction of frequency is achieved smoothly. As the output current decreases from heavy load conditions, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. Contrarily, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point between DEM and CCM operation is shown in Figure 2 and can be calculated as follows :

$$I_{LOAD} = \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

, where t_{ON} is the on-time of high-side MOSFET.

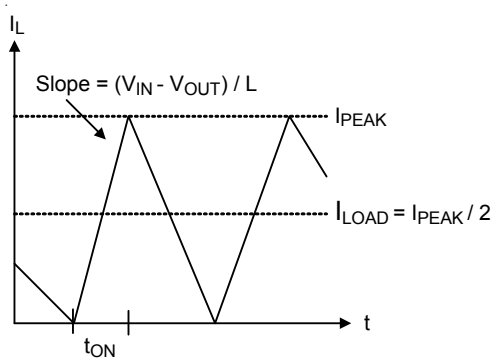


Figure 2. Boundary Condition of CCM/DEM

The switching frequency in DEM can be calculated as follows :

$$f_{SW}(I_{LOAD}) = \frac{2LI_{LOAD}}{V_{IN}t^2_{ON}\left(\frac{V_{IN}}{V_{OUT}} - 1\right)}$$

, where I_{LOAD} is smaller than I_{LOAD_BCM}.

As can be observed in the equation, switching frequency is a function of output load current, I_{LOAD}, and it is proportional to I_{LOAD}, which means it becomes higher at heavy load and reduces to almost zero at a very light load. Besides, inductor selection can also change the switching frequency in DEM. Choosing large inductance makes more switching loss as compared to small inductance. However, the core loss of inductor increases with larger inductor current ripple for a given inductor. That is, proper selection of inductor based on efficiency target is important.

Moreover, in order to achieve smooth transition from DEM to CCM or backward, during discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially. The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for preset switching frequency and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and

discontinuous switching.

FCCM (Forced Continuous Conduction Mode) at Light Load

Unlike diode emulation mode (DEM) that enables zero current detection (ZDC) to reject negative inductor current during low-side MOSFET turns on. For RT6230BL/BH, the inductor current can be negative until next on-time is generated in FCCM. The switching frequency is fixed from no load to full load. Therefore, benefits like better transient response from light load to heavy load and smaller EMI/EMC come along with FCCM. Nevertheless, poor efficiency in light load is a tradeoff.

Power On / Power Off

The RT6230 can be powered on by EN when VCC LDO is above UVLO threshold as specified in electrical table. When V_{EN} exceeds its logic-high level (1.35V typical), the IC is fully operational. The RT6230 provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramp of internal reference voltage which is compared with FB signal. And it will correct the output voltage more accurately after soft-start. The typical soft-start duration is 1.5ms.

On the other hand, the enable input (EN) has a logic-low level of 1.15V. When V_{EN} is below the logic-low level, the IC enters shutdown mode and supply current drops to less than 5μA (typical). The PWM stops switching and the output capacitors are discharged through output load or feedback resistors.

Power Good Indicator

The power good is an open-drain indicator to inform the status of VOUT for system and it requires a pull-up resistor connected to a pull-up voltage source. Generally, the open-drain control signal is held high after VCC POR and the power good keeps low until VOUT ramps up over 90% of VOUT setting for a de-glitch time of 500μs ($t_{PGDLY\_LowtoHigh}$). The status of power good is based on VOUT threshold as specified in electrical table. The power good is high only as VOUT is within the power good design range. Moreover, in order to prevent VOUT glitches that induce wrong power good status during VOUT transient state, there is a blanking time about 2μs ($t_{PGDLY\_HightoLow}$) for power good to transit from high to low.

Output Over-Current Protection (OCP)

In order to prevent excessive heat on chip which may induce catastrophic damage, the RT6230 implements an output OCP mechanism. The current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between Source and Drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the current limit, the on-time one-shot is inhibited until the inductor current ramps down below the current limit. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If VOUT drops below the output under-voltage protection level (see next section), the IC will stop switching to avoid excessive heat.

Output Over-Voltage Protection (OVP)

In order to prevent abnormal output high voltage which may induce catastrophic damage on chip, the RT6230 features an output OVP mechanism. For the RT6230A and the RT6230BL, if the output voltage rises above the regulation level for longer than 5us(typical), the IC stops switching and is latched off. On the other hand, for the RT6230AH and the RT6230BH, the IC will stop switching and restart automatically after a short period (about 2.5ms) which is the so-called Hiccup mode. To restart operation from latch off, toggle EN or power the IC off and then turn on again.

Output Under-Voltage Protection (UVP)

In order to prevent the IC from over-heating because of output voltage has been clamped by OCP, the RT6230 features an output UVP mechanism. If the output voltage drops below the UVP trip threshold for longer than 5μs (typical), the UVP is triggered, and the IC turns on low-side MOSFET to discharge the inductor current until ZCD and then shuts down. Likewise, for the RT6230A and the RT6230BL, the IC stops switching and is latched off. On the other hand, for the RT6230AH and the RT6230BH, the

IC will stop switching and enter the Hiccup mode. To restart operation from latch off, toggle EN or power the IC off and then turn on again.

Input Under-Voltage Lockout (UVLO)

In addition to the enable function, the RT6230 features an UVLO function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Over-Temperature Protection (OTP)

The RT6230 features an OTP circuitry to prevent overheating due to excessive power dissipation. The OTP shuts down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 25°C the IC resumes normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C. Note that the VCC regulator remains on as the OTP is triggered.

Absolute Maximum Ratings (Note 1)

- VIN to PGND ---------- –0.3V to 27V
- SW to PGND
  - DC ---------- –1V to 27.3V
  - AC (<30ns) ---------- –5V to 28V
- BOOT to PGND
  - DC ---------- –0.6V to 33.3V
  - AC (<30ns) ---------- –5V to 34V
- BOOT to SW ---------- –0.3V to 6V
- EN, FB to AGND ---------- –0.3V to 27V
- VBYP to AGND ---------- –0.3V to 5.3V
- VCC, PGOOD, IC to AGND ---------- –0.3V to 6V
- PGND to AGND ---------- –0.3V to 0.3V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- ESD Susceptibility
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, VIN ---------- 6V to 23V
- Output Voltage ---------- 5V to 12V
- Junction Temperature Range ---------- –40°C to 150°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		UQFN-16L 3x3 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	70	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	19.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	43	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current							
Shutdown Current		V_{EN} = 0V		--	2.5	5	μA
Quiescent Current		V_{EN} = 2V, no switching	(RT6230A/AH)	--	100	130	μA
			(RT6230BL/BH)	--	110	150	
BOOT to SW Leakage Current							
BOOT to SW Leakage Current		V_{BYP} = 5V, V_{EN} = 0V		--	--	2.5	μA
Switch On-Resistance							
Switch On-Resistance	$R_{DS(ON)\_H}$	V_{BOOT} – V_{SW} = 5V		--	31	--	mΩ
	$R_{DS(ON)\_L}$			--	20	--	
High-Side MOSFET Leakage Current	$I_{Leakage\_H}$	V_{IN} = 12V, V_{EN} = 0V		--	--	1	μA
Current Limit							
Current Limit	I_{OC}	Valley current of low-side switch		7.6	--	11.4	A
Switching Frequency and Minimum Off Timer							
Switching Frequency	f_{SW}			450	500	550	kHz
Minimum Off-Time	t_{OFF_MIN}			--	200	--	ns
Protections							
OVP Trip Threshold	V_{OVP}	With respect to output voltage		120	125	130	%
OVP Propagation Delay	t_{OVPDLY}			--	5	--	μs
UVP Trip Threshold	V_{UVP}	With respect to output voltage		53	58	63	%
UVP Propagation Delay	t_{UVPDLY}			--	5	--	μs
Reference and Soft-Start							
Feedback Reference Voltage	V_{REF}			0.594	0.600	0.606	V
Soft-Start Time	t_{SS}	From EN high to PGOOD high		1	1.5	2	ms
Enable and UVLO							
EN Input High Voltage	V_{ENH}			1.25	1.35	1.45	V
EN Hysteresis	V_{ENHYS}			50	200	250	mV
EN Input Current	I_{EN}	V_{EN} = 2V		--	1	--	μA
		V_{EN} = 0V		--	0	--	
VCC UVLO Rising	V_{CCUVLO}			3.8	4.2	4.45	V
VCC UVLO Hysteresis	V_{CCHYS}			75	400	650	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Regulator						
VCC Regulator	V_{VCC}		4.805	5	5.295	V
VCC Switch Over Threshold to VBYP		V_{BYP} rising edge	4.4	4.6	4.8	V
VCC Switch Over Hysteresis			150	200	400	mV
Switch Over On-Resistance			--	3	5	Ω
Power Good Indicator						
PGOOD Threshold From Lower		V_{OUT} rising	86.5	91.5	96.5	%
PGOOD Low Hysteresis		V_{OUT} falling	--	10	--	%
PGOOD Low to High Delay	t_{PGDLY}		--	0.5	--	ms
PGOOD Sink Current Capability	V_{PGSINK}	Sink 4mA	--	--	0.4	V
PGOOD Leakage Current	I_{PGLEAK}	V_{PGOOD} = 5V	--	--	100	nA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	T_J rising	135	150	--	°C
Thermal Shutdown Hysteresis			--	25	--	°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} and θ_{JC} are measured or simulated at T_A = 25°C based on the JEDEC 51-7 standard.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm, furthermore, outer layers with 1 oz. Cu and inner layers with 1 OZ. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Typical Application Circuit

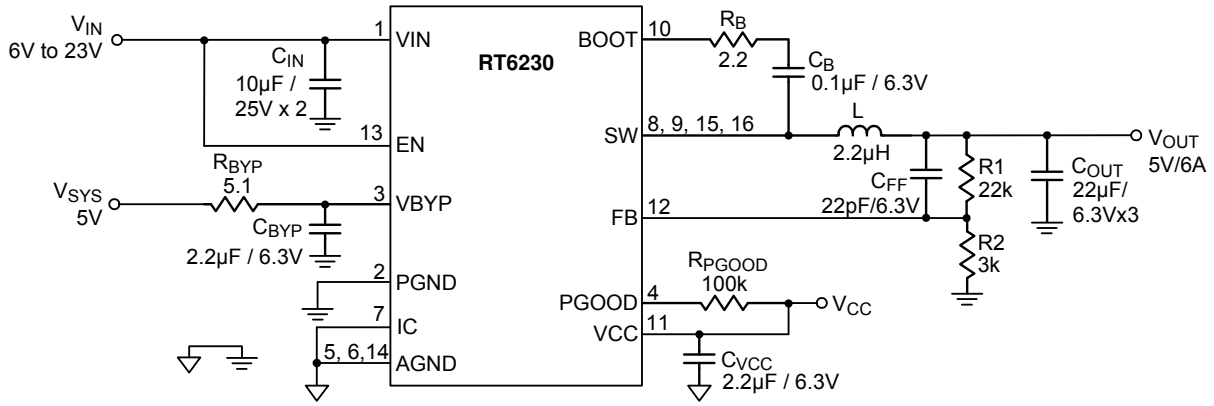


Figure 3. Typical Application Circuit for V_{OUT} = 5V

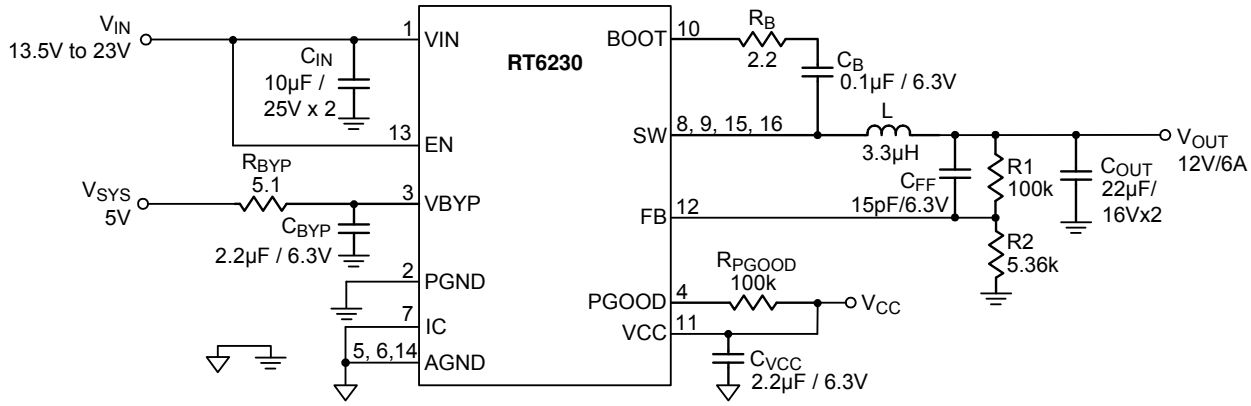
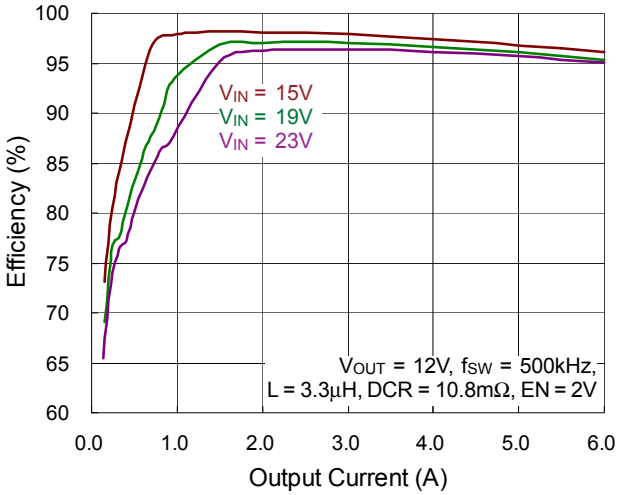


Figure 4. Typical Application Circuit for V_{OUT} = 12V

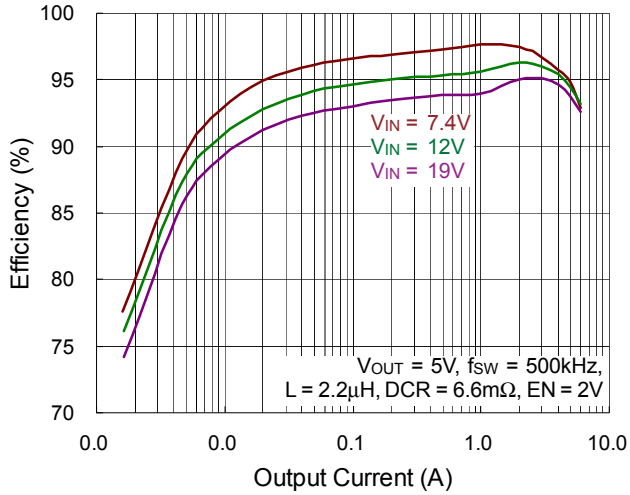
Typical Operating Characteristics

Performance waveforms are tested on the evaluation board of the Typical Application Circuit, T_J = 25°C, unless otherwise noted.

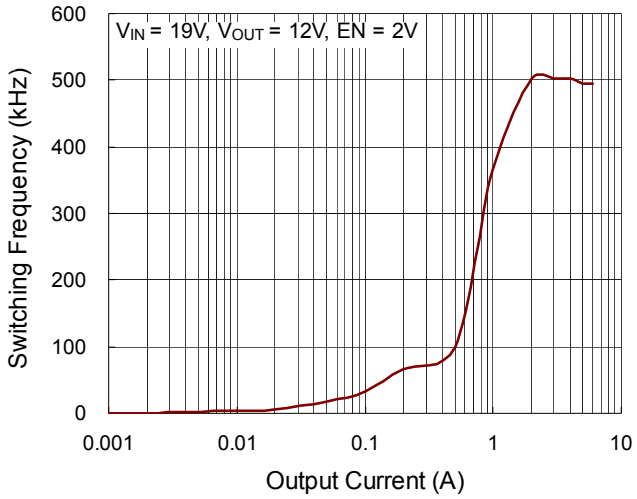
Efficiency vs. Output Current



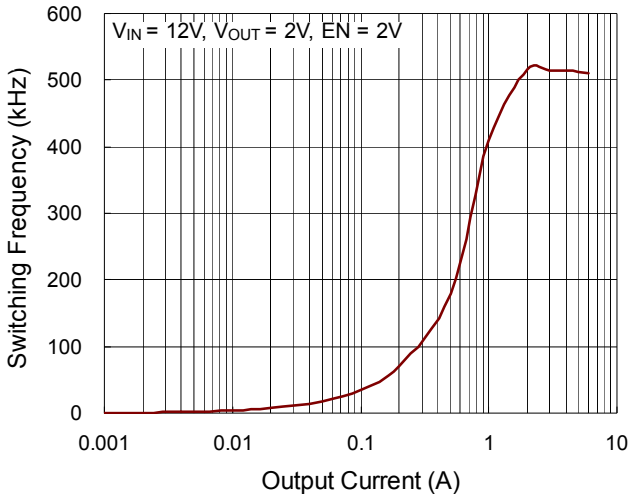
Efficiency vs. Output Current



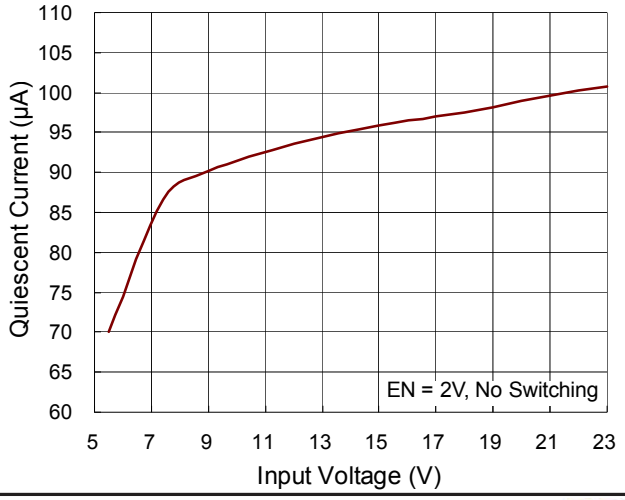
Switching Frequency vs. Output Current



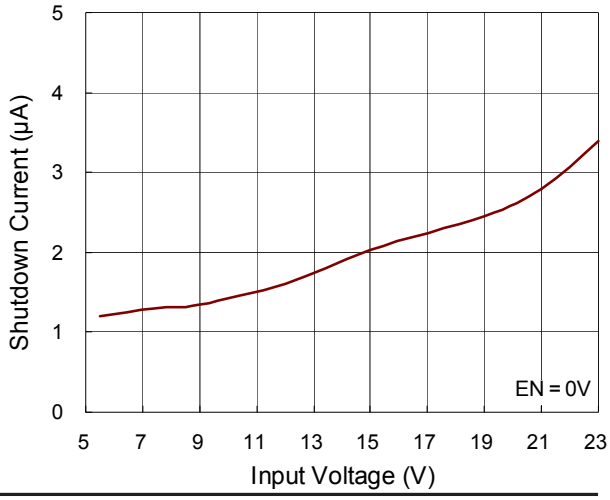
Switching Frequency vs. Output Current



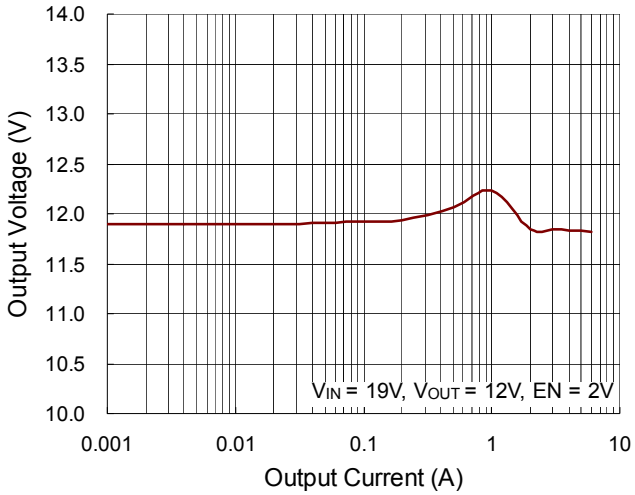
Quiescent Current vs. Input Voltage



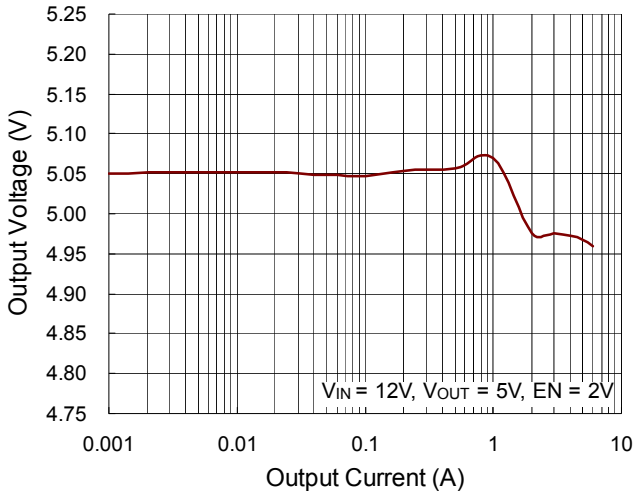
Shutdown Current vs. Input Voltage



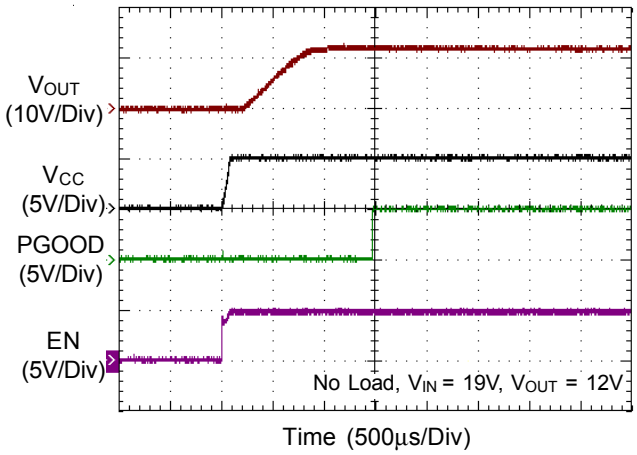
Output Voltage vs. Output Current



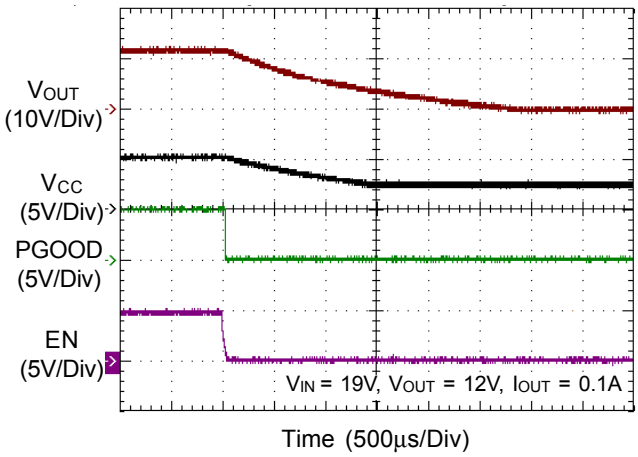
Output Voltage vs. Output Current



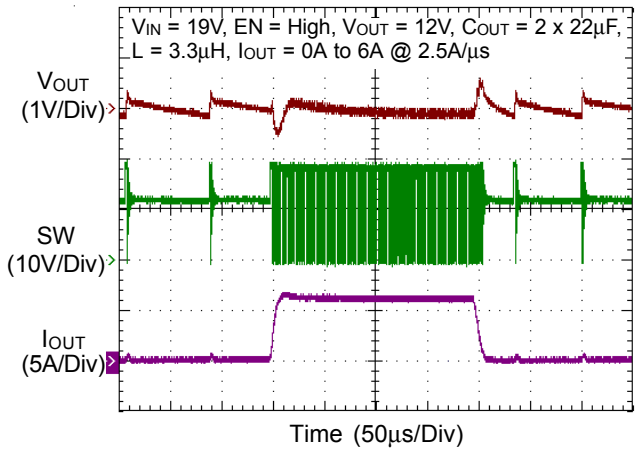
Power On Through EN



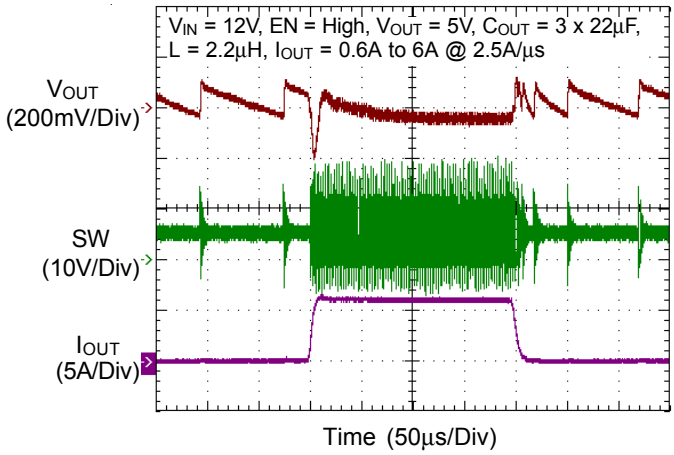
Power Off Through EN



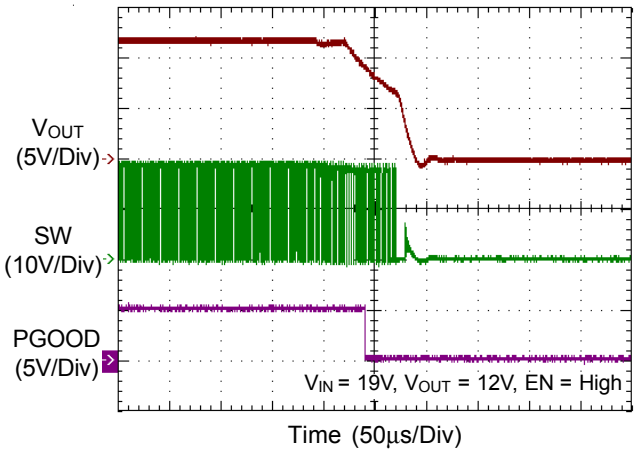
Load Transient Response



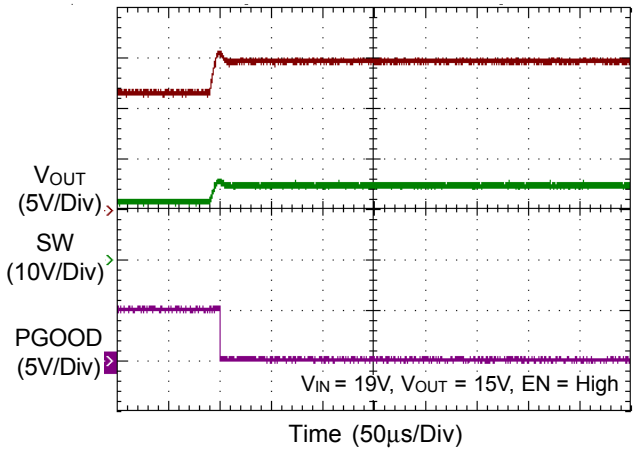
Load Transient Response



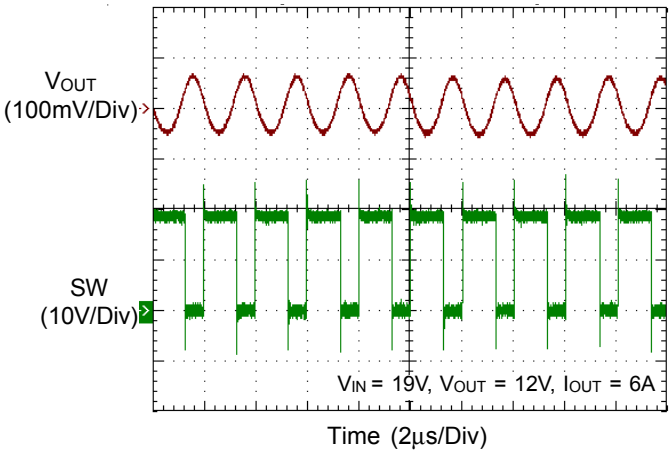
UVP



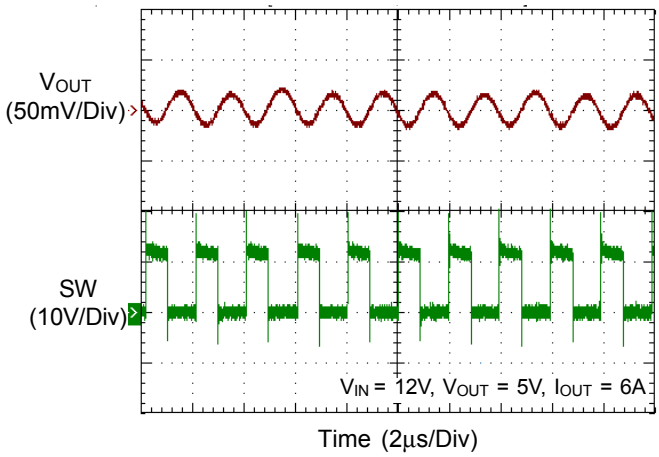
OVP



Output Ripple



Output Ripple



Application Information

Output Voltage Setup

The output voltage of RT6230 is adjustable and with valley control. There is an easy way to determine the output voltage only by two resistors, R1 and R2. As the feedback circuit shown in Figure 5, the relation of V_{OUT} and V_{REF} can be derived as V_{OUT} = (1+R1/R2) x V_{REF} readily. Generally, the stability is a serious issue for converter. In order to achieve better performance on stability and transient, a feed-forward capacitor, C_{FF}, is added to increase the noise margin and transient response of loop control. However, there is a tradeoff of adding a feed-forward capacitor. An additional dc offset will be generated on output voltage due to the amplified feedback ripple by feed-forward compensator. This is not always the case that every C_{FF} makes the same value of dc offset, and it is based on different pole and zero placement generated by R1, R2 and C_{FF}. For simplicity, a symbol named $V_{dc,offset}$ is supposed to be the value of dc offset. This value may influence the performance (e.g. regulation or peak value of V_{OUT}) of converter slightly, and the suggested C_{FF} is to select a pair of pole and zero to provide the maximum phase lead at switching frequency.

$$V_{OUT,valley} = \left(1+\frac{R1}{R2}\right)\times V_{REF} + V_{dc,offset}$$

$V_{OUT,valley}$ is the valley of output voltage, and $V_{dc,offset}$ is used for describing the additional dc offset on V_{OUT}, the value is related to the output voltage ripple and C_{FF}.

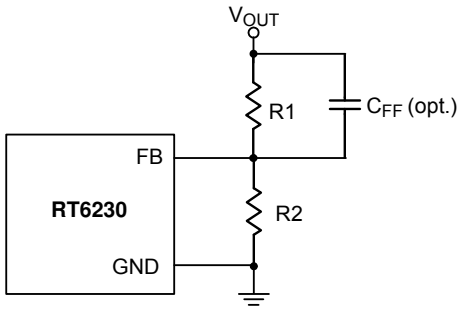


Figure 5. The Equivalent Circuit of Feedback Loop

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response. However, they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20 to 50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times f_{SW}\times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times f_{SW}\times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements.

For low inductor core losses, a shielded-type ferrite core is usually best, although possibly larger or more expensive, will probably give fewer EMI noise.

For the RT6230, the maximum allowable inductance depends on the noise margin between output feedback ripple and internal ramp to avoid multi-pulse in light-load. When output capacitor is designed with 22μF/0805/16V x 2 and VOUT is 12V, the maximum allowable inductance is 3.3μH.

Output Capacitor Selection

The RT6230 is optimized for ceramic output capacitors and best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(ESL)} = \frac{d}{dt} I_L \times ESL$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

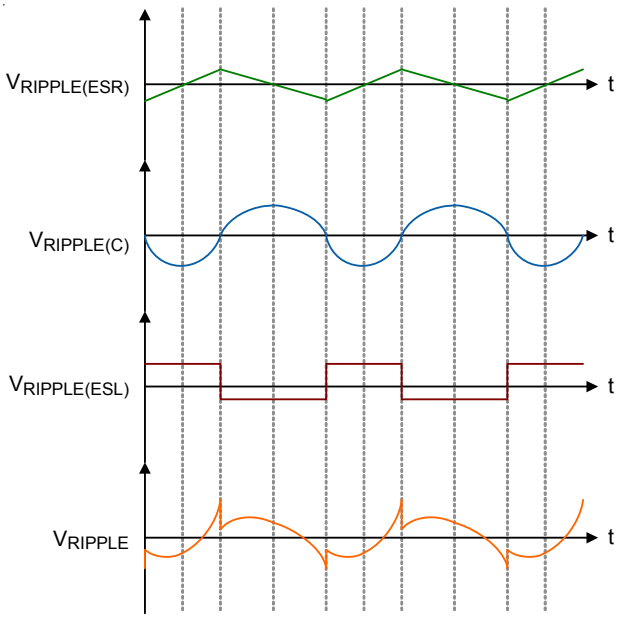


Figure 6. Output Ripple Decomposition

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is

as fast as allowed. The behavior diagram of output voltage drop is depicted as Figure 7. Calculate the approximate on-time (neglecting parasitic) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increases compensations for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

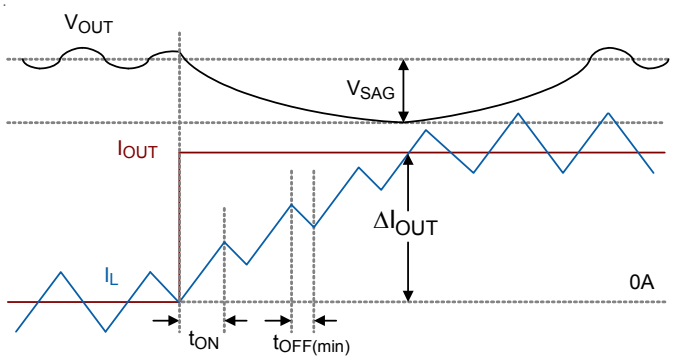


Figure 7. Output Voltage Drop (V_{SAG}) Estimation as Output Load Current Step Up

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

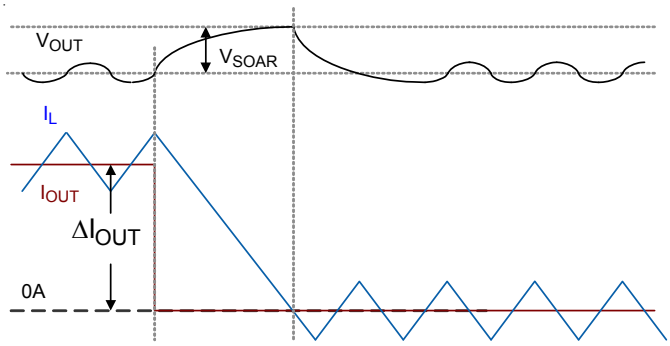


Figure 8. Output Voltage SOAR (V_{SOAR}) Estimation as Output Load Current Step Down

Most applications never experience instantaneous full load steps and the RT6230's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that over-voltage protection and under-voltage protection will not be triggered.

In addition, the recommended dielectric type of the capacitor is X7R which has the best performance among temperature and DC and AC bias voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Moreover, the maximum allowable output capacitance should consider the soft-start time and inductor current limit threshold. If output capacitance is too large, the IC will be unable to ramp up the output voltage to reference target within the determined soft-start time. During soft-start period, the UVP is masked. After that, the UVP is triggered as VOUT is still below UVP threshold, and IC enters latch mode or restart by hiccup mechanism.

Input Capacitor Selection

A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance causes high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

The capacitor voltage rating should meet reliability and safety requirements. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current due to low ESR and ESL. The following equation is used to estimate the required effective capacitance that will meet the ripple requirement.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1\text{-}D)}{\Delta V_{IN\_PP} \times f_{SW}}$$

Where D is calculated as below :

$$D = \frac{V_O}{V_{IN} \times \eta}$$

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1 - \frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Besides, since the ESL of ceramic capacitors plays a significant role on voltage spike at input and phase node, it is desirable to add a small capacitor with low ESL near VIN pin.

While the MLCC is excellent regarding allowable ripple current, it is well-known regarding effective capacitance that is necessary to meet transient response requirements. There could be two VIN spikes during the transient: the first spike is related to the ESR; and the second spike is caused by the difference between the buck-converter input current (i_{IN_B}) and the bus-converter output current (i_{PS}) as depicted in Figure 10. Both spikes should be lower than the VIN undershoot or overshoot requirement (VIN_tran). First, since the MLCCs have very small ESR, the component of ESR drop can almost be ignored. The second spike is related to the response of the bus converter. The converter output-current rise time during a transient event, t_{R_PS}, can be approximated by the following equation :

$$t_{R\_PS} \cong \frac{0.35}{f_{BW\_PS}}$$

, where f_{BW_PS} is the control loop bandwidth of Buck converter.

The equivalent capacitance of the input capacitors should be greater than that calculated with following equation :

$$C_{IN} \geq \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times t_{R\_PS}}{V_{IN\_Tran}}$$

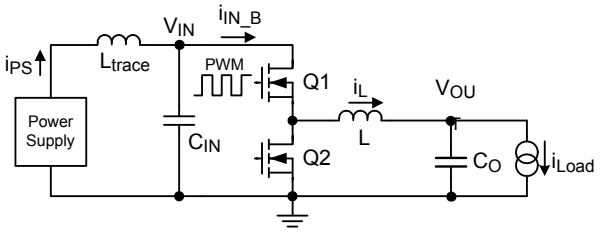


Figure 9. The Basic Circuit of a Buck Converter

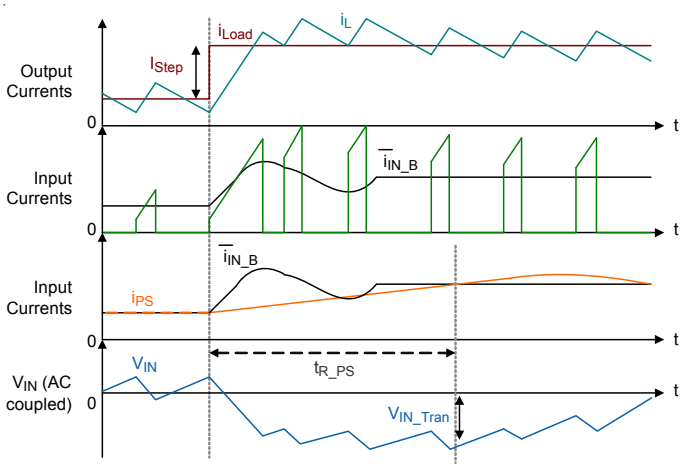


Figure 10. VIN Transient Current Diagram

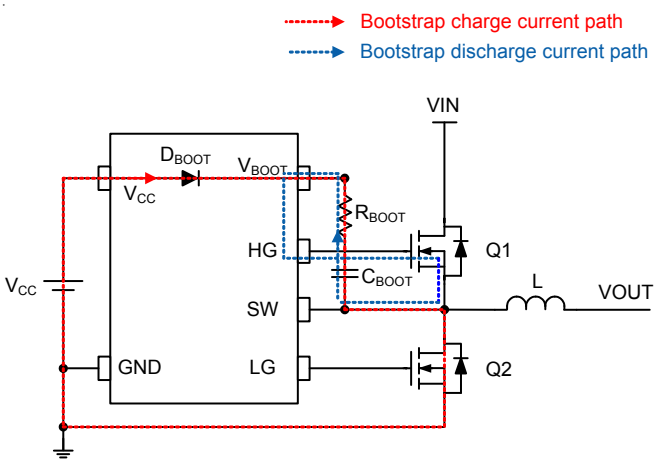


Figure 11. Bootstrap Power Supply Circuit

Either Vin ripple (ΔV_{IN_PP}) or Vin transient ripple (V_{IN_Tran}) should meet the design requirements. For the RT6230, the input voltage should be always higher than 6V threshold to confirm the IC functionality. Moreover, it should be noticed that many de-rating factors, including Vbias dc voltage, ac voltage and operating temperature, make equivalent capacitance be smaller than the capacitance without bias.

Bootstrap Circuit

The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. When the SW node goes below the IC supply voltage V_{CC} or is pulled down to ground (the low-side MOSFET is turned on and the high-side MOSFET is turned off), the bootstrap capacitor, C_{BOOT}, charges through the bootstrap resistor, R_{BOOT}, and bootstrap diode, D_{BOOT}, from the V_{CC} power supply, as shown in Figure 11. On the other hand, the voltage across V_{BOOT} and SW can supply gate charge to high-side MOSFET when low-side MOSFET is turned off and SW node goes to a higher voltage, VOUT. In the meantime, the bootstrap diode reverses bias and blocks the rail voltage from the IC supply voltage, V_{CC}. It should be noticed that the circuit in Figure 11 is just an example to describe the current paths during bootstrap circuit operation, and the actual application circuit of the RT6230 should refer to Typical Application Circuit section.

There are some design considerations for a bootstrap circuit. First, the selection of bootstrap capacitor (C_{BOOT}) is based on the maximum voltage drop across C_{BOOT} to guarantee the high-side MOSFET has enough charge to turn on periodically. The maximum allowable voltage drop (ΔV_{BOOT}) depends on the minimum gate drive voltage (for the high-side MOSFET) to maintain. If V_{GSMIN} is the minimum gate-source voltage, the capacitor drop must be :

$$\Delta V_{BOOT} = V_{CC} - V_F - V_{GSMIN}$$

where V_{CC} is the supply voltage of gate driver, and V_F is the forward voltage drop of bootstrap diode.

Therefore, the value of bootstrap capacitor is calculated as :

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{BOOT}}$$

where Q_{Total} is the total amount of the charge required for driving the high-side MOSFET and some leakage charge in the chip.

Second, when the external bootstrap resistor is used, the resistance, R_{BOOT}, introduces an additional voltage drop :

$$V_{RBOOT} = \frac{Q_{Total}}{t_{Charge}} \times R_{BOOT}$$

where t_{Charge} is the bootstrap charging time (the low-side MOSFET turn-on time).

The power dissipation on R_{BOOT} should be considered when choosing the package size of resistor. When estimating the maximum allowable voltage drop, the value of voltage drop of bootstrap resistor should be taken into account.

For example, assume V_{CC} = 5V, V_F = 0.7V, R_{BOOT} = 1Ω, V_{GSMIN} = 2.5V and Q_{Total} = 5nC. The ΔV_{BOOT} can be calculated as 1.8V. The estimated C_{BOOT} is 2.8nF. Generally, the ΔV_{BOOT} is not suggested to be too large and also need to consider the additional voltage drop on R_{BOOT}. Moreover, the de-rating factors, including Vbias dc voltage, ac voltage and operating temperature, make equivalent capacitance be smaller. The common selection value of C_{BOOT} is 100nF to 220nF, that makes the ΔV_{BOOT} to be 50mV and 25mV separately. If choosing the bias capacitor with 0201 package and 6.3V voltage rating, the de-rating factor is about 0.5. Therefore, the ΔV_{BOOT} increases to 100mV and 50mV. In addition, the voltage drop on R_{BOOT} = 1Ω is 25mV as t_{Charge} is 200nsec. Adding the R_{BOOT} can reduce the EMI noise as well as voltage spike on phase node. However, the additional power loss will reduce the system efficiency.

VCC LDO Decoupling Capacitor

The RT6230 integrates an internal 5V voltage regulator (V_{CC}) which is supplied by VIN and provides power to the internal circuitry. The V_{CC} can be used as the PGOOD pull-up supply, but it can't be a power source to external loads. A decoupling capacitor is necessary to place near VCC pin and the equivalent minimum capacitance should be at least 0.9μF. In many applications, a 2.2μF/6.3V/ X5R/0603 capacitor is recommended and the layout placement should be as close as possible to VCC pin and AGND pin, in order to reduce the parasitic inductance and impedance. When choosing the package size and voltage rating of a capacitor, the de-rating coefficient versus voltage and temperature is important for taking account of equivalent capacitance under actual operating condition.

Feed-Forward Compensator Design

For saving time to design compensator and reducing the layout area through external components, the components of compensator are integrated in IC. However, this integrated compensator might not suit to every load transient spec. Hence, for the RT6230 to be more adaptable, the feed-forward capacitor C_{FF} is used in the feedback loop to improve transient response, as shown in Figure 12. Figure 13 shows the comparison result of bode plot with different feedback loop conditions. Referring to Figure 13, through connecting a C_{FF} in feedback network, the gain and phase are raised in mid-frequency that not only can extend the bandwidth, but also boost the phase margin. Moreover, there is also a high frequency pole to eliminate high frequency noise. Consequently, those features of feed-forward feedback network allow the RT6230 have faster response to handle different load transient.

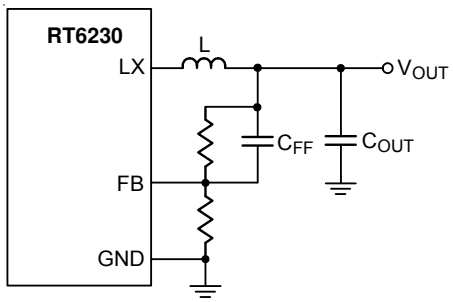


Figure 12. Feedback Loop with Feed-Forward Capacitor

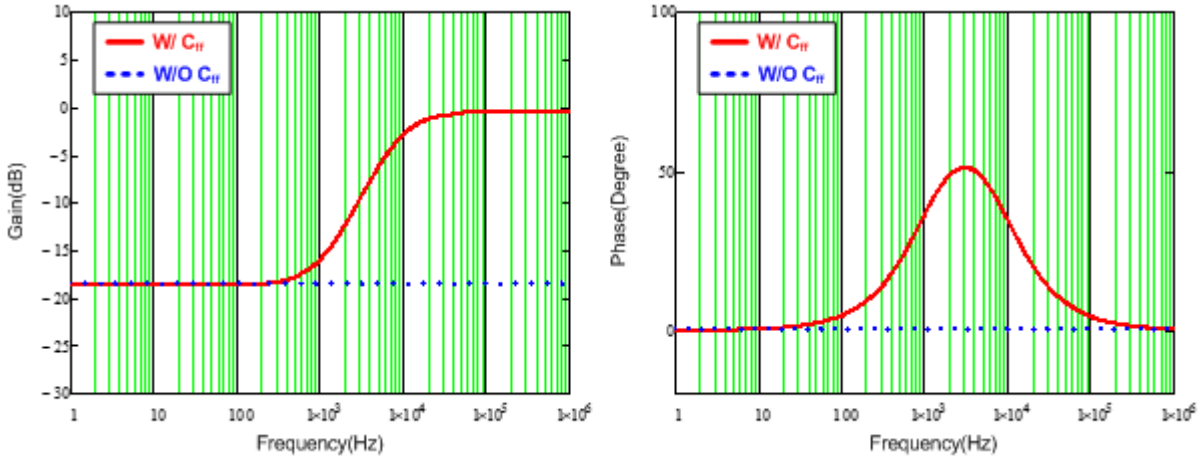


Figure 13. Bode Plot with Different Feedback Loop Conditions

The transfer function of feedforward network is expressed in equation (1) and the positions of zero and pole are calculated in equation (2) and equation (3).

$$\frac{V_{FB}(s)}{V_{OUT}(s)} = \frac{1}{1+\frac{R1}{R2}} \times \frac{1+\frac{s}{\frac{1}{R1\times C_{FF}}}}{1+\frac{s}{\frac{1}{(R1//R2)\times C_{FF}}}} \quad (1)$$

$$f_P = \frac{1}{2\pi\times(R1//R2)\times C_{FF}} \quad (2)$$

$$f_Z = \frac{1}{2\pi\times R1\times C_{FF}} \quad (3)$$

Observing Figure 13, the maximum phase boost occurs between zero and pole frequencies that is defined as maximum phase boost frequency, as expressed in equation (4). Hence, in order to achieve the maximum phase boost by adding C_{FF} in the RT6230, the system's original bandwidth has to be located at maximum phase boost frequency.

$$f_{ph\_max} = \sqrt{f_P \times f_Z} \quad (4)$$

For putting zero at the correct frequency to implement maximum phase boost, the first thing is to determine system's bandwidth. There is a simple way to measure bandwidth of the RT6230 that is load transient analysis. By using a converter without feedforward network to observe the voltage deviation frequency during load step, the bandwidth of converter can be obtained because of the crossover frequency related to voltage deviation frequency approximately, as shown in Figure 14.

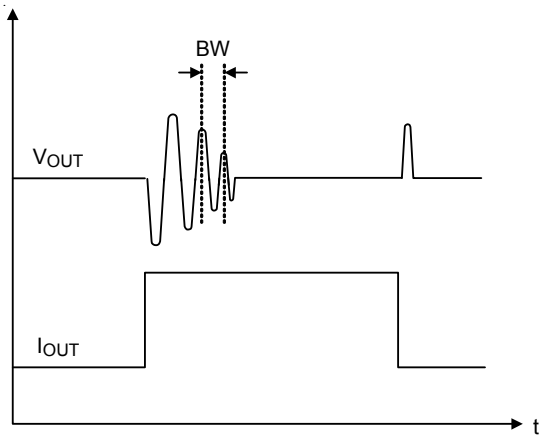


Figure 14. Bandwidth Estimation by Step Load Measurement

Following the above concept, the equation of bandwidth with feedforward C_{FF} can be derived, as expressed in equation (5).

$$BW = \sqrt{\frac{1}{2\pi\times R1C_{FF}} \times \frac{1}{2\pi\times C_{FF}}\left(\frac{1}{R1}+\frac{1}{R2}\right)} \quad (5)$$

For optimizing transient response, the C_{FF} can be obtained from equation (5), as shown in equation (6).

$$C_{FF} = \frac{1}{2\pi\times BW}\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)} \quad (6)$$

After defining the C_{FF}, please also check the load regulation, because feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage is over spec caused by calculated C_{FF}, please decrease the value of feedforward capacitor C_{FF}.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-16L 3x3 (FC) package, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.4W for a UQFN-16L 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 15 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

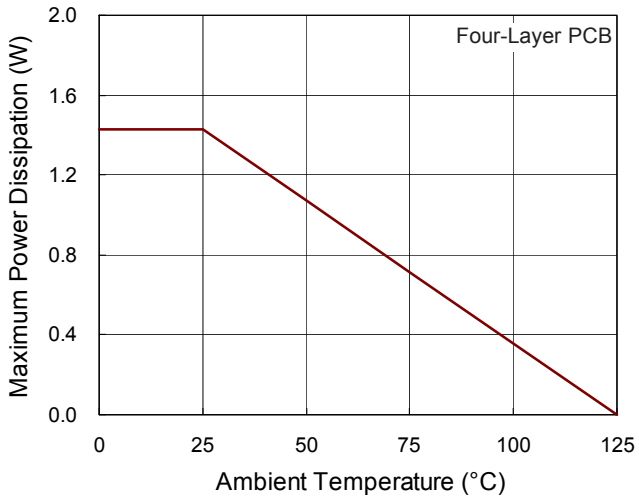


Figure 15. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT6230.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and PGND).
- The SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent noise coupling.
- The PGND pin should be connected to a strong ground plane for heat sinking and noise protection.
- Avoid using vias in the power path connections that have switched currents (from C_{IN} to PGND and C_{IN} to V_{IN}) and the switching node (SW).
- The ground of VCC is recommended to connect to GND layer through via, and the decoupling capacitor (C_{VCC}) should be placed near VCC pin. No via connection is recommended.

An example of PCB layout guide is shown in Figure 16 for reference.

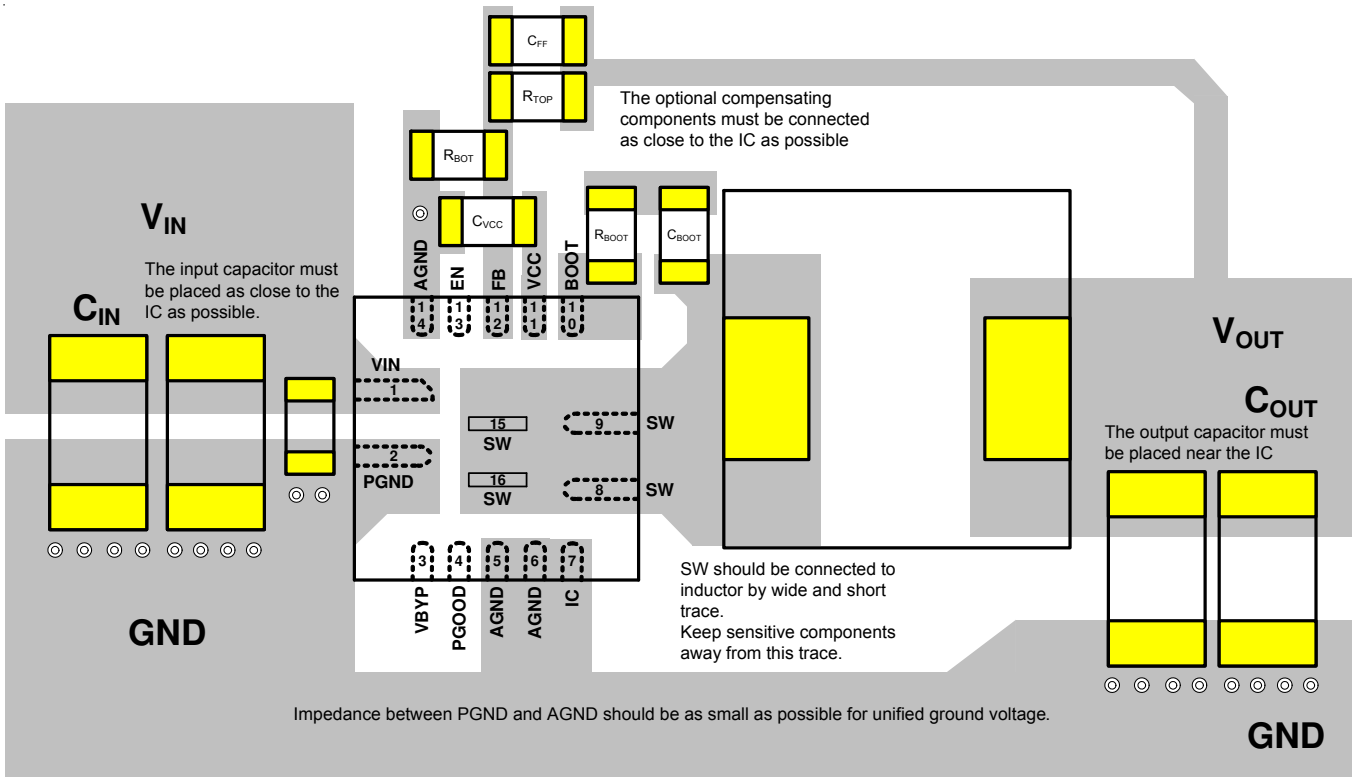


Figure 16. PCB Layout Guide

Trace Width Design

For thermal, efficiency and PCB handling current capability, the trace width design is very important. According to IPC-2221 formally IDC-D-275 PWB, the following formulas can be used to calculate the trace width for printed circuit boards.

Inner trace :

$$I(Amp) = 0.015 \times \Delta T(°C)^{0.5453} \times Area(mils^2)^{0.7349}$$

Outer trace :

$$I(Amp) = 0.0647 \times \Delta T(°C)^{0.4281} \times Area(mils^2)^{0.6732}$$

$$Width(mil) = \frac{Area(mils^2)}{Thickness(oz) \times 1.37\left(\frac{mil}{oz}\right)}$$

where

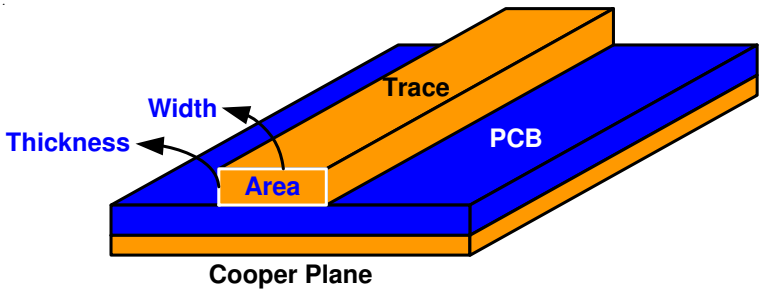
I(Amp) = Current,

ΔT(°C) = Temperature rise,

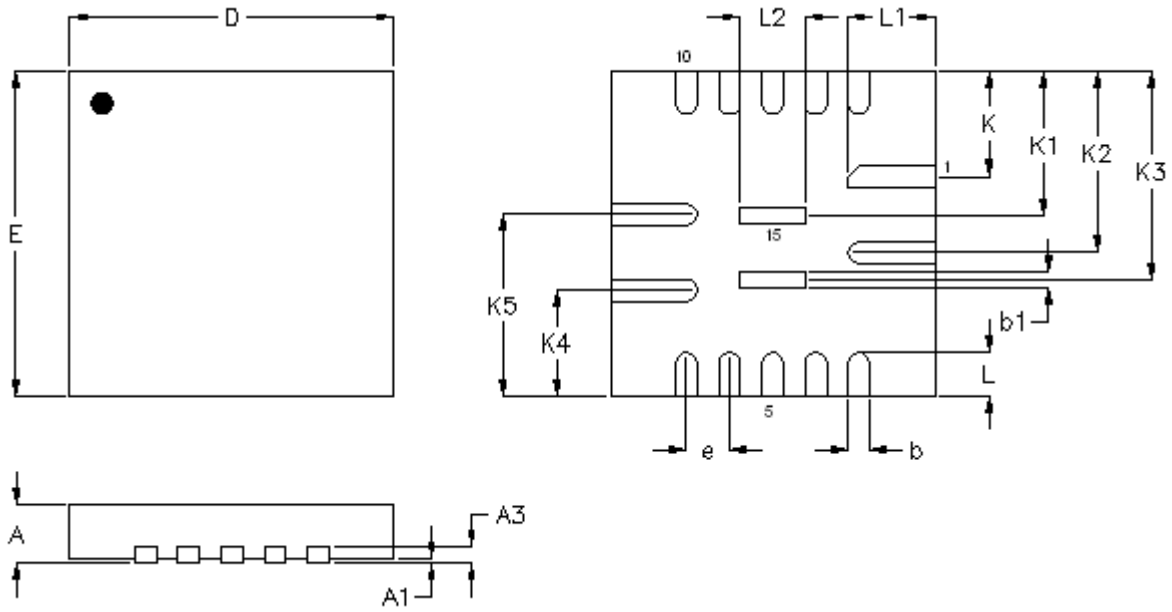
Area(mils^2) = Cross sectional area = Width x Thickness,

Width(mil) = Trace width, and

Thickness(oz) = Layer Cu thickness.



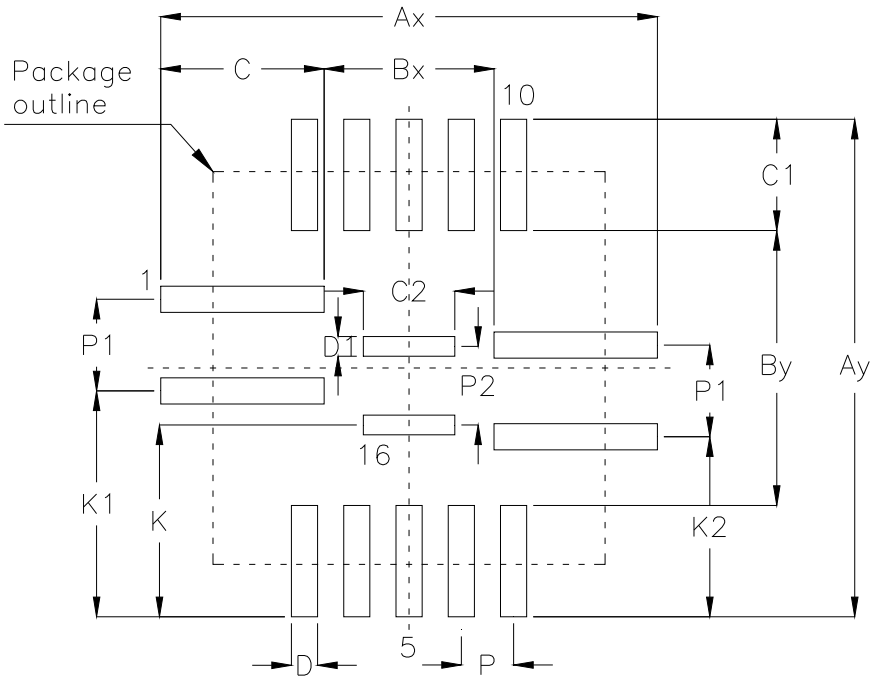
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
b	0.150	0.250	0.006	0.010
b1	0.100	0.200	0.004	0.008
L	0.350	0.450	0.014	0.018
L1	0.750	0.850	0.030	0.033
L2	0.550	0.650	0.022	0.026
e	0.400		0.016	
K	0.975		0.038	
K1	1.335		0.053	
K2	1.675		0.066	
K3	1.935		0.076	
K4	0.975		0.038	
K5	1.675		0.066	

U-Type 16L QFN 3x3 (FC) Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	P1	P2	Ax	Bx	Ay	By	C*4	
UQFN3x3-16(FC)	16	0.400	0.700	0.600	3.800	1.300	3.800	2.100	1.250	±0.050

Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		C1*10	C2*2	D*14	D1*2	K	K1	K2		
UQFN3x3-16(FC)	16	0.850	0.700	0.200	0.150	1.465	1.725	1.375		±0.050

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