NISSHINBO

R1260S Series

60V Input / 80V Absolute Maximum Rating Synchronous Step-down DC/DC Controller

No.EA-511-220222

OVERVIEW

The R1260S is a step-down DC/DC controller which can generate an output voltage of 1.0 V to 16.0 V by driving external high- / low-side NMOSFETs. By the adoption of a unique current mode PWM architecture without an external current sense resistor, this device can make up a stable DC/DC converter with high-efficiency even if adding low Ron MOSFETs and a low DCR inductor externally.

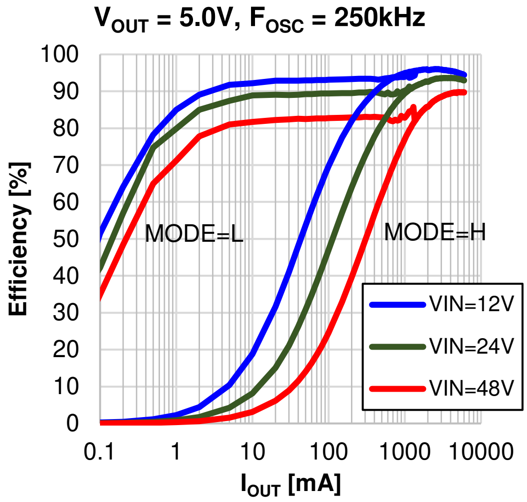
KEY BENEFITS

- 48 V power can be provided by a wide-ranging input voltage of 5 V to 60 V.
- High-accuracy feedback voltage: 0.8 V ±1.5% (−40°C ≤ Ta ≤ 105°C)
- High efficiency at light load (I_{OUT}=1mA) by VFM control (80% @V_{IN}=24V, 70% @V_{IN}=48V)

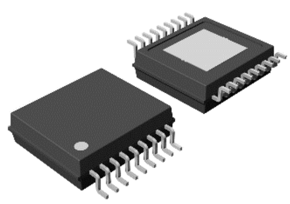
KEY SPECIFICATIONS

- Input Voltage Range: 5 V to 60 V
- Maximum Rating: 80 V
- Output Voltage Range: 1.0 V to 16.0 V
- Feedback Voltage: 0.8 V ±1.5%
- Consumption Current at No Load: Typ.15µA (at VFM mode)
- Oscillator Frequency: 150kHz to 600kHz
- Adjustable Soft-start with an external capacitor : 600µs (without external capacitor)
- Minimum ON Time: Typ. 130 ns
- Minimum OFF Time: Typ.120 ns
- Selectable Output Voltage Controls: PWM/VFM Auto-switching mode / Forced PWM / PLL_PWM mode
- Operating Temperature Range: -40°C to 105°C
- Spread Spectrum Clock Generator (SSCG)*Option
- Power Good Output
- Undervoltage Detection (UVD), Overvoltage Detection (OVD)
- Undervoltage Lockout (UVLO)
- Thermal Shutdown: Tj = 160°C (Typ.)
- Overcurrent Protection: Hiccup-type, Latch-type
- Short-circuit Protection: LX to V_{IN} or GND

TYPICAL CHARACTERISTICS



PACKAGE



HSOP-18
(5.2 mm x 6.2 mm x 1.45 mm)

APPLICATIONS

- Power source for systems that require step-down from high voltages such as 24V or 48V.
  ・PLC ・PoE Drive Equipment ・FA Equipment ・5G Base Station ・Industrial Equipment etc.

Nisshinbo Micro Devices Inc.

SELECTION GUIDE

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1260Sxxyz-E2-FE	HSOP-18	1,000	Yes	Yes

xx : Select the set output voltage range.

xx	Set Output Voltage Range
01	1 V ≤ V_{OUT} ≤ 3.15 V
02	3.15V < V_{OUT} ≤ 8 V
03	8 V < V_{OUT} ≤ 16 V

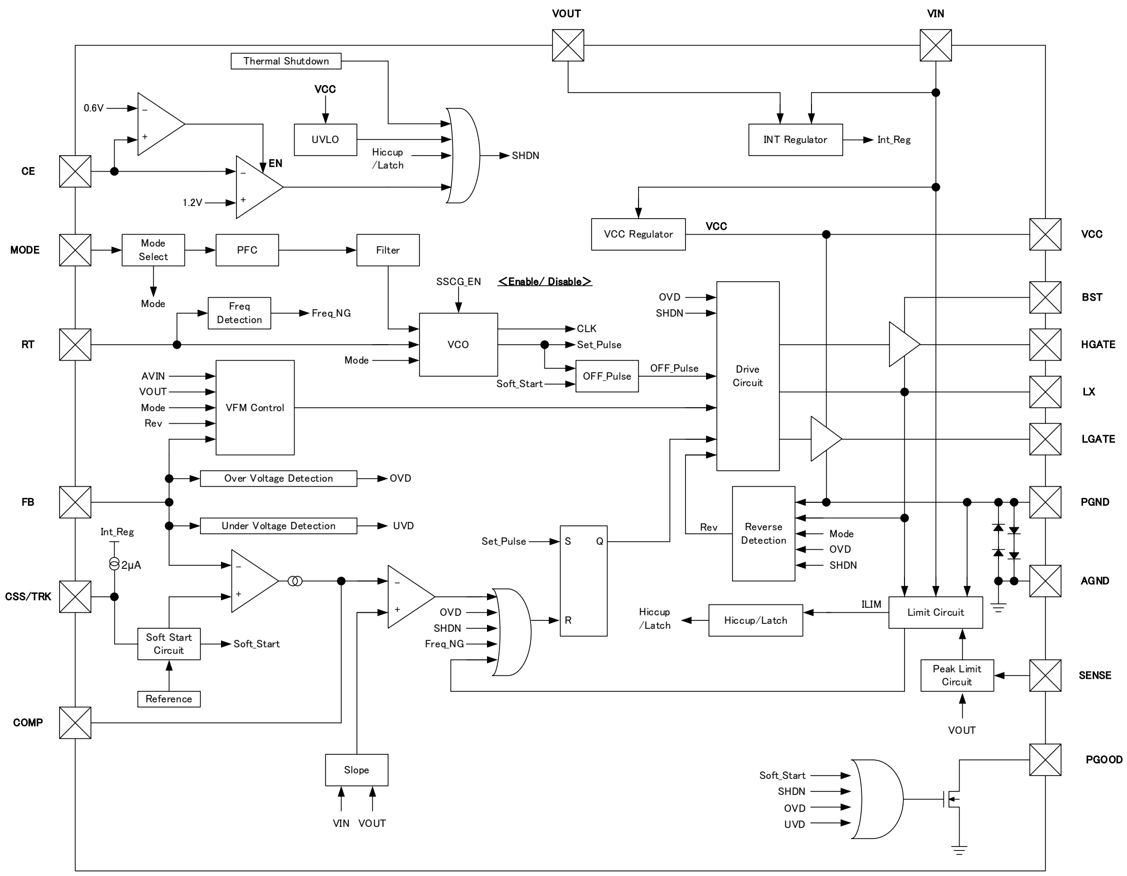
y : Select the current limit threshold voltage.

y	Current limit threshold voltage (Typ.)	Reverse current limit threshold voltage (Typ.)
1	50mV	−25mV
2	70mV	−35mV
3	100mV	−50mV

z : Select the combination of overcurrent protection and SSCG.

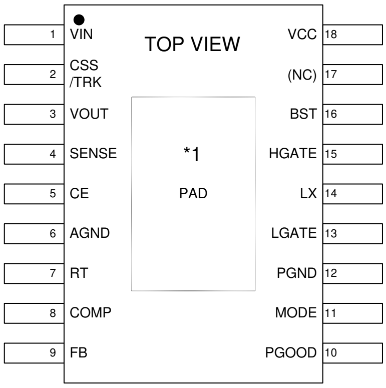
z	Overcurrent Protection	SSCG
A	Hiccup mode	Disable
B	Hiccup mode	Enable
C	Latch mode	Disable
D	Latch mode	Enable

BLOCK DIAGRAM



R1260S Block Diagram

PIN DESCRIPTIONS



R1260S Pin Configuration

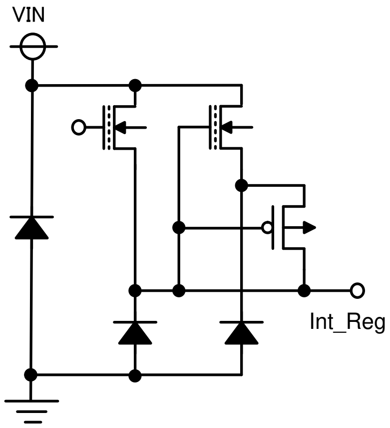
∗1 The tab on the bottom of the package must be electrically connected to GND (substrate level) when mounted on the board.

Pin Description

Pin No.	I/O	Pin Name	Description
1	I	VIN	Power Supply Input Pin. Apply input voltage between VIN pin and GND. Connect the input capacitor between the VIN pin and GND.
2	I	CSS/TRK	Soft-start and Tracking Control input pin. A capacitor to ground from this pin sets the ramp time to full output voltage. Without the capacitor, soft start time is Typ. 600us. Controlling this pin externally from 0V to 0.8V with a certain slope, the output voltage tracks the slope.
3	I	VOUT	Power Supply for Internal Circuit/Output Voltage Sense pin. Connect this pin to Output Voltage node. Connect a capacitor between this pin and GND.
4	I	SENSE	Sense pin for inductor current. By connecting a sense resistor between the VOUT pin and SENSE pin, the current value of the current limit and reverse current limit can be set.
5	I	CE	Chip enable pin. Forcing this pin above 1.3V enables the operation of the R1260. Forcing this pin below 1.1V stops switching operation of the R1260. Forcung this pin below 0.39V, all functions are disabled.
6	–	AGND	Analog ground of the internal circuit. Connect this pin to the GND of PCB.
7	I	RT	Timing Resistor pin to Program the Oscillator Frequency. Connecting a resistor to ground from this pin sets the switching frequency. Switching frequency range is from 150kHz to 600kHz. R_{RT} [kΩ] = 34064 x f_{OSC} [kHz] ^ (-1.025)
8	O	COMP	Error amplifier phase compensation pin. Connect a resistor and a capacitor for phase compensation.
9	I	FB	Feedback input pin to the error amplifier. Receives the feedback voltage from a restive divider connected across the output.
10	O	PGOOD	Power-good output pin. NMOS open-drain logic output that is pulled to ground when the output voltage is not within the normal state. Refer to the “Power Good Function”. Pull-up voltage rating is 6V.
11	I	MODE	Mode Select and External Clock Synchronization Input pin. To select forced PWM mode, connect this pin to above designated “High”. Connecting this pin to a voltage between 0V and designated “Low” selects PWM/VFM auto-switching mode.
12	–	PGND	Power ground. Connect this pin close to GND of PCB.
13	O	LGATE	Gate Drive pin for Bottom(low-side) Synchronous N-Channel MOSFET.

14	I	LX	Switch Node Connection to Inductor. This pin connects to the switch node between source of the high-side MOSFET and the drain of the low-side MOSFET, and the inductor.
15	O	HGATE	Gate Drive pin for Top(high-side) N-Channel MOSFET.
16	O	BST	Bootstrapped pin. A capacitor (C_{BST}) between the LX pin and the BST pin, and Schottky diode are tied between the VCC pin and the BST pin. Voltage between BST pin and Lx pin is controlled to Typ.5V.
17	—	NC	No connection. It is recommended to be left open to reduce the risk of adjacent pins' short.
18	O	VCC	Output pin of Internal 5V linear Regulator The control circuits of drive external NMOSFETs are powered from this voltage source. Must be decoupled to power ground with an output capacitor (C_{VCC}).

Internal Equivalent Circuit for Each Pin



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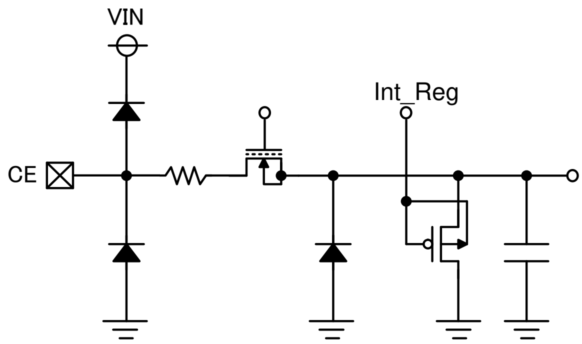

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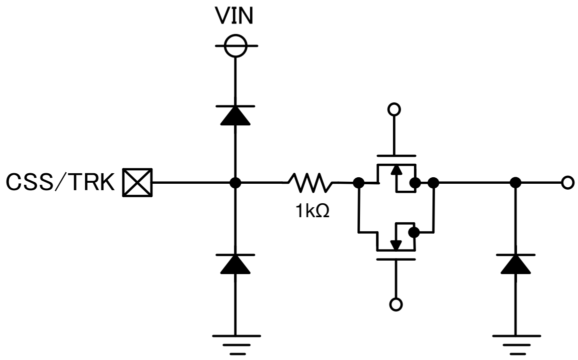

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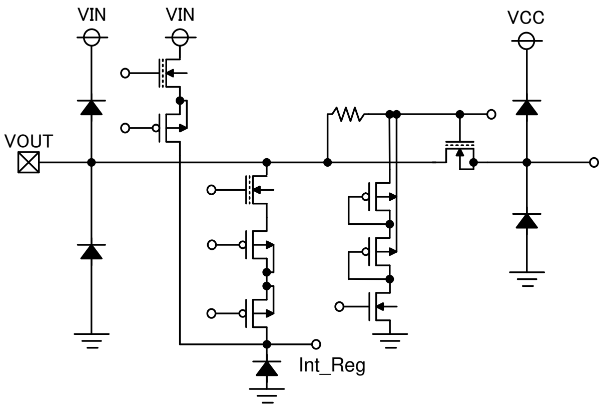

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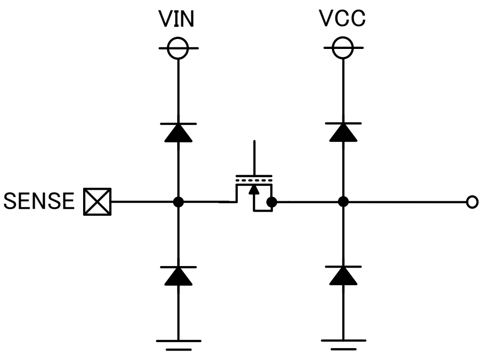

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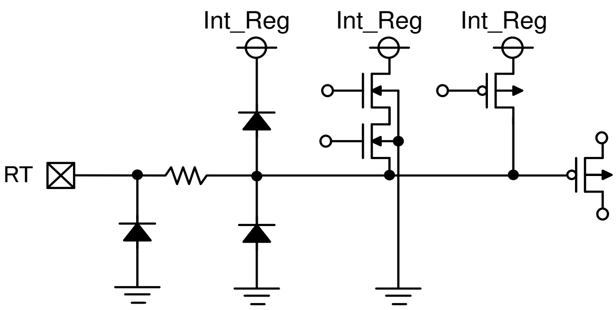

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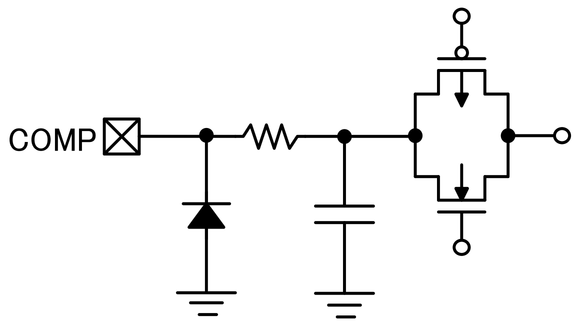

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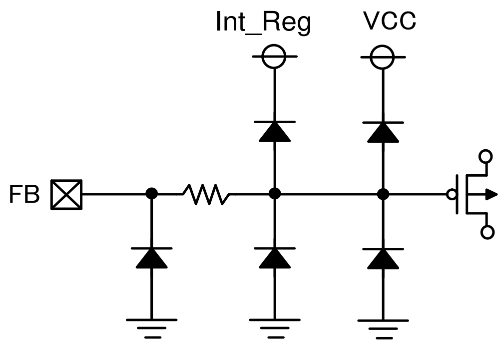

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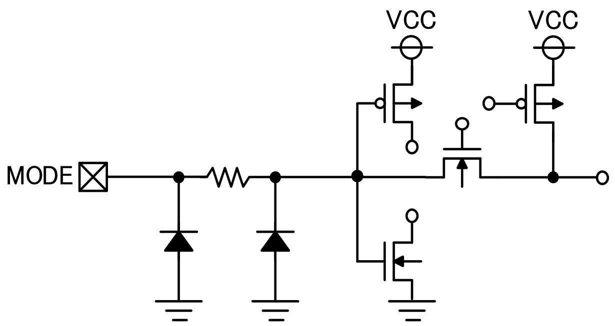

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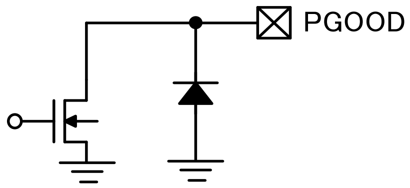
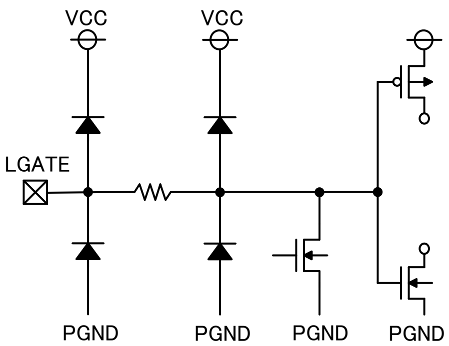


< PGOOD Pin >



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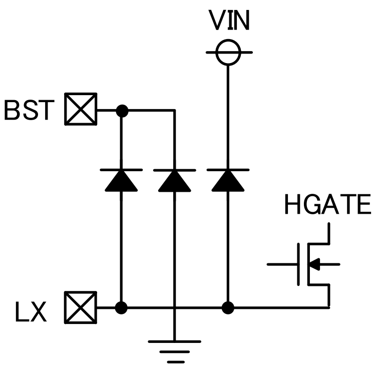
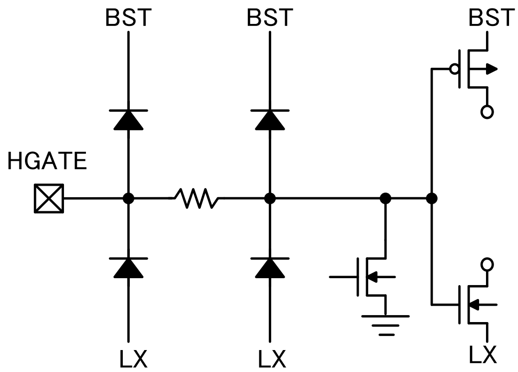


< LX、BST Pin >



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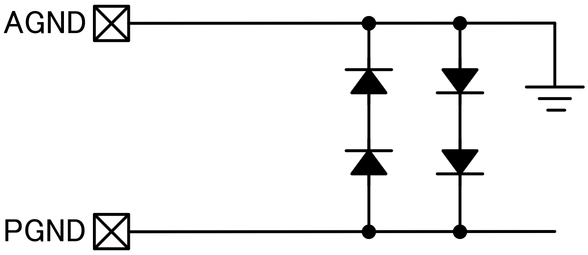
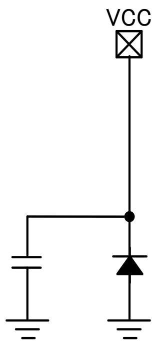


< AGND-PGND Pins >



< VCC Pin >

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Ratings	Unit
V_{IN}	Input voltage	-0.3 to 80	V
V_{CE}	CE pin voltage	-0.3 to V_{IN}+0.3 ≤ 80	V
$V_{CSS/TRK}$	CSS/TRK pin voltage	-0.3 to 3	V
V_{OUT}	VOUTpin voltage	-0.3 to 20	V
V_{SENSE}	SENSE pin voltage	-0.3 to 20	V
V_{RT}	RT pin voltage	-0.3 to 3	V
V_{COMP}	COMP pin voltage	-0.3 to V_{CC} + 0.3 ≤ 6	V
V_{FB}	FB pin voltage	-0.3 to 2.85	V
$V_{SENSEOUT}$	Voltage between VOUT and SENSEpins	-0.3 to 0.3	V
V_{CC}	VCC pin votlage	-0.3 to 6	V
	Output current for VCC pin	Internally limited	mA
V_{BST}	BST pin voltage	LX-0.3 to LX+6	V
V_{HGATE}	HGATE pin voltage	LX-0.3 to BST	V
V_{LX}	LX pin voltage	-0.3 to V_{IN} +0.3 ≤ 80	V
V_{LGATE}	LGATE pin voltage	-0.3 to V_{CC} + 0.3 ≤ 6	V
V_{MODE}	MODE pin voltage	-0.3 to 6	V
V_{PGOOD}	PGOOD pin voltage	-0.3 to 6	V
P_D	Power Dissipation	Refer to Appendix *“POWER DISSIPATION”*	
Tj	Junction Temperature	-40 to 125	°C
Tstg	Storage Temperature Range	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

ELECTROSTATIC DISCHARGE(ESD) RATINGS

Symbol	Conditions	Ratings	Unit
V_{HBM}	HBM C=100pF、R=1.5kΩ	±2000	V
V_{CDM}	CDM	±1000	

Electrostatic Discharge Ratings

The electrostatic discharge test is done based on JESD47.
In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Ratings	Unit
V_{IN}	Input Voltage	5.0 to 60	V
Ta	Operating Temperature Range	−40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48 V, V_{CE} = 5 V, unless otherwise specified.

The specifications surrounded by $\boxed{}$ are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1260Sxxyz Electrical Characteristics (Ta = 25°C)

Symbol	Item		Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage			1		16	V
V_{CC}	VCC Pin Voltage (VCC – AGND)		V_{FB} = 0.84 V	$\boxed{4.85}$	5.1	$\boxed{5.3}$	V
$I_{STANDBY}$	Standby Current		V_{IN} = 60 V, V_{CE} = 0 V		3	8.5	µA
I_{VIN1}	VIN Consumption Current 1 at Switching Stop in PWM Mode	R1260S01yz	V_{FB} = 0.84 V, V_{MODE} = 5 V, V_{OUT} = V_{SENSE} = V_{LX} = 5 V		1.37	1.77	mA
		R1260S02yz R1260S03yz	V_{FB} = 0.84 V, V_{MODE} = 5 V, V_{OUT} = V_{SENSE} = V_{LX} = 5 V		1.00	1.50	
I_{VIN2}	VIN Consumption Current 2 at Switching Stop in VFM mode	R1260S01yz	V_{FB} = 0.84 V, V_{MODE} = 0 V V_{OUT} = V_{SENSE} = V_{LX} = 5 V		48	85	µA
		R1260S02yz R1260S03yz	V_{FB} = 0.84 V, V_{MODE} = 0 V V_{OUT} = V_{SENSE} = V_{LX} = 5 V		15	45	
V_{UVLO2}	UVLO Threshold Voltage		V_{CC} Rising	4.20	4.50	4.80	V
V_{UVLO1}			V_{CC} Falling	3.68	3.80	3.97	V
V_{FB}	FB Voltage Accuracy		Ta = 25°C	0.792	0.8	0.808	V
			-40°C ≤ Ta ≤ 105°C	$\boxed{0.788}$		$\boxed{0.812}$	
f_{OSC0}	Oscillation Frequency 0		RT = 200 kΩ	$\boxed{135}$	150	$\boxed{165}$	kHz
f_{OSC1}	Oscillation Frequency 1		RT = 47 kΩ	$\boxed{540}$	600	$\boxed{660}$	kHz
t_{OFF}	Minimum OFF Time		V_{IN} = 5 V, V_{OUT} = 5 V		120	$\boxed{190}$	ns
t_{ON}	Minimum ON Time				130	$\boxed{170}$	ns
f_{SYNC}	Synchronizing Frequency		f_{OSC} as reference	$\boxed{f_{OSC}\ x0.5}$		$\boxed{f_{OSC}\ x1.5}$	kHz
				$\boxed{150}$		$\boxed{600}$	
t_{SS1}	Soft-start Time 1		$V_{CSS/TRK}$ = OPEN	$\boxed{0.25}$	0.6	$\boxed{1.35}$	ms
t_{SS2}	Soft-start Time 2		C_{SS} = 4.7 nF	$\boxed{1.6}$	2.1	$\boxed{2.8}$	ms
I_{TSS}	Charge Current for Soft-start Pin		$V_{CSS/TRK}$ = 0 V	$\boxed{1.8}$	2	$\boxed{2.2}$	µA
V_{SSEND}	CSS/TRK pin Voltage at End of Soft-start			$\boxed{V_{FB}}$	V_{FB} +0.03	$\boxed{V_{FB}+0.06}$	V
R_{DIS_CSS}	Discharge Resistance for CSS/TRK Pin		V_{IN} = 4.5 V, V_{CE} = 0 V, $V_{CSS/TRK}$ = 3 V	$\boxed{1.0}$	3.0	$\boxed{6.5}$	kΩ
$R_{UPHGATE}$	On-resistance of Pull-up Transistor (HGATE Pin)		(BST – LX) = 5 V, I_{HGATE} = -100 mA		2.5	$\boxed{5.7}$	Ω
$R_{DOWNHGATE}$	On-resistance of Pull-down Transistor (HGATE Pin)		(BST – LX) = 5 V, I_{HGATE} = 100 mA		1.5	$\boxed{5.0}$	Ω
$R_{UPLGATE}$	On-resistance of Pull-up Transistor (LGATE Pin)		(VCC – PGND) = 5V, I_{LGATE} = -100mA		4.0	$\boxed{7.2}$	Ω
$R_{DOWNLGATE}$	On-resistance of Pull-down Transistor (LGATE Pin)		(VCC – PGND) = 5 V, I_{LGATE} = 100 mA		1.5	$\boxed{4.7}$	Ω

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

V_{IN} = 48 V, V_{CE} = 5 V, unless otherwise specified.

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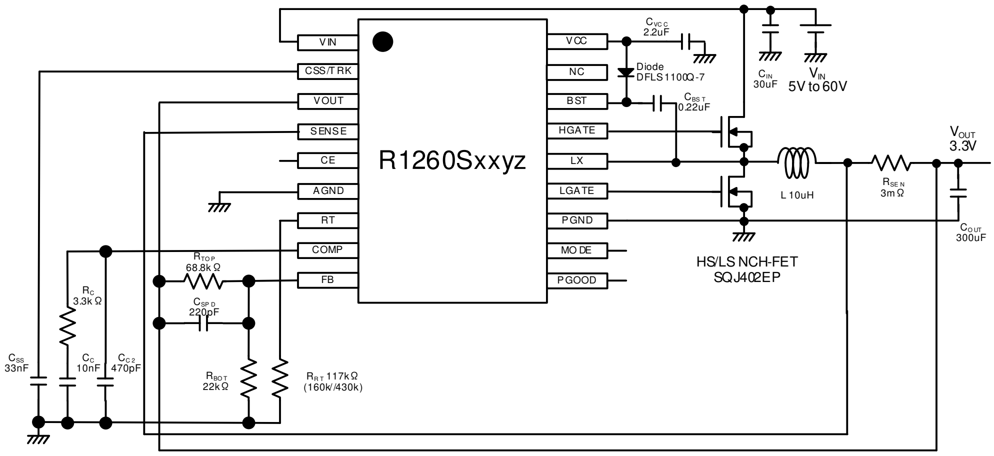
The specifications surrounded by ☐ are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1260Sxxyz Electrical Characteristics (Ta = 25°C)

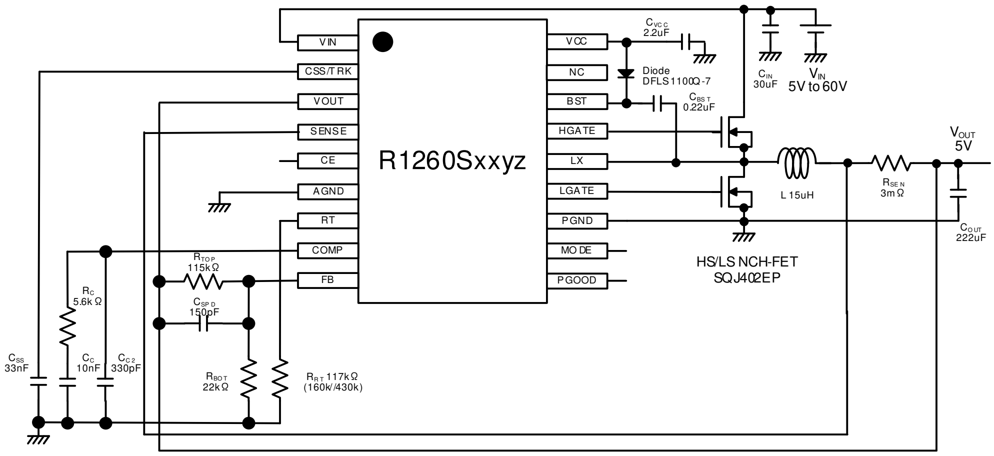
Symbol	Item		Conditions	Min.	Typ.	Max.	Unit
V_{ILIMIT}	Current Limit Threshold Voltage (SENSE – VOUT)	R1260Sxx1z		40	50	64	mV
		R1260Sxx2z		56	70	84	mV
		R1260Sxx3z		88	100	116	mV
$V_{IREVLIMIT}$	Reverse Current Sense Threshold (SENSE – VOUT)	R1260Sxx1z	MODE = "High" or "CLK Input"	-39	-25	-14	mV
		R1260Sxx2z	MODE = "High" or "CLK Input"	-49	-35	-22	mV
		R1260Sxx3z	MODE = "High" or "CLK Input"	-64	-50	-39	mV
$V_{LXSHORTL}$	LX Short to GND Detector Threshold Voltage (VIN – LX)			0.80	1.0	1.2	V
$V_{LXSHORTH}$	LX Short to VCC Detector Threshold Voltage (LX – PGND)			0.32	0.40	0.44	V
V_{CEH}	CE Pin Input Voltage, high			1.3			V
V_{CEL}	CE Pin Input Voltage, low					1.1	V
I_{CEH}	CE Pin Input Current, high		V_{CE} = 60 V	-0.10		2.45	µA
I_{CEL}	CE Pin Input Current, low		V_{CE} = 0 V	-1.00	0	1.00	µA
I_{FBH}	FB Pin Input Current, high		V_{FB} = 2.85 V	-0.10		0.10	µA
I_{FBL}	FB Pin Input Current, low		V_{FB} = 0 V	-0.10		0.10	µA
V_{MODEH}	MODE Pin Input Voltage, high			1.33			V
V_{MODEL}	MODE Pin Input Voltage, low					0.74	V
I_{MODEH}	MODE Pin Input Voltage, high	R1260S01yz R1260S02yz	V_{MODE} = 5 V	7.0	10.7	18.6	µA
		R1260S03yz		3.0	5.3	9.6	
I_{MODEL}	MODE Pin Input Voltage, low		V_{MODE} = 0 V	-1.00	0	1.00	µA
$V_{PGOODOFF}$	PGOOD Pin Output Voltage, low		V_{IN} = 5.0 V, I_{PGOOD} = 1 mA		0.26	0.64	V
$I_{PGOODOFF}$	PGOOD Pin Leakage Current		V_{IN} = 60 V, V_{CE} = 0 V, V_{PGOOD} = 6 V	-0.10	0	0.10	µA
V_{FBOVD1}	FB Pin OVD Threshold Voltage		V_{FB} Rising	V_{FB} x1.070	V_{FB} x1.100	V_{FB} x1.135	V
V_{FBOVD2}			V_{FB} Falling	V_{FB} x1.044	V_{FB} x 1.070	V_{FB} x1.110	V
V_{FBUVD1}	FB Pin UVD Threshold Voltage		V_{FB} Falling	V_{FB} x0.865	V_{FB} x 0.900	V_{FB} x0.936	V
V_{FBUVD2}			V_{FB} Rising	V_{FB} x0.890	V_{FB} x 0.930	V_{FB} x0.970	V
gm (EA)	Trans Conductance Amplifier		V_{COMP} = 1.5 V	0.55	1.00	1.45	mS

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

TYPICAL APPLICATION CIRCUIT



R1260S Typical Application Circuit at 250 kHz / 3.3V

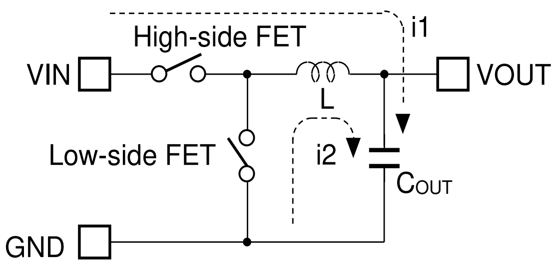


R1260S Typical Application Circuit at 250kHz / 5.0V

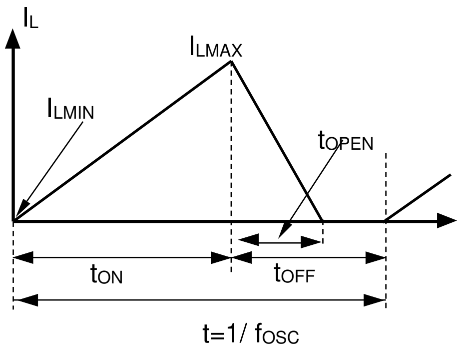
OPERATION

Operation of Step-down Converter

A basic step-down DC/DC converter circuit is illustrated in the following figures. This DC/DC converter charges energy in the inductor when the high-side MOSFET turns on, and discharges the energy from the inductor when the high-side MOSFET turns off and controls with less energy loss, so that a lower output voltage than the input voltage is obtained.



Basic Circuit



Current Through Inductor

Step1. The high-side MOSFET turns on and current IL (= i1) flows, and energy is charged into C_{OUT}. At this moment, I_L increases from I_{LMIN} (= 0) to reach I_{LMAX} in proportion to the on-time period (ton) of the high-side MOSFET turns on and current I_L (= i1) flows, and energy is charged into C_{OUT}. At this moment, I_L increases from I_{LMIN} (= 0) to reach I_{LMAX} in proportion to the on-time period (t_{ON}) of the high-side MOSFET.

Step2. When the high-side MOSFET turns off, the low-side MOSFET turns on in order to maintain I_L at I_{LMAX}, and current I_L (= i2) flows.

Step3. **When MODE = "Low" (VFM/PWM Auto-switching mode),**
If the output current is small, I_L (= i2) decreases gradually and reaches $I_L = I_{LMIN} = 0$ after a time period of t_{OPEN}, and the low-side MOSFET turns off. This case is called as discontinuous mode. The VFM mode is switched if go to the discontinuous mode. If the output current is increased, a time period of t_{OFF} runs out prior to reach of $I_L = I_{LMIN} = 0$. The result is that the high-side MOSFET turns on and the low-side MOSFET turns off in the next cycle. This case is called continuous mode. Upon entering this continuous mode, R1260S will transition to the PWM mode.
When MODE = "High" (Forced PWM mode), MODE = External Clock (PLL_PWM mode),
Since the continuous mode works at all time, the low-side MOSFET turns on until going to the next cycle. That is, the low-side MOSFET must keep "On" to meet $I_L = I_{LMIN} < 0$, when reaches $I_L = I_{LMIN} = 0$ after a time period of t_{OPEN}.

In the PWM mode, the output voltage is maintained constant by controlling t_{ON} with the constant switching frequency (f_{OSC}). In VFM mode, t_{ON} is constant and the output voltage is kept constant by controlling f_{OSC}.

Chip Enable Function

Standby state by entering the "Low" to the CE pin, can be set to the active state by entering the "High". When the CE pin voltage drops below the CE “Low” input voltage (V_{CEL}) of 1.1V, the switching is turned off state. When the CE pin voltage rises above the CE “High” input voltage (V_{CEH}) of 1.3 V, the R1260S boots and begins a soft start.
In order for the current flowing through the VIN pin to be the standby current ($I_{STANDBY}$), the CE pin voltage must be 0.39V or less.
If the chip enable function is not required, connect the CE pin to the VIN pin, etc. so that "High" is input at startup. However, please note that if the VIN pin and CE pin are turned on at the same time at Ta> 105°C, the thermal shutdown detection state may occur.

MODE Switching Function

The R1260S operating mode is switched among the forced PWM mode, PWM/VFM auto-switching mode and PLL_PWM mode, by a voltage or a pulse applied to MODE pin. The forced PWM mode is selected when the voltage of the MODE pin is more than 1.33 V, and the PWM works regardless of a load current. The PWM/VFM auto-switching mode is selected when it is less than 0.74 V, and control is switched between a PWM mode and a VFM mode depending on the load current. See *Forced PWM mode and VFM mode* for details. And see *Frequency Synchronization Function* for the operation on connecting an external clock.

Forced PWM Mode and VFM Mode

The output voltage control methods are selectable between the PWM / VFM Auto-switching mode and the forced PWM mode by using the MODE pin.

Forced PWM Mode

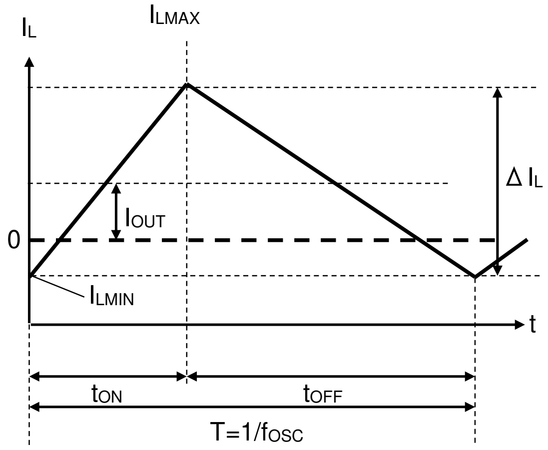
Forced PWM mode is selected when setting the MODE pin to “High”. This mode can reduce the output noise, since the frequency is fixed during light load conditions. Thus, I_{LMIN} becomes less than "0" when I_{OUT} is less than $\Delta I_L/2$. That is, the electric charge, which is charged to C_{OUT}, is discharged via MOSFET for the durations – when I_L reaches “0” from I_{LMIN} during the t_{ON} periods and when I_L reaches I_{LMIN} from “0” during t_{OFF} periods.

But, pulses are skipped to prevent the overvoltage when high-side MOSFET is set to ON under the condition that the output voltage being more than the set output voltage.

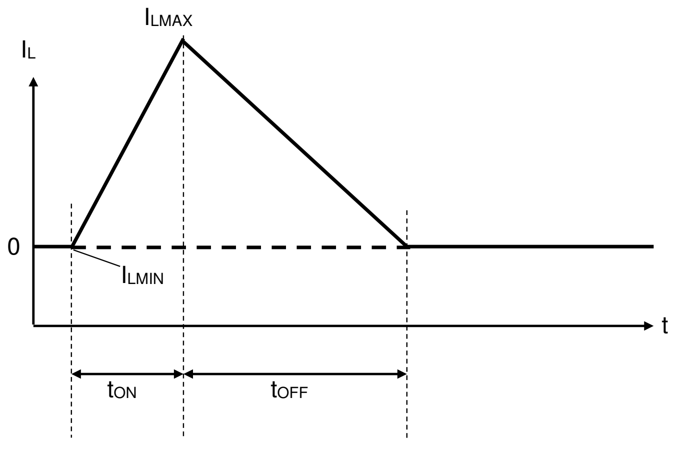
VFM Mode

PWM / VFM Auto-switching mode is selected when setting the MODE pin to “Low”. This mode can automatically switch from PWM to VFM to achieve a high-efficiency during light load conditions. By the VFM mode architecture, the high-side MOSFET is turned on for t_{ON} x 1.54 (Typ.) at the PWM mode under the same condition as the VFM mode when the VFB pin voltage drops below the internal reference voltage (Typ. 0.8 V). After the On-time, the high-side MOSFET is turned off and the low-side MOSFET is turned on. When the inductor current of 0 A is detected, the low-side MOSFET is turned off and the switching operation is stopped (Both of hi- and low-side MOSFETs are OFF). The switching operation restarts when the VFB pin voltage becomes less than 0.8 V.

The On-time at the PWM mode is determined by a resistance, input and output voltages, which are connected to the RT pin. Refer to “*Calculation of VFM Ripple”* for detailed description on the On-time at the VFM mode.



Forced PWM Mode



VFM Mode

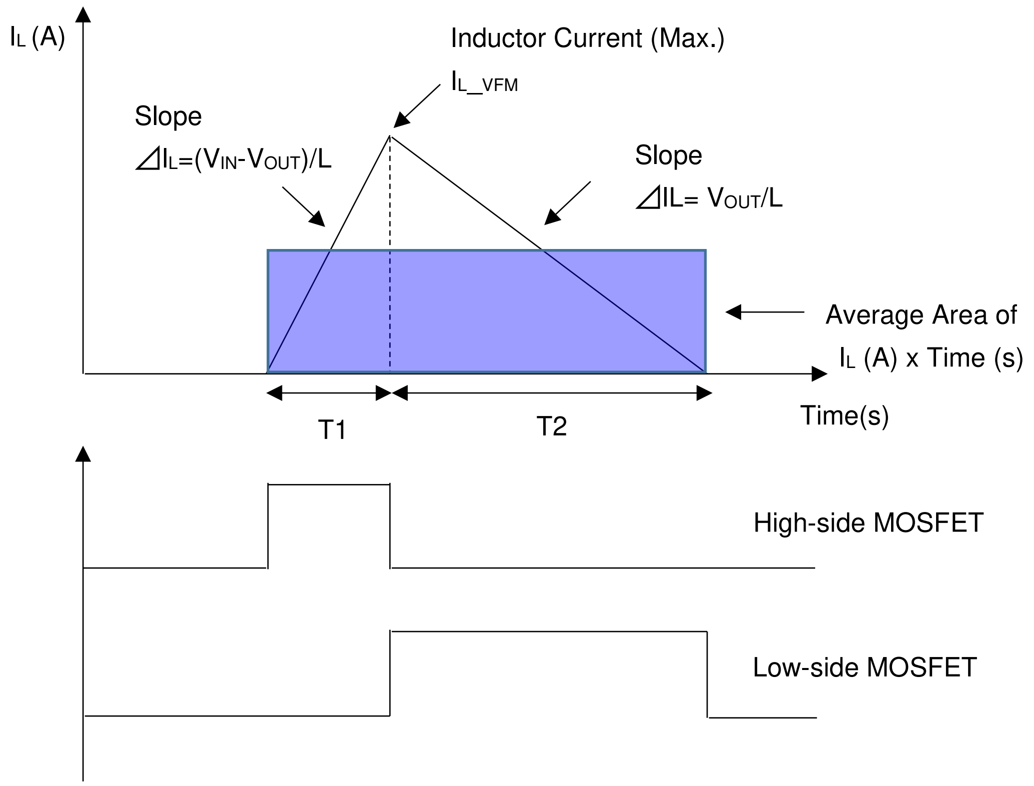
Calculation of VFM Ripple

Calculation example of output ripple voltage (V_{OUT_VFM}) is described. V_{OUT_VFM} can be calculated by Equation 1. And, the maximum value of inductor current (I_{L_VFM}) can be calculated by Equation 2.

$V_{OUT\_VFM} = R_{COUT\_ESR} \times (I_{L\_VFM}) + C_{OEF\_TON\_VFM} \times (I_{L\_VFM} / 2) / f_{OSC} / C_{OUT\_EFF}$ ························ Equation 1

$I_{L\_VFM} = ((V_{IN} - V_{OUT}) / L) \times C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC}$ ··· Equation 2

V_{OUT_VFM} : Output ripple
R_{COUT_ESR} : ESR of output capacitor
I_{L_VFM} : Maximum current of inductor
$C_{OEF\_TON\_VFM}$: Scaling factor of On-time - Typ.1.54X (Design value)
$(V_{IN}-V_{OUT}) / L$: Slope of inductor current
$C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC}$: On-time



Inductor Current Waveform at VFM Mode

Output voltage can be calculated by the following simple equation.

$V_{OUT} = I \times T/C$

I : Current, C : Capacitance, T : Time

Since I is represented by *1/2 x* I_{L_VFM} as the average current, the time of current passing at the VFM mode can be expressed by the following equation.

$T = C_{OEF\_TON\_VFM} / f_{OSC}$

And, the output ripple voltage (V_{OUT_VFM}) is superimposed a voltage for ESR × I, and Equation 1 is determined. But, ESR is so small that it may be ignored if ceramic capacitors are connected in parallel.

The amount of charge to the output capacitor can be calculated by Equation 3.

(High-side MOSFET On-time (T1) + Low-side MOSFET On-time (T2)) × Average amount of current ············ Equation 3

Then, T1 and T2 can be calculated by the following equations, and the time of current passing can be determined.

$T1 = C_{OEF\_TON\_VFM} / f_{OSC} \times V_{OUT} / V_{IN}$ ····· (On-time at VFM)

$T2 = (V_{IN}/V_{OUT}-1) \times T1$ $(0 = I_{L\_VFM} - V_{OUT}/L \times T2)$

$T = T1 + T2$

$= V_{IN} / V_{OUT} \times T1$

$= C_{OEF\_TON\_VFM} / f_{OSC}$

And then, the amount of charge can be determined as Equation 4.

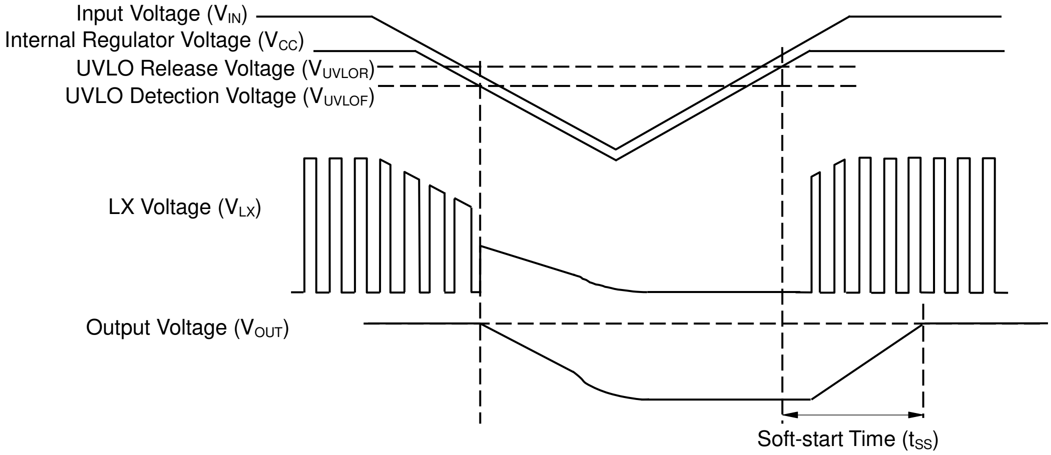
$T \times I_{L\_VFM} /2 = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} /2$ ·· Equation 4

With using above equations, the output ripple voltage (V_{OUT_VFM}) can be calculated by Equation 5.

$V = IT/C = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} / 2 / C_{OUT\_EFF}$ ··· Equation 5

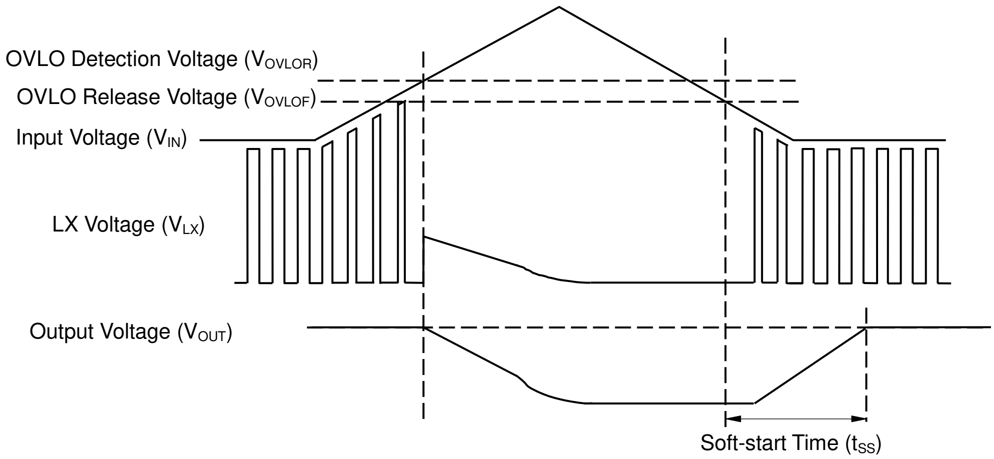
UVLO (Undervoltage Lockout) Function

The UVLO function is a function that prevents malfunction by turning off switching when the VCC pin voltage becomes lower than the UVLO detection voltage (V_{UVLOF}) due to a drop in the input voltage. Since switching stops, the output voltage drops depending on the load and C_{OUT}. When the VCC pin voltage rises above the UVLO release voltage (V_{UVLOR}), the R1260S restarts and begins a soft start.



OVLO (Overvoltage Lockout) Function

The OVLO function is a function to prevent malfunction by turning off switching when the input voltage exceeds the OVLO detection voltage (V_{OVLOR}), 85V (Typ.), and to prevent overvoltage destruction of the high-side MOSFET and low-side MOSFET. Since switching stops, the output voltage drops depending on the load and C_{OUT}. If the input voltage drops below the OVLO release voltage (V_{OVLOF}), 82.8V (Typ.), the R1260S will restart and start a soft start. This function does not guarantee operation above the absolute maximum rating.



Frequency Synchronization Function

The R1260S can synchronize to the external clock being inputted via the MODE pin, with using a PLL (Phase-locked loop). The forced PWM mode is selected during synchronization. The external clock with a pulse-width of 100 ns or more is required. The allowable range of oscillation frequency is 0.5 to 1.5 times of the set frequency[(1)], and the operating guaranteed frequency is in the 150 kHz to 600 kHz range. The R1260S can synchronize to the external clock even if the soft-start works. That is, the R1260S executes the soft-start and the synchronization functions at a time if having started up while inputting an external clock to the MODE pin.
When the maxduty or the duty_over state is caused by reduction in differential between input and output voltages, the device runs at asynchronous to the MODE pin, and it operates in the frequency reduced until one-fourth of the external clock frequency. Likewise, the CLKOUT pin becomes asynchronous to the MODE pin. If making synchronization to the MODE pin, take notice in use under a reduced input voltage.

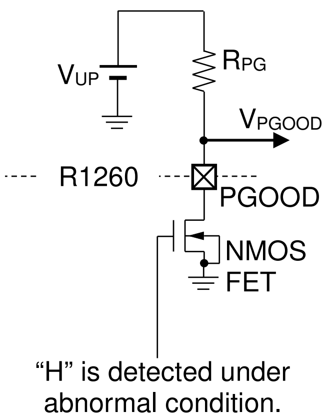
PGOOD (Power Good) Output Function

The power good function with using a NMOS open drain output pin can detect the following states of the R1260S. The NMOS turns on and the PGOOD pin becomes “Low” when detecting them. After the R1260S returns to their original state, the NMOS turns off and the PGOOD pin outputs “High” (PGOOD Input Voltage: V_{UP}).

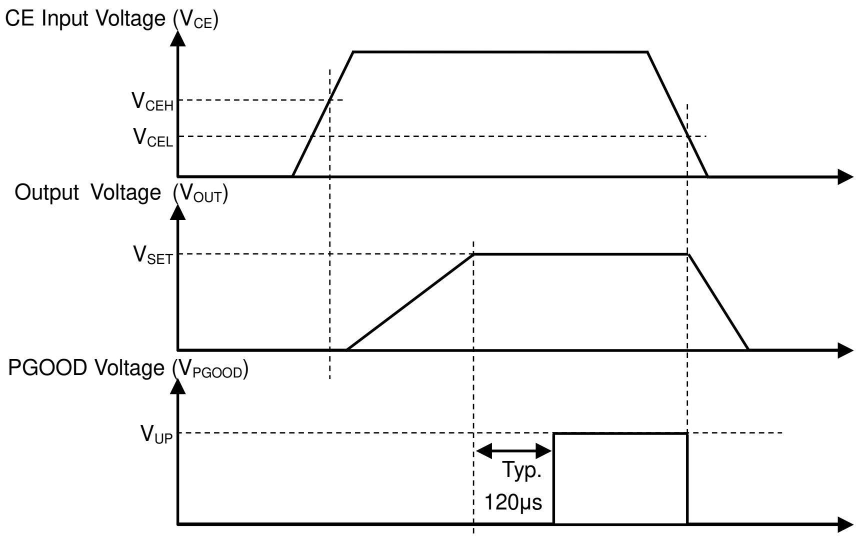
- CE = “Low” (Shut down)
- UVLO (Shut down)
- Thermal Shutdown
- Soft-start time

- at UVD Threshold Voltage Detection
- at OVD Threshold Voltage Detection
- at hiccup-type Protection (when hiccup mode is selected)
- at latch-type Protection (when latch mode is selected)

The PGOOD pin is designed to become 0.64 V or less in “Low” level when the current floating to the PGOOD pin is 1 mA. The use of the PGOOD input voltage (V_{UP}) of 5.5 V or less and the pull-up resistor (RPG) of 10 kΩ to 100 kΩ are recommended. If not using the PGOOD pin, connect it to “Open” or “GND”.



Power Good Circuit Diagram



Power Good Circuit Rise / Fall Sequence

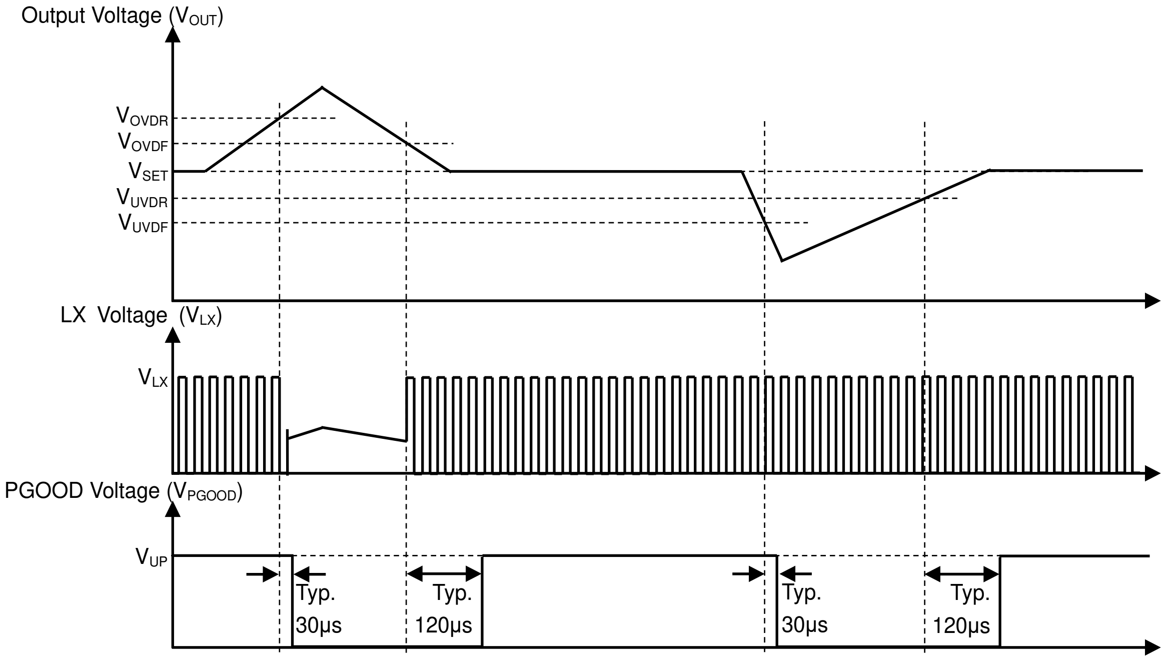
(1) See *Oscillation Frequency Setting* for details of the set frequency.

Under Voltage Detection (UVD)

The UVD function indirectly monitors the output voltage with using the FB pin. The PGOOD pin outputs "Low" when the UVD detector threshold is 90% (Typ.) of V_{FB} and V_{FB} is less than the UVD detector threshold for more than 30 µs (Typ.). When V_{FB} is over 93% (Typ.) of 0.8V, the PGOOD pin outputs "High" after delay time (Typ.120 µs.). And, the hiccup- / latch-type overcurrent protection works when detecting a current limit, an LX power supply protection, or an over voltage protection during the UVD detection.

Over Voltage Detection (OVD)

The OVD function indirectly monitors the output voltage with using the FB pin. Switching stops even if the internal circuit is active state, when detecting the over voltage of V_{FB}. The PGOOD pin outputs "Low" when the OVD detector threshold is 110% (Typ.) of V_{FB} and V_{FB} is over the OVD detector threshold for more than 30 µs (Typ.). When V_{FB} is under 107% (Typ.) of V_{FB}, which is the OVD released voltage, the PGOOD pin outputs "High" after delay time (Typ.120 µs.). Then, switching is controlled by normal operation. The over voltage protection works when an error is caused by a feedback resistor in peripheral circuits for the FB pin.



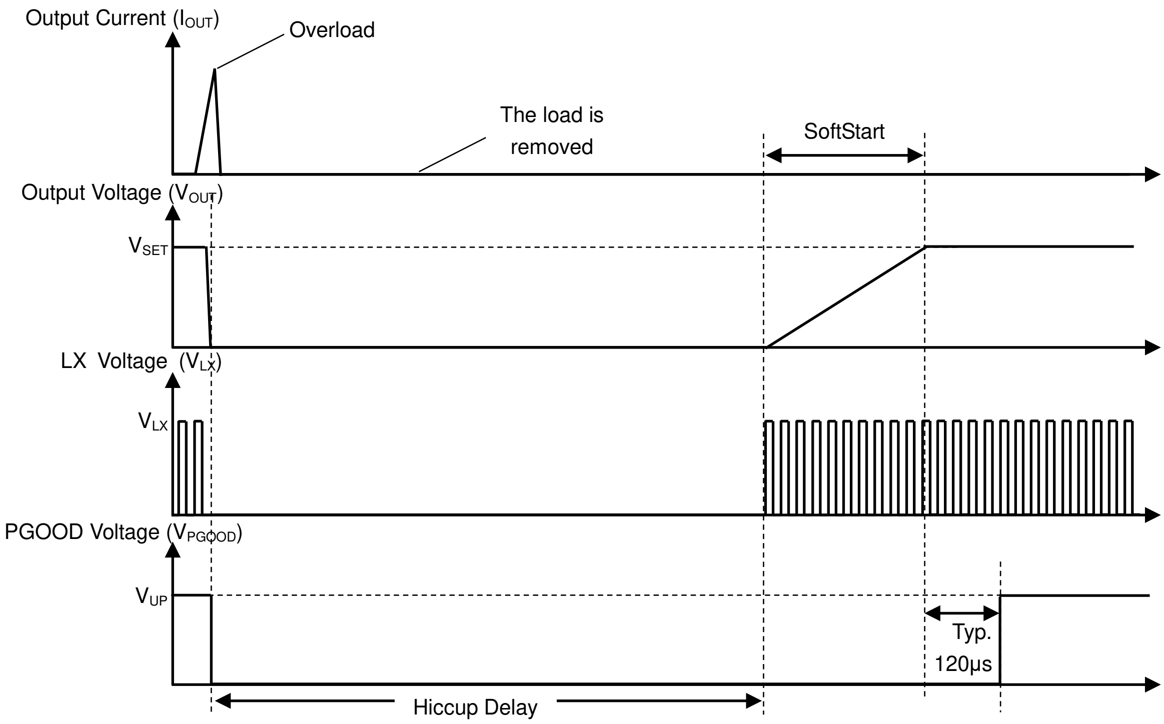
Over Voltage Detection / Under Voltage Detection Sequence

LX Power Supply (VIN Short) / GND (GND Short) Protection

In addition to normal current limit, the R1260S provides the LX power supply / GND short protection to monitor the voltage between the MOSFET's drain and source. Since the current limit function is controlled with an external inductor's DCR or a sense resistance, the current limit function cannot work when a through-current is flowed through the MOSFET and when an overcurrent is generated by shorting the LX pin to VIN/GND. LX power supply protection monitors the voltage between drain and source of the low-side MOSFET during its on period and turns off the MOSFET when the detection threshold is exceeded.
LX ground protection monitors the voltage between drain and source of the high-side MOSFET during its on period and turns off the MOSFET when the detection threshold is exceeded.
This function repeats with each switching. The detect threshold voltage at LX short to GND is 1V(Typ.) and the detect threshold voltage at LX short to VIN is Typ.0.4 V(Typ.). The detecting current is determined by the detect threshold voltage when LX short to VIN / GND (MOSFET_On-resistance x Current).

Hiccup-type / Latch-type Overcurrent Protection

The hiccup-type / latch-type overcurrent protection can work under the operating conditions that is the UVD can function during the current limit or OVP and the LX GND short protection. The latch-type protection can release the circuit by setting the CE pin to “Low” or by reducing V_{IN} to be less than the UVLO detector threshold, when the output is latched off. The hiccup type protection stops switching releases the circuit after the protection delay time 7ms (Typ.). The Hiccup type automatically recovers after the overcurrent protection is activated. And, damage due to the overheating might not be caused because the term to release is long. When the output is shorted to GND, switching of “ON” / “OFF” is repeated until the shorting is released.



Hiccup-Type Overcurrent Protection Timing Chart

Current Limit Function

The current limit function can be to limit the current by the peak current method to turn the high-side MOSFET off when the potential differences between voltage of SENSE pin and VOUT pin is over the current limit threshold voltage. The threshold voltage is selectable among 50 mV / 70 mV / 100 mV. And, the two following detection methods can be selected by external components connected.

A. Detecting Method with R_{SENSE}

The current limit value is detected with the voltage across the inductor that a sense resistance is connected in series. By connecting a resistance with low level of variation, the current limit with high accuracy can achieve.
As a result, be caution that the power loss is caused from the current and R_{SENSE}. The peak current in the current limit inductor can be calculated by the following equation.

Peak current in Current limit inductor (A) = Current limit threshold voltage (mV) / R_{SENSE} (mΩ)

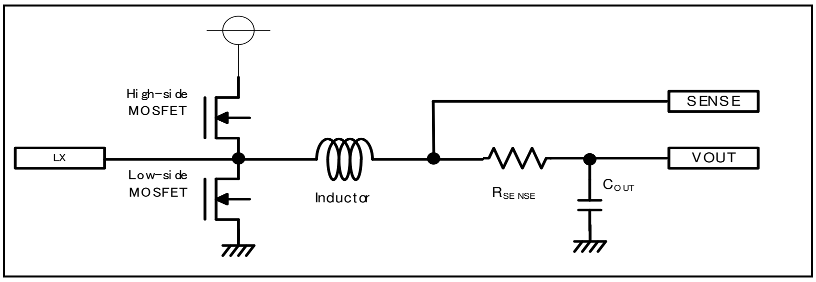


Figure A Detection with Sense Resistance

B. Detecting Method with DCR of Inductor

The current limit value is detected with the DCR of the inductor. The reduction of the loss is minimized since the inductor is in no need of a resistance. But, the SENSE pin requires to connect a resistor and a capacitor to each end of the inductor. Because a constant slope is caused depending on the inductance and the capacitance. Factors causing the poor accuracy of current limit value include the variation in production of the inductor's DCR and the temperature characteristics. R_S and C_S can be calculated by the following equation.

Peak current in Current limit inductor (A) = Current limit threshold voltage (mV) / Inductor's DCR (mΩ)
$C_S = L / (DCR \times R_S)$

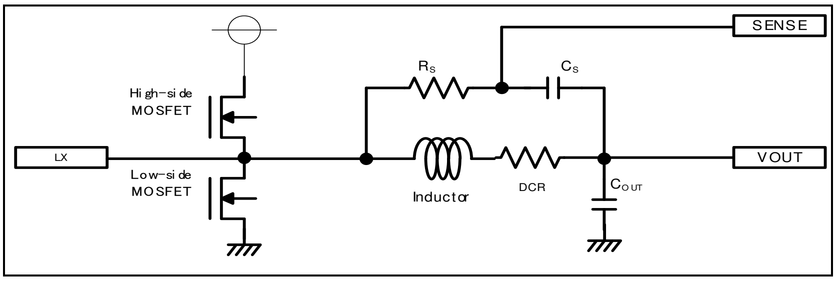


Figure B Detecting with Inductor's DCR

Output Voltage Setting

The output voltage (V_{OUT}) can be set by adjustable values of R_{TOP} and R_{BOT}. The value of V_{OUT} can be calculated by Equation 1 :

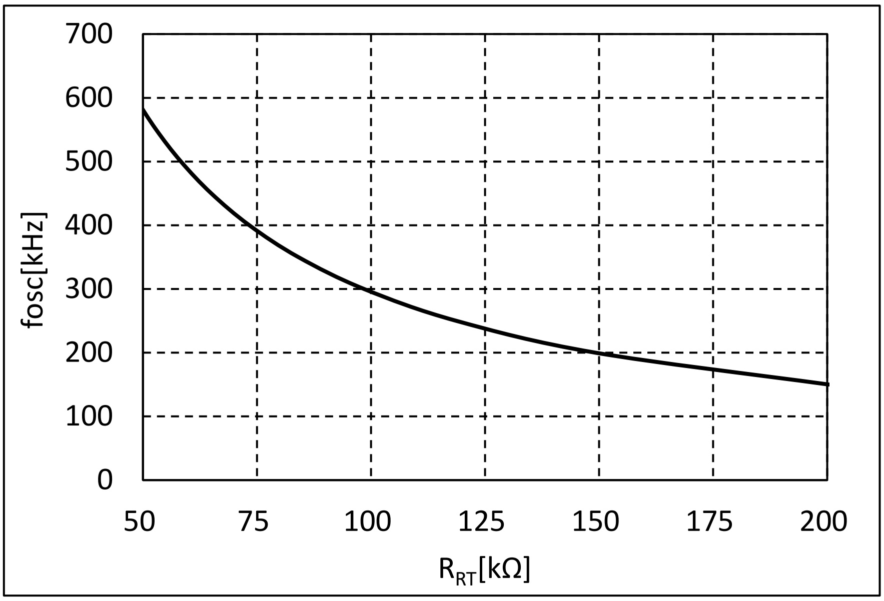
$V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT}$ ································· Equation 1

For example, when setting V_{OUT} = 3.3 V and setting R_{BOT} = 22 kΩ, R_{TOP} can be calculated by substituting them to Equation 1. As a result of the expanding Equation 2, R_{TOP} can be set to 68.8 kΩ.
To make 68.8 kΩ with E24 resistors, connect 62 kΩ and 6.8 kΩ in series. (If the tolerance level of the output voltage is permitted, 68 kΩ may be used.)

R_{TOP} = (3.3 V / 0.8 V - 1) × 22 kΩ
= 68.8 kΩ ································· Equation 2

Oscillation Frequency Setting

Connecting the oscillation frequency setting resistor (R_{RT}) between the RT pin and GND can control the oscillation frequency in the range of 150 kHz to 600 kHz. For example, using the resistor of 100 kΩ can set the frequency of about 300 kHz.
The Electrical Characteristics guarantees the oscillation frequency under the conditions stated below for f_{OSC0} (at R_{RT} = 200 kΩ) and f_{OSC1} (at R_{RT} = 47 kΩ).



R_{RT} [kΩ] = 34064 x f_{OSC} [kHz] ^ (-1.025)

Oscillation Frequency Setting Resistor (R_{RT}) vs. Oscillation Frequency (f_{OSC})

Soft-start Function

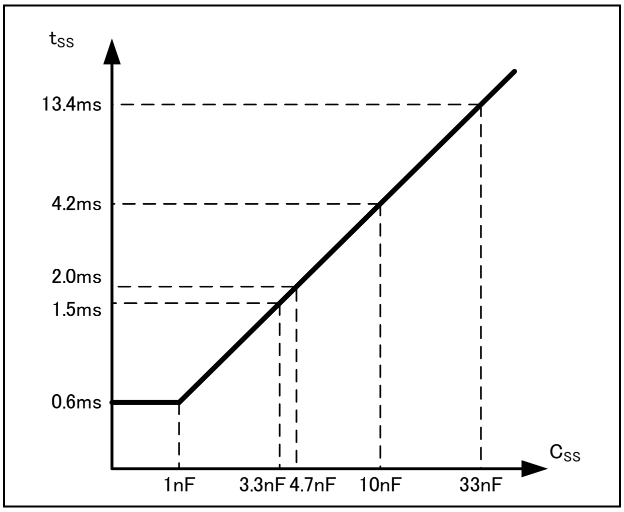
The soft-start time is a time between a rising edge (“High” level) of the CE pin and the timing when the output voltage reaches the set output voltage.
Connecting a capacitor (C_{SS}) to the CSS / TRK pin can adjust the soft-start time (t_{SS}) – provided the internal soft-start time of 600 µs (Typ.) as a lower limit. The adjustable soft-start time (t_{SS2}) is 2.0 ms (Typ.) when connecting an external capacitor of 4.7 nF with the charging current of 2.0µA (Typ.).

Soft start time(T_{SS})[ms] = C_{SS} [nF] / 2.0 [µA] × 0.8 [V]+ 0.16 [ms]

If C_{SS} = 4.7 nF

T_{SS} = 4.7 / 2.0 × 0.8 + 0.16 ≒ 2.0 [ms]

If not required to adjust the soft-start time, set the CSS / TRK pin to “Open” to enable the internal soft-start time (t_{SS1}) of 600 µs (Typ.). If connecting a large capacitor to an output signal, the overcurrent protection or the LX GND short protection might run. To avoid these protections caused by starting abruptly when reducing the amount of power current, soft-start time must be set as long as possible.
Each of soft-start time (tss1/ tss2) is guaranteed under the conditions described in the chapter of “Electrical Characteristics”.

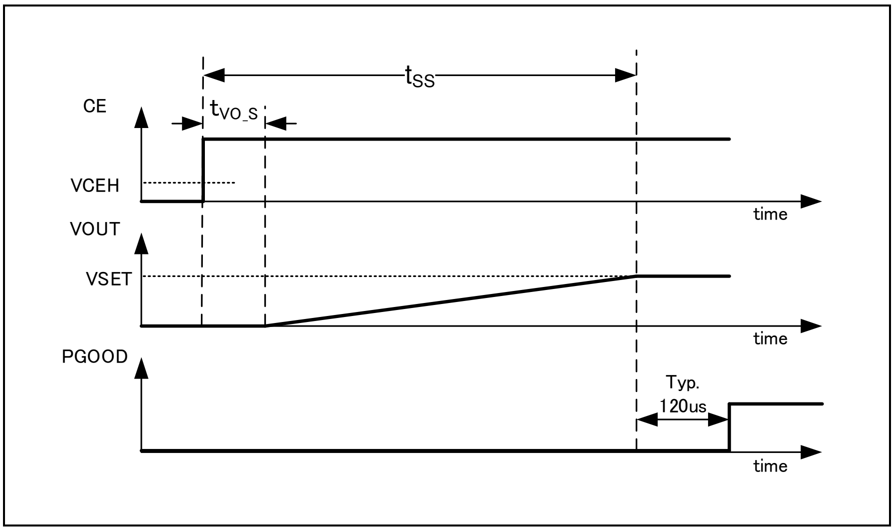


C_{SS} [nF] = (t_{SS} [ms] - t_{VO_S} [ms]) / 0.8[V] × 2.0 [μA]

t_{SS}: Soft-start time (ms)

t_{VO_S}: Time period from CE = "High" to VOUT's rising (Typ. 0.160 ms)

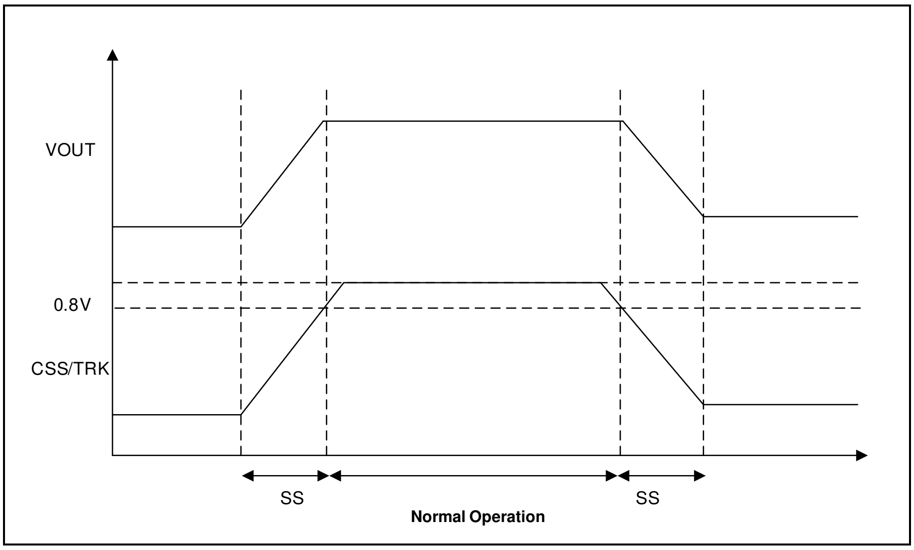
Soft-start Time Adjustable Capacitor (C_{SS}) vs. Soft-start Time (t_{SS})



Soft-start Sequence

Tracking Function

Applying an external tracking voltage to the CSS / TRK pin can control the soft-start sequence – provided that the lowest internal soft-start time is limited to 600 µs (Typ.). Since V_{FB} becomes nearly equal to $V_{CSS/TRK}$ at tracking, start timing and soft-start can be easily designed. The available voltage at tracking is between 0 V and 0.8 V. If the tracking voltage is over 0.8 V, the internal reference voltage of 0.8 V is enabled. Also, turning off slope can be set by forcing $V_{CSS/TRK}$ to from 0.8 V (Typ.) to 0V, since the R1260S supports both of up- and down- tracking.



Tracking Sequence

Min. ON-time

The min. ON time (Max. 170 ns), which is determined in the R1260S internal circuit, is a minimum time to turn high-side MOSFET on. The R1260S cannot generate a pulse width less than the min. ON time. Therefore, settings of the output set voltage and the oscillator frequency are required so that the minimum step-down ratio [V_{OUT}/V_{IN} x (1 / f_{OSC})] does not stay below 170ns. If staying below 170 ns, the pulse skipping will operate to stabilize the output voltage. However, the ripple current and the output voltage ripple will be large.

Min. OFF-time

By the adoption of bootstrap method, the high-side MOSFET, which is used as the R1260S internal circuit for the min. OFF time, is used a NMOS. The voltage sufficient to drive the high-side MOSFET must be charged. Therefore, the min. OFF time is determined from the required time to charge the voltage. By the adoption of the frequency's reduction method by one-quarter of a set value (Min.), if the input-output difference voltage becomes small or load transients are caused, the OFF period can be caused once in four-cycle period of normal cycle. As a result, the min. OFF time becomes 190 ns (Typ.) substantially, and the maximum duty cycle can be improved.

Through-current Protection

The HGATE pin voltage (V_{HGATE}) and the LGATE pin voltage (V_{LGATE}) are monitored to protect a through-current caused by an external MOSFET. In the case of turning-on the low-side MOSFET, after a difference between V_{HGATE} - LX pin voltage (V_{LX}) becomes 1V or less, increasing V_{LGATE} can prevent not to turn on both of the high-side and low-side MOSFETs at a time and thereby prevent the through-current. In the case of turning-on the high-side MOSFET, after a difference between V_{LGATE} - GND (PGND pin voltage) becomes 1 V or less, increasing a difference between V_{HGATE} - V_{LX} can prevent the through-current.

Reverse Current Limit Function

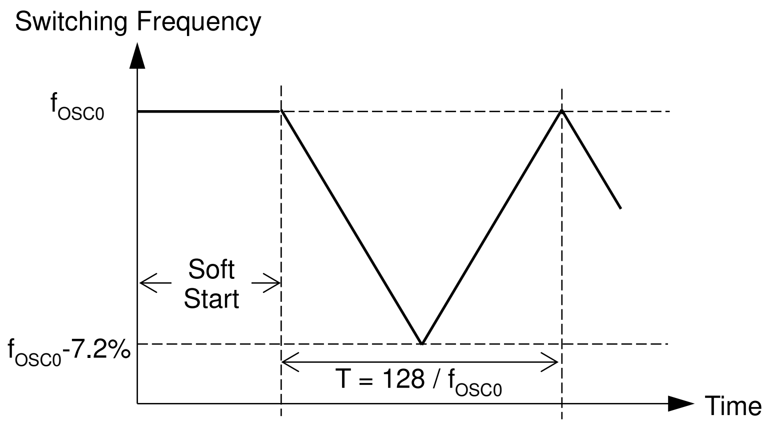
The reverse current limit function can be to limit the current by the peak current method to turn the low-side MOSFET off when the potential differences between voltage of VOUT and SENSE is over the reverse current limit threshold voltage.
Reverse current limit inductor peak current is calculated by the following equation.

Reverse current limit inductor peak current (A) = Reverse current limit threshold voltage (mV) / R_{SENSE} (mΩ)

This function mainly operates when the output is tied to a voltage higher than the set output voltage in some reasons.

SSCG (Spread Spectrum Clock Generator)

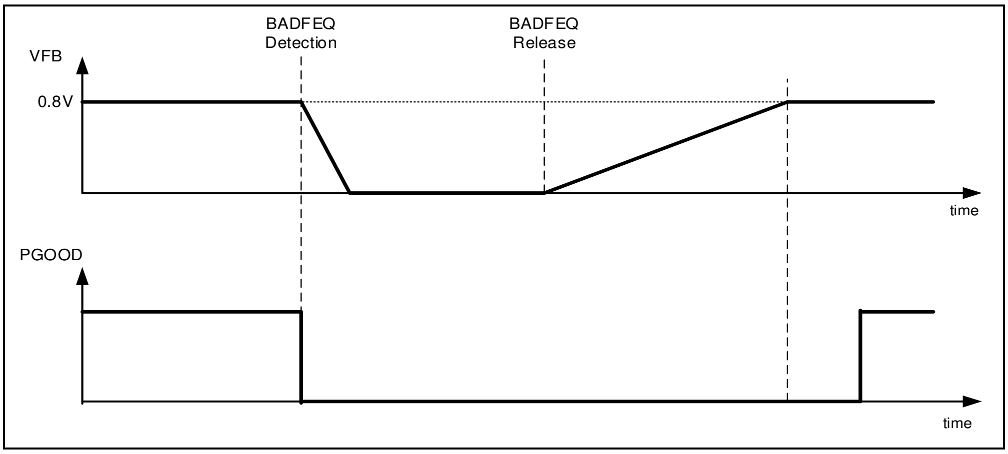
In order to reduce the interference of conductive / radioactive noise, we have prepared an option of SSCG (Spread Spectrum Clock Generator) function. SSCG function is valid during PWM operation. SSCG suppresses the peak noise by spreading the switching frequency in a specific range. In this option, the switching frequency (f_{OSC}) changes in between -7.2% (Typ.) and the original frequency. The modulation cycle is f_{OSC} / 128. See the figure below.
SSCG is valid only during PWM operation and disabled during VFM operation. Also note that the SSCG is invalid when an external clock is applied.
At soft start, the switching frequency is not modulated and operates at the set frequency or the external clock frequency.



Switching frequency modulation diagram by SSCG

Bad Frequency (BADFREQ) Protection

If a resistor connected RT pin is open or short, the switching of the R1260S stops. In other words, when a current equivalent to 1000 kHz (Typ.) or more or 100 kHz (Typ.) or less flows to the RT pin, the R1260S stops switching and the internal state becomes before the soft-start condition. The R1260S will restart under the normal control with soft start when recovering from the abnormal condition.



BADFREQ Detection / Release Sequence

Thermal shutdown function

When the junction temperature exceeds the thermal shutdown detection temperature (Typ.160°C), this IC cuts off the output and suppresses the self-heating.
When the junction temperature falls below the thermal shutdown release temperature (Typ.140°C), this IC will restart with the soft start operation.

TECHNICAL NOTES

The performance of power source circuits using this IC largely depends on peripheral circuits. When selecting the peripheral components, please consider the conditions of use. Do not allow each component, PCB pattern or the IC to exceed their respected rated values (voltage, current, and power) when designing the peripheral circuits.

- It is recommended to mount all the external components on the same layer as the IC on board. External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- Since the current loop of a switching regulator changes with each switching, the current changes significantly and high-frequency noise may be generated due to parasitic capacitance and inductance. Design the board layout so that the current loop length is as short as possible. Also, make sure that the current loops do not overlap the line from C_{OUT} to the subsequent load side to avoid the bad impact from the output voltage ripple.

- AGND and PGND for the controller must be wired to the GND line at the low impedance point of the same layer with C_{IN} and C_{OUT}. Reduce the impedance between the AGND and PGND of IC

- It is recommended that the C_{IN}, high-side, and low-side MOSFETs be placed on the same layer as the IC on PCB. If vias are used and placed on a different layer from the IC, the parasitic inductance of vias may affect the ringing of the LX pin voltage and increase noise.

- R_{TOP}, R_{BOT}, and C_{SPD} should be set close to the FB pin, but mount them away from the inductor, LX pin, and BST pin to avoid their noise.

- Place a capacitor (C_{BST}) as close as possible to the LX pin and the BST pin. If controlling slew rate for EMI, a resistor (R_{BST}) should be in series between the BST pin and the capacitor (C_{BST}), but not be in series to MOSFET for HGATE and LGATE pins. Because connecting the resistor in series to the MOSFET becomes a cause of a through-current.

- The tab on the bottom of the HSOP-18 package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, set via to release the heat to the other layer in the connecting part of the tab on the bottom. Likewise, thermal dissipation for MOSFET is required.

- The MODE pin requires the "High" / "Low" voltages with the high stability when the forced PWM mode (MODE = “High”) or the VFM mode (MODE = “Low”) is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as “High” level or the AGND pin as “Low” level is recommended. If connecting to the PGND pin as noisy, a malfunction may occur. Avoid the use of the MODE pin being “Open”.

- If V_{OUT} is a minus potential, the setup cannot occur.

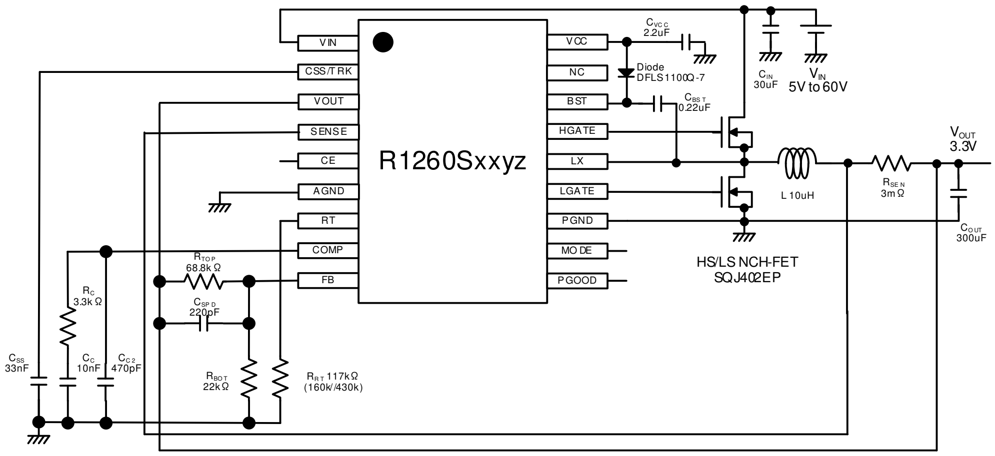
- The power for the controller and for the high-side MOSFET must be used on the same power supply, since the internal slope compensation is applied as the power supply voltage of the high-side MOSFET is equal to the controller's. If applying the other power supply voltage, the controller will become unstable owing to the inappropriate slope compensation.

- The thermal shutdown function prevents the IC from danger in smoke or burn, but not to ensure the reliability of the IC or to keep it below the absolute maximum rating. In addition, it is not effective against the heat generated by abnormal condition such as latch-up and overvoltage forcing.

- Do not design with depending on the thermal shutdown function of this IC as the system protection. The thermal shutdown function is designed for this IC.

APPLICATION INFORMATION

Typical Application Circuit



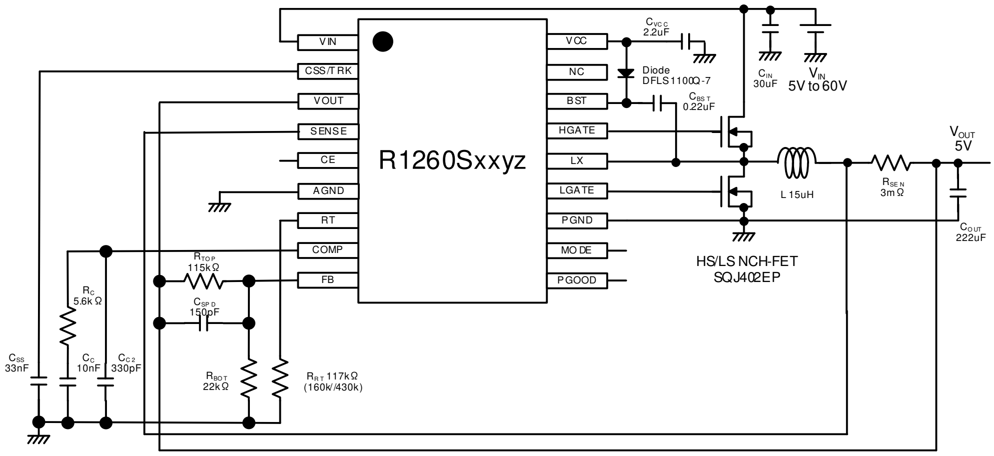
R1260S Typical Application Circuit at 250 kHz / 3.3V

Symbol	Capacitor	Parts Number	Maker
C_{IN}	10µF*3(para)	CGA9N3X7S2A106K	TDK
C_{OUT}	100µF*3(para)	CKG57NX7S1C107M	TDK
C_{BST}	0.22µF	GCM188R71E224KA55D	muRata
C_{VCC}	2.2µF	GCM21BR71E225KA73L	muRata

Symbol	Inductance	Parts Number	Maker
L	10µH	IHLP5050FDER100M5A	VISHAY

Symbol	FET	Parts Number	Maker
FET	MOSFET N-CH	SQJ402EP	VISHAY

Symbol	Diode	Parts Number	Maker
Diode	Diode	DFLS1100Q-7	DIODES



R1260S Typical Application Circuit at 250 kHz / 5.0V

Symbol	Capacitor	Parts Number	Maker
C_{IN}	10µF*3(para)	CGA9N3X7S2A106K	TDK
C_{OUT}	100µF*2+22µF*1(para)	CKG57NX7S1C107M	TDK
		CGA6P1X7R1C226M	TDK
C_{BST}	0.22µF	GCM188R71E224KA55D	muRata
C_{VCC}	2.2µF	GCM21BR71E225KA73L	muRata

Symbol	Inductance	Parts Number	Maker
L	15µH	IHLP5050FDER150M5A	VISHAY

Symbol	FET	Parts Number	Maker
FET	MOSFET N-CH	SQJ402EP	VISHAY

Symbol	Diode	Parts Number	Maker
Diode	Diode	DFLS1100Q-7	DIODES

Selection of External Components

External components and its value required for R1260S are described. Each value is reference value at initial.
Since inductor's variations and output capacitor's effective value may lead a drift of phase characteristics, adjustment to a unity-gain and phase characteristics may be required by evaluation on the actual unit.

Inductor

- Choose an inductor that has small DC resistance, has sufficient allowable current and is hard to cause magnetic saturation. The inductance value must be determined with consideration of load current under the actual condition. If the inductance value of an inductor is extremely small, the peak current of LX may increase along with the load current. As a result, the current limit circuit may start to operate when the peak current of LX reaches to "LX limit current".

Capacitor

- Choose a capacitor that has a sufficient margin to the drive voltage ratings with consideration of the DC bias characteristics and the temperature characteristics.
- Ceramic capacitors are recommended for C_{IN} and C_{OUT}. If combined use of a ceramic and an electrolyte capacitors, the stable operation will improve since the margin becomes bigger. Choose the electrolyte capacitor with the lowest possible ESR with consideration of the allowable ripple current rating (I_{RMS}). I_{RMS} can be calculated by the following equation.
  $I_{RMS} \fallingdotseq I_{OUT}/V_{IN} \times \sqrt{\{V_{OUT} \times (V_{IN} - V_{OUT})\}}$

MOSFET

- Gate – Source Voltage
  When considering variations in production and margin, a MOSFET with a withstand voltage of 10 V or more is recommended despite the 5 V high and low driver.
- Gate Threshold Voltage
  Choose a MOSFET with the threshold voltage between 1.0 V (Min.) and 3.4 V (Max.) with consideration of variations in production and margin.
- Drain Current
  Choose a MOSFET having a sufficient margin with consideration of peak current and limit current.
- Input Capacitor (C_{ISS})
  As an index of performance, C_{ISS}: 1000pF ～ 2000pF
- On-resistance (R_{DS} (on)) & All Gate Capacitance (Qg)
  Choose a MOSFET with the lowest possible characteristics because having an influence on efficiency. Generally, a high-performance MOSFET is rated that R_{DS} x Qq (performance figure) is small.
- Since test specifications vary with MOSFET makers, it is necessary to confirm the application with the R1260S implemented on a board system.

Diode

- A Schottky barrier diode with a small forward voltage (V_F) is recommended. If the V_F is large, the BST pin voltage will drop, and the gate drive voltage of the MOSFET will drop, which may deterioration efficiency. Select a Schottky barrier diode based on V_F = 0.5V (at I_F = 100mA) or less.

- If the reverse current (I_R) becomes large at high temperature, it may cause thermal runaway, which may lead to IC destruction. Use a diode with as low an I_R as possible.

- At both ends of the diode is applied a voltage between the BST pin -VCC pin. Considering the ringing of the BST pin voltage and the drop of the VCC voltage, it is recommended to use a diode with "maximum input voltage (V_{IN}) + 6V" or higher voltage rating.

1. Determination of Requirements

Determine the frequency, the output capacitor, and the input voltage required. For reference values, parameters listed in the following table will be used to explain each equation.

Parameter	Value
Output Voltage (V_{OUT})	3.3 V
Output Current (I_{OUT})	5 A
Input Voltage (V_{IN})	48 V
Input Voltage Range	20 V to 60 V
Frequency (f_{OSC})	250 kHz
ESR of Output Capacitor (R_{COUT_ESR})	3 mΩ

2. Selection of Unity-gain Frequency (f_{UNITY})

The unity-gain frequency (f_{UNITY}) is determined by the frequency that the loop gain becomes “1” (zero dB). It is recommended to select within the range of one-sixth to one-tenth of the oscillator frequency (f_{OSC}). Since the f_{UNITY} determines the transient response, the higher the f_{UNITY}, the faster response is achieved, but the phase margin will be tight. Therefore, it is required that the f_{UNITY} can secure the adequate stability. As for the reference, the f_{UNITY} is set to 12.5 kHz.

3. Selection of Inductor

After the input and the output voltages are determined, a ripple current (ΔI_L) for the inductor current is determined by an inductance (L) and an oscillator frequency (f_{OSC}). The ripple current (ΔI_L) can be calculated by Equation 1.

$\Delta I_L = (V_{OUT} / L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$ ······ Equation 1

V_{IN_MAX} : Maximum input voltage

The core loss in the inductor and the ripple current of the output voltage become small when the ripple current (ΔI_L) is small. But, a large inductance is required as shown by Equation 1. The inductance can be calculated by Equation 2 when a reference value of ΔI_L assumes 30% of I_{OUT} is appropriate value.

$L = (V_{OUT} / \Delta I_L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$ ······ Equation 2

$= (V_{OUT} / (I_{OUT} \times 0.3) / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$

The inductance can be calculated by substituting each parameter to Equation 2.

$L = (3.3\ V / 5\ A / 250\ kHz) \times (1 - 3.3\ V / 60\ V)$

$= 8.32\ \mu H$

When selecting the inductor of 6.8µH as an approximate value of the above calculated value, ΔI_L can be shown as below.

$\Delta I_L = (3.3\ V / 6.8\ \mu H / 250\ kHz) \times (1 - 3.3\ V / 60\ V)$

$= 1.834\ A$

when used in the automatic switching mode (MODE = "Low"), consider the maximum value of the offset voltage of the reverse current detection comparator for detecting a continuous current mode and discontinuous mode. Select L for which the calculation result of Equation 2 satisfies the following Equation 3.

$\Delta I_L > (10\ mV / R_{ONL}\ [m\Omega]) * 2$ ······ Equation 3

$= 10\ mV / 11.6\ m\Omega * 2$

$= 1.724\ A$

R_{ONL}: ON resistance of low-side MOSFET

Note that if Equation 3 is not met, PWM mode may not switch to VFM mode at light loads. In that case, reduce the inductance value and increase ΔIL, or reselect the low-side MOSFET with a large R_{ONL}.

4. Setting of Output Capacitance

The output capacitance (C_{OUT}) must be set to meet the following conditions.

■ Calculation based on phase margin

To secure the adequate stability, it is recommended that the pole frequency (f_{P_OUT}) is set to become equal or below one-fourteenth of the unity-gain frequency. The pole frequency (f_{P_OUT}) can be calculated by Equation 4.

$$f_{P\_OUT} = 1/(2 \times \pi \times C_{OUT\_EFF} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR}))$$

……………Equation 4

C_{OUT_EFF} : Output capacitance (effective value)
R_{OUT_MIN} : Output resistance at maximum output current

$$R_{OUT\_MIN} = V_{OUT} / I_{OUT} = 3.3\ V / 5\ A = 0.66\ \Omega$$

Can be expressed by substituting $f_{P\_OUT} = f_{UNITY} / 14$ to Equation 4.

$$C_{OUT\_EFF} = 14 / (2 \times \pi \times f_{UNITY} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR}))$$

……………Equation 5

Then, the output capacitance (effective value) can be calculated by substituting each parameter to Equation 5.

$$C_{OUT\_EFF} = 14 / (2 \times \pi \times 12.5\text{kHz} \times ((0.66\Omega \times 2 \times \pi \times 250\ \text{kHz} \times 6.8\ \mu\text{H}) / (0.66\Omega + 2 \times \pi \times 250\text{kHz} \times 6.8\mu\text{H}) + 3\text{m}\Omega)) = 285.4\ \mu\text{F}$$

■ Calculation based on ripple at PWM mode

With using the calculated value of C_{OUT}, the amount of ripple at the PWM mode can be shown as Equation 6 and Equation 7.

$I_{L\_PWM} = ((V_{IN\_MAX} - V_{OUT}) / L) \times V_{OUT} / V_{IN\_MAX} / f_{OSC}$ ……… Equation 6
$V_{OUT\_PWM} = R_{COUT\_ESR} \times (I_{L\_PWM}) + (I_{L\_PWM} / 2) / f_{OSC} / C_{OUT\_EFF}$ ……… Equation 7

IL_PWM: maximum inductor current at PWM
V_{OUT_PWM} : Maximum output ripple at PWM

PWM ripple, must be set to be equal to or less than the about 10 ~ 15mV. If V_{OUT_PWM} is over the target value, the output capacitance must be calculated by Equation 8.

$C_{OUT\_EFF} = (I_{L\_PWM} / 2) / f_{OSC} / (V_{OUT\_PWM} - R_{COUT\_ESR} \times (I_{L\_PWM}))$ ……… Equation 8

Substituting each parameter into Equation 8, the output capacitance (effective value) is as follows.

C_{OUT_EFF} = 1.724 A / 2 / 250 kHz / (15 mV – 3mΩ × 1.724 A)

= 350.8 µF

It is recommended that the output capacitance is set to become equal or over the effective value calculated by Equation 5 and 8.

When using in the automatic switching mode (MODE = ”Low”), also consider and select “Calculation based on ripple at VFM mode” described later.

The output capacitance (effective value), which is derated depending on the DC voltage applied, can be calculated by Equation 9. Refer to “*Capacitor Manufacture’s Datasheet”* for details about derating.

$C_{OUT\_EFF} = C_{OUT\_SET} \times (V_{CO\_AB} - V_{OUT}) / V_{CO\_AB}$ ··Equation 9

C_{OUT_SET} : Output capacitor’s spec

V_{CO_AB} : Capacitor’s voltage rating

With using Equation 9, the effective value is calculated to become 350.8 µF or more. The output voltage (C_{OUT}) can be shown as below when V_{CO_AB} is 16 V.

$C_{OUT\_SET} > C_{OUT\_EFF} / ((V_{CO\_AB} - V_{OUT}) / V_{CO\_AB})$

C_{OUT_SET} > 350.8µF / ((16 - 3.3) / 16)

C_{OUT} > 441.9 µF

As the calculated result, C_{OUT} selects a capacitor of 470 µF (the effective value is 373.1 µF).

PWM ripple at this time is as follows from the formula 7.

V_{OUT_PWM} = 3 mΩ × 1.724 A + (1.724 A / 2) / 250 kHz / 373.1 µF

= 14.41 mV

■ Calculation based on ripple at VFM mode

With using the calculated value of C_{OUT}, the amount of ripple at the VFM mode can be shown as Equation 10 and Equation 11. It is not necessary to consider this parameter when using forced PWM.

$I_{L\_VFM} = ((V_{IN\_MAX}-V_{OUT}) / L) \times C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN\_MAX} / f_{OSC}$ ······································· Equation 10

$V_{OUT\_VFM} = R_{COUT\_ESR} \times (I_{L\_VFM}) + C_{OEF\_TON\_VFM} \times (I_{L\_VFM} / 2) / f_{OSC} / C_{OUT\_EFF}$ ························· Equation 11

I_{L_VFM} : Maximum current of inductor
$C_{OEF\_TON\_VFM}$: On-time scaling (multiples of PWM_ON time)
V_{OUT_VFM} : Maximum output ripple

$C_{OEF\_TON\_VFM}$ can be calculated by 1.54 times (Typ.) as the design value. The ripple value can be calculated by substituting each parameter to Equation 10 and Equation 11.

$I_{L\_VFM} = ((60\ V - 3.3\ V) / 6.8\ \mu H) \times 1.54 \times 3.3\ V / 60\ V / 250\ kHz$
$= 2.824\ A$

$V_{OUT\_VFM} = 3\ m\Omega \times 2.824\ A + 1.54 \times (2.824\ A / 2) / 250\ kHz / 373.1\ \mu F$
$= 31.78\ mV$

However, if V_{OUT_VFM} is set too small, the inductor current may be superimposed by continuous switching during VFM mode operation. Thus, the VFM ripple voltage may increase, or the inductor current may become unstable, causing the phenomenon of fluctuating between PWM mode and VFM mode.
Confirm that the VFM ripple voltage satisfies the following equation 12.

$V_{OUT\_VFM} > V_{OUT\_PWM} / 2 + 15.3mV$ ·· Equation 12
$= 14.41mV / 2 + 15.3mV$
$= 22.51mV$

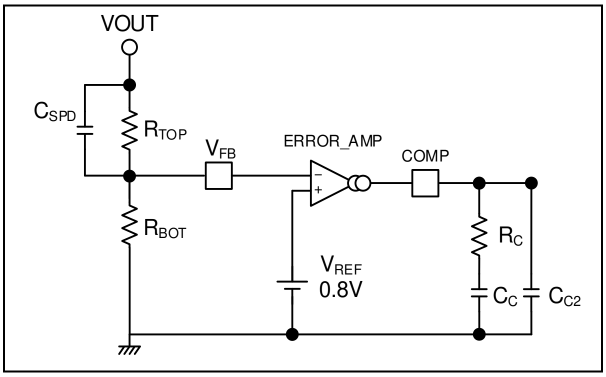
Equation 12 is a conditional expression for not switching in succession when switching from the PWM mode to the VFM mode.
VFM ripple voltage in the calculation example satisfies Equation 12.
If Equation 12 cannot be met, adjust the COUT value. The condition of the capacity value can be calculated as follows.

$C_{OUT\_EFF} < [(1.54^2 - 0.5) \times I_{L\_PWM} / 2 / f_{OSC}] / [15.3mV - R_{COUT\_ESR} \times (1.54 - 0.5) \times I_{L\_PWM}]$ ····· Equation 13
$= 650.46\ [\mu F]$

The effective value C_{OUT}_EFF of C_{OUT} in the calculation example satisfies the above equation 13. If there is no capacity value condition that satisfies the above, reduce the inductance value in order to increase the inductor current.

5. Designation of Phase Compensation

Since the current amplifier for the voltage feedback is output via the COMP pin, the phase compensation is achieved with using external components. The phase compensation is able to secure stable operation with using an external ceramic capacitor and the phase compensation circuit.



Connection Example for External Phase Compensation Circuit

■ Calculation of R_C

The phase compensation resistance (R_C) to set the calculated unity-gain frequency can be calculated by Equation 14.

$R_C = 2 \times \pi \times f_{UNITY} \times V_{OUT} \times C_{OUT\_EFF} / (g_{m\_ea} \times V_{REF} \times g_{m\_pwr})$ ·· Equation 14

g_{m_ea} : Error amplifier of g_m
V_{REF} : Reference voltage (0.8 V)
g_{m_pwr} : power level of g_m

$g_{m\_pwr} \times \Delta V_S = \Delta I_L$
$g_{m\_ea} / \Delta V_S = M \times 10$ ^ $(-6) \times f_{OSC} / V_{OUT}$
$g_{m\_ea} \times g_{m\_pwr} = M \times 10$ ^ $(-6) \times \Delta I_L \times f_{OSC} / V_{OUT}$ ·· Equation 15

ΔV_S : Output amplitude of the slope circuit
M : Slope Coefficient
M = 0.148 (R1260S01yz) , 0.298 (R1260S02yz) , 0.576 (R1260S03yz)

R_C can be calculated by substituting Equation 15 to Equation 14.

$R_C = 2 \times \pi \times f_{UNITY} \times V_{OUT} \times C_{OUT\_EFF} / (V_{REF} \times M \times 10$ ^ $(-6) \times \Delta I_L \times f_{OSC} / V_{OUT})$
$= 2 \times \pi \times 12.5\ kHz \times 3.3\ V \times 373.1\ \mu F / (0.8 \times 0.298 \times 10$ ^ $(-6) \times 1.724A \times 250\ kHz / 3.3\ V)$
$= 3.105\ k\Omega \fallingdotseq 3.3\ k\Omega$ ※For R1260S02yz

■ Calculation of C_C

C_C must be calculated by Equation 4 so that the zero frequency of the error amplifier meets the highest pole frequency (f_{P_OUT}). Then, f_{P_OUT} = 0.683 kHz is determined by calculation of Equation 16.

$C_C = 1 / (2 \times \pi \times R_C \times f_{P\_OUT})$ ············ Equation 16
$= 1/ (2 \times 3.14 \times 3.3\ k\Omega \times 0.683\ kHz)$
$= 70.65\ nF \fallingdotseq 68\ nF$

■ Calculation of C_{C2}

C_{C2} can be calculated by two different calculation methods to vary from the zero frequency (f_{Z_ESR}) depending on the ESR of a capacitor. f_{Z_ESR} can be calculated by Equation 17.

$f_{Z\_ESR} = 1 / (2 \times \pi \times R_{COUT\_ESR} \times C_{OUT\_EFF})$ ············ Equation 17
$= 142.2\ kHz$

[When the zero frequency is lower than f_{OSC} / 2]

C_{C2} sets the pole to f_{Z_ESR}.

$C_{C2} = R_{COUT\_ESR} \times C_{OUT\_EFF} / R_C$ ············ Equation 18

[When the zero frequency is higher f_{OSC} / 2]

C_{C2} sets the pole to f_{OSC} / 2 so as to be a noise filter for the COMP pin.

$f_{OSC} / 2 = 1 / (2 \times \pi \times R_C \times C_{C2})$
$C_{C2} = 2 / (2 \times \pi \times R_C \times f_{OSC})$ ············ Equation 19

In the reference example, C_{C2} is used as the noise filter for the COMP pin because of being higher than f_{OSC}/2.

$C_{C2} = 385.83\ pF \fallingdotseq 330\ pF$

■ Calculation of C_{SPD}

C_{SPD} sets the zero frequency to meet the unity-gain frequency.

$R_{TOP} = R_{BOT} \times (V_{OUT} / V_{REF} -1)$

$C_{SPD} = 1 / (2 \times \pi \times f_{UNITY} \times R_{TOP})$ ······························ Equation 20

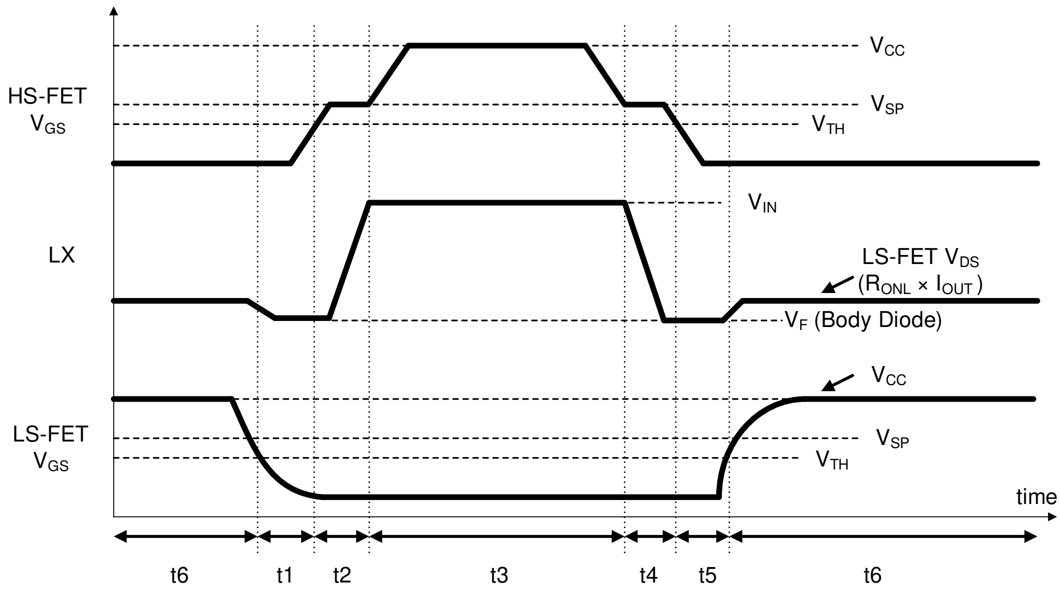
When $R_{BOT} = 22\ k\Omega$,

$R_{TOP} = 22\ k \times (3.3\ V / 0.8\ V -1)$
$= 68.8\ k\Omega$

$C_{SPD} = 1 / (2 \times \pi \times 12.5\ kHz \times 68.8\ k\Omega)$
$= 185.1\ pF \fallingdotseq 220\ pF$

MOSFET Losses

The MOSFET total loss is calculated by the sum of the switching losses when the high-side and the low-side MOSFETs turning-on / off and the conduction losses by the MOSFET's on-resistance. If the total loss become larger than expected, the external MOSFET must be selected with consideration of the on-resistance, the switching losses and the package's power dissipation. The following figure shows the timing chart of the high side / low side MOSFETs at normal switching. The loss at each delay time can be calculated as follows.



DC / DC Converter Basic Switching Timing Chart

t1 (t5):

For the duration between the low-side MOSFET's turn-off and the high-side MOSFET's turn-on, the loss occurs to supply a current from the body diode on the low-side MOSFET. Likewise, for the duration between the high-side MOSFET's turn-off and the low-side MOSFET's turn-on, the loss occurs. The losses (P_{DEAD}) for t1 and t5 can be calculated by the following equation.

$$P_{DEAD} = V_F \times I_{OUT} \times f_{OSC} \times (t_{DEAD1} + t_{DEAD5})$$

V_F: The forward voltage of a body-diode

t_{DEAD1}: The delay time from the instant when the gate-source voltage (V_{GS}) falls below the threshold voltage (V_{TH}) on the low-side MOSFET to the instant when V_{GS} exceeds V_{TH} on the high-side MOSFET.

T_{DEAD5}: The delay time from the instant when V_{GS} falls below V_{TH} on the high-side MOSFET to the instant when V_{GS} exceeds V_{TH} on the low-side MOSFET.

t2 (t4):

Since the drain-source voltage (V_{DS}) is equal to V_{IN} when the high-side MOSFET turns on/off after delay time ($t_{DEAD}1$ / t_{DEAD5}), the source current and the output current (I_{OUT}) become equal. Therefore, a large loss occurs. The losses (P_{SW}) at turn-on / off can be calculated by the following equation.

$$P_{SW} = 1/2 \times V_{IN} \times I_{OUT} \times f_{OSC} \times (t_{RISE} + t_{FALL})$$

t_{RISE}: A duration between the gate voltage rising start time from the threshold voltage and the end of stabilized voltage (V_{SP}) on the high-side MOSFET.

T_{FALL}: A duration between the start time of the gate voltage stabilizing and the falling time below the threshold voltage on the high-side MOSFET.

For the stabilized duration, V_{GS} of the high-side MOSFET remains constant roughly since the gate charge current is used to charge C_{GD}. And, the reverse recovery loss (P_{RR}) occurs to recover the body diode of the low-side MOSFET when the high-side MOSFET turns on. Refer to *the MOSFET datasheet* for information about the electric charge (Qrr) required for recovery.

$$P_{RR} = V_{IN} \times Qrr \times f_{OSC}$$

The power (P_{GH}, P_{GL}) for electric charge of the MOSFET' gate and the power (P_{OSSH}, P_{OSSL}) for electric charge of the MOSFET's output capacity occur. Each power can be calculated by following equations. Refer to *the MOSFET datasheet* for detailed values.

$P_{GH} = Q_{GH} \times V_{CC} \times f_{OSC}$
$P_{GL} = Q_{GL} \times V_{CC} \times f_{OSC}$
$P_{OSSH} = 1/2 \times C_{OSSH} \times (V_{IN})^2 \times f_{OSC}$
$P_{OSSL} = 1/2 \times C_{OSSL} \times (V_{IN})^2 \times f_{OSC}$

V_{CC}: VCC pin voltage
Q_{GH}, Q_{GL}: Gate electric charge quantity for High- /Low- side MOSFETs
C_{OSSH}, C_{OSSL}: Drain-gate capacity + Drain-source capacity for High- /Low- side MOSFETs

t3 (t6):

For the duration of t3, the conduction loss of the high-side MOSFET (P_{HS}(on)) occurs. For the duration of t6, the conduction loss of the low-side MOSFET (P_{LS}(on)) occurs. Each loss can be calculated by the following equation. ON duty is closely analogous to V_{OUT} / V_{IN}.

$I_{RMS} = \sqrt{}\ (((I_{OUT})^2 + (I_{P-P})^2 / 12))$
$P_{HS}\ (on) = (I_{RMS})^2 \times R_{ONH} \times V_{OUT} / V_{IN}$
$P_{LS}\ (on) = (I_{RMS})^2 \times R_{ONL} \times (1 - V_{OUT} / V_{IN})$

I_{RMS}: MOSFET's rms current
I_{P-P}: MOSFET's peak current amplitude
R_{ONH}, R_{ONL}: On-resistance for High- /Low- side MOSFETs

Since the conduction loss depends on the duty, the loss varies with step-down ratio. When the step-down ratio is large and the ON duty is small, the loss of the low side MOSFET becomes larger, and when the ratio is small, the loss of the high-side MOSFET becomes larger. From above equations, each loss of the high-side and the low-side MOSFETs can be calculated by the following equations.

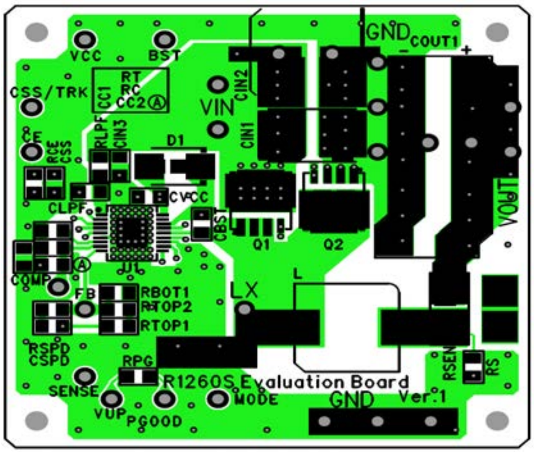
$P_{HS} = P_{HS}\ (on) + P_{SW} + P_{RR} + P_{GH} + P_{OSSH}$
$P_{LS} = P_{LS}\ (on) + P_{GL} + P_{OSSL} + P_{DEAD}$

As is evident from these equations, the switching loss becomes predominant when the input voltage and the frequency are high, and the conduction loss conversely becomes predominant when they are low.

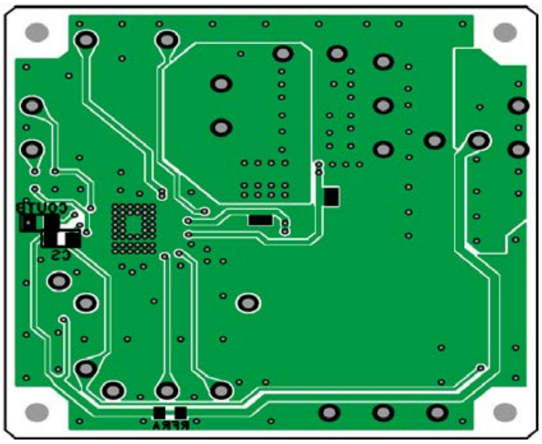
PCB Layout

R1260S (Package：HSOP-18) PCB Layout

Top Layer



Bottom Layer

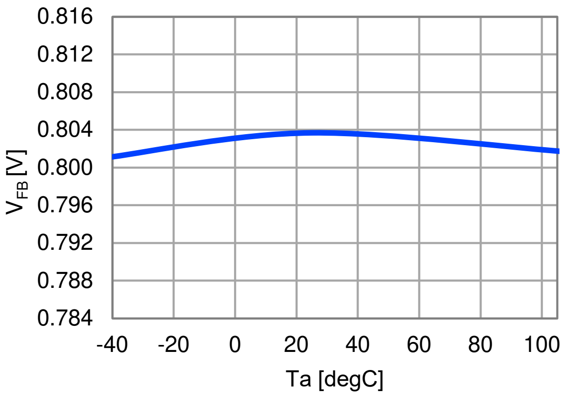


TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) FB Voltage

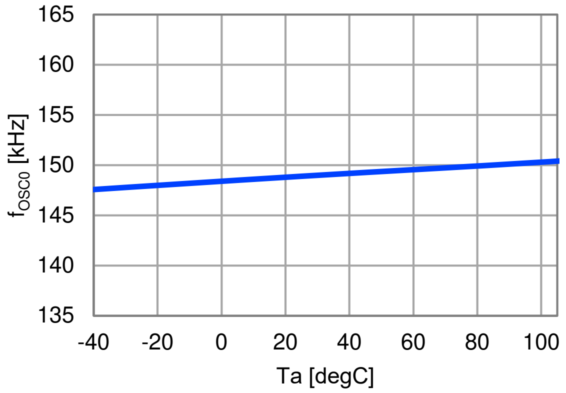
V_{IN} = 48 V , MODE = "High"



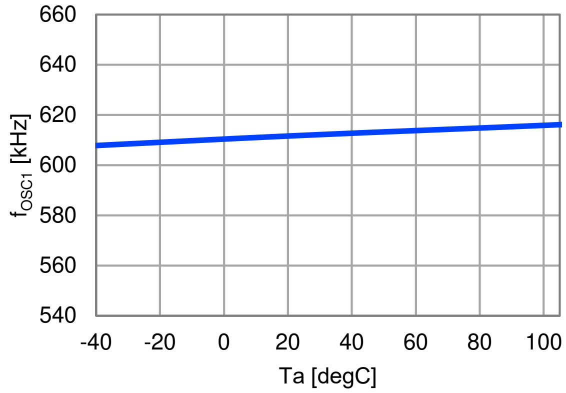
2) Oscillation Frequency

V_{IN} = 48 V , MODE = "High"

150 kHz (RT = 200 kΩ)

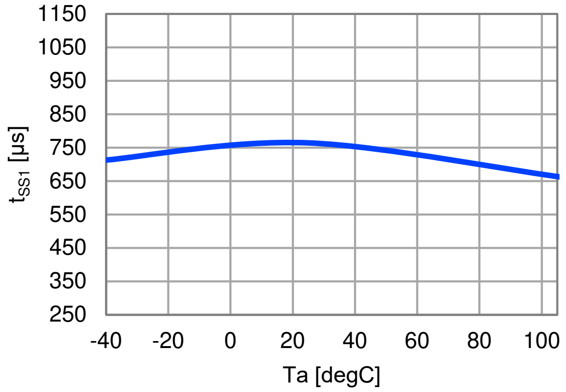


600 kHz (RT = 47 kΩ)

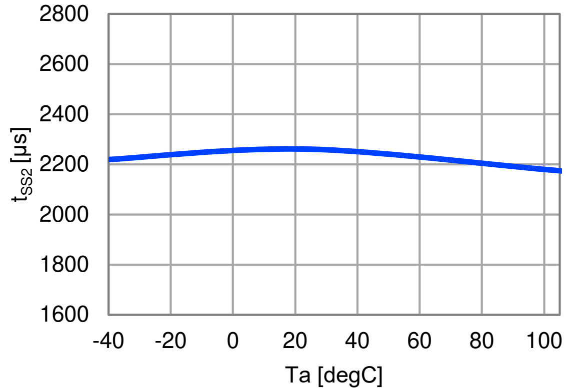


3) Soft-Start Time

V_{IN} = 48 V , Css = open



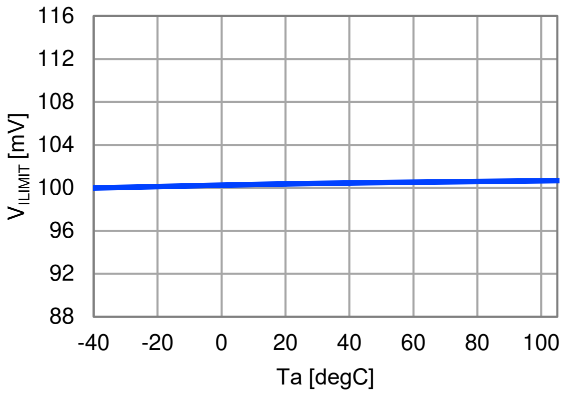
V_{IN} = 48 V , Css = 4.7 nF



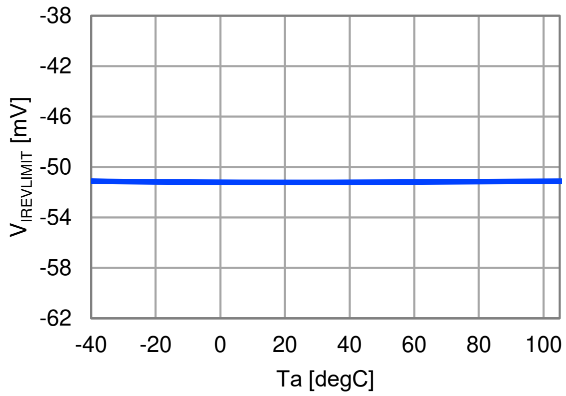
4) Current Limit Threshold Voltage

R1260S023A , V_{IN} = 48 V , MODE = "High"

Current Limit Threshold Voltage



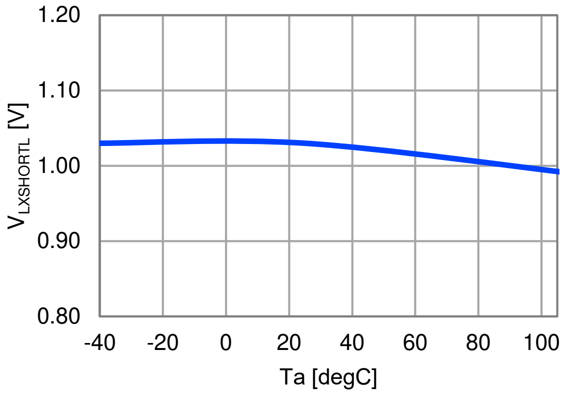
Reverse Current Limit Threshold Voltage



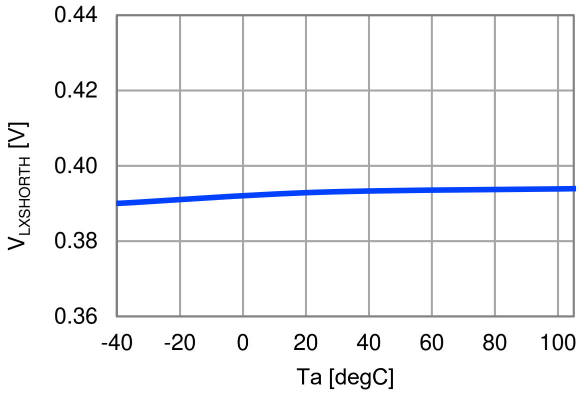
5) LX Ground Short / VIN Short Detection Threshold Voltage

V_{IN} = 48 V , MODE = "High"

LX Ground Short Detection Threshold Voltage



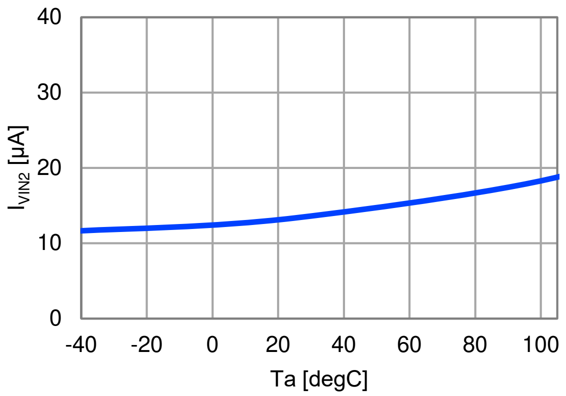
LX VIN Short Detection Threshold Voltage



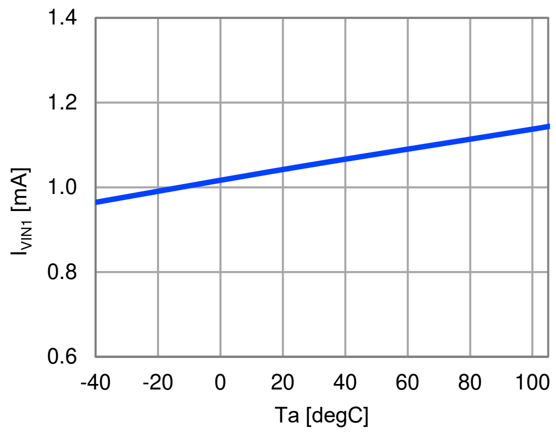
6) Current Consumption

R1260S023A , V_{IN} = 48 V , V_{OUT} = 5 V

MODE = "Low"

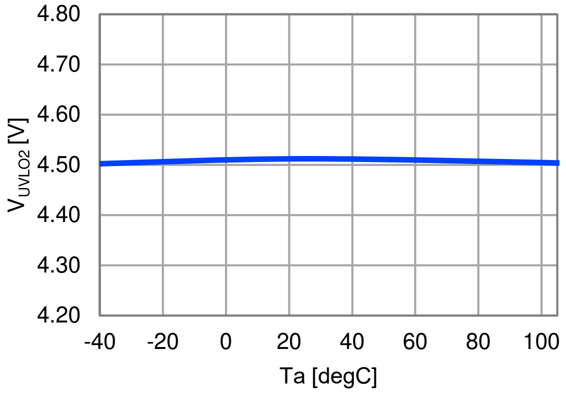


MODE = "High"

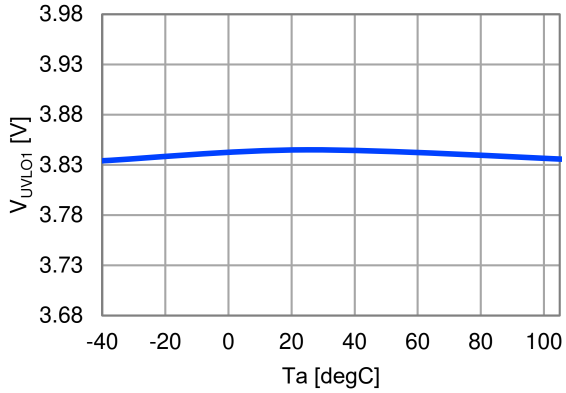


7) UVLO Release / Detection Voltage

UVLO Release Voltage

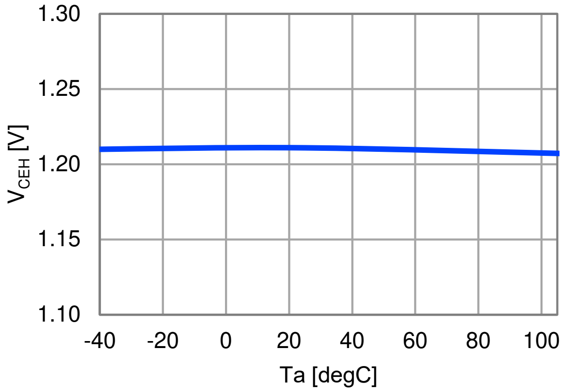


UVLO Detection Voltage

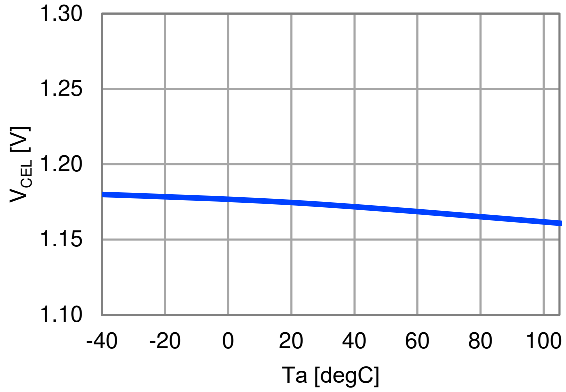


8) CE Input Voltage

V_{IN} = 48 V , CE = "High"



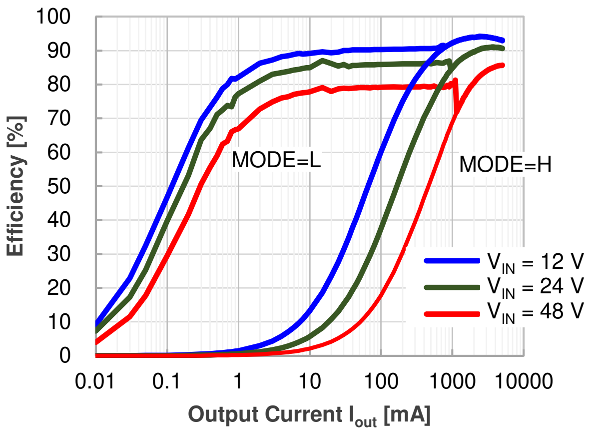
V_{IN} = 48 V , CE = "Low"



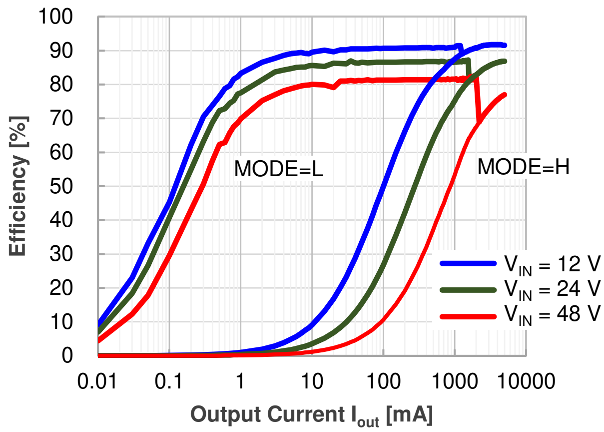
9) Efficiency

R1260S023A , V_{IN} = 12 V / 24V / 48 V , MODE = "High / Low" , V_{OUT} = 3.3 V

fosc = 250 kHz

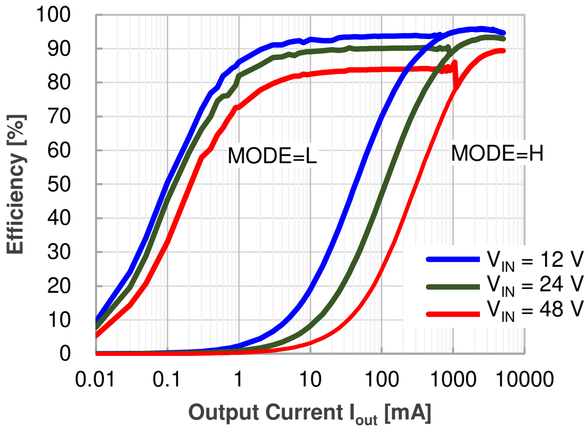


fosc = 600 kHz

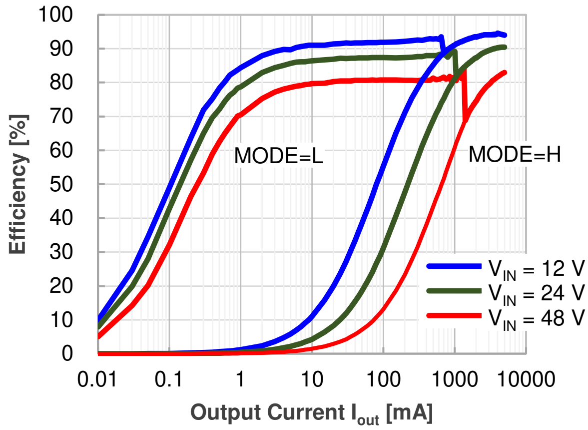


R1260S023A , V_{IN} = 12 V / 24V / 48 V , MODE = "High / Low" , V_{OUT} = 5.0 V

fosc = 250 kHz

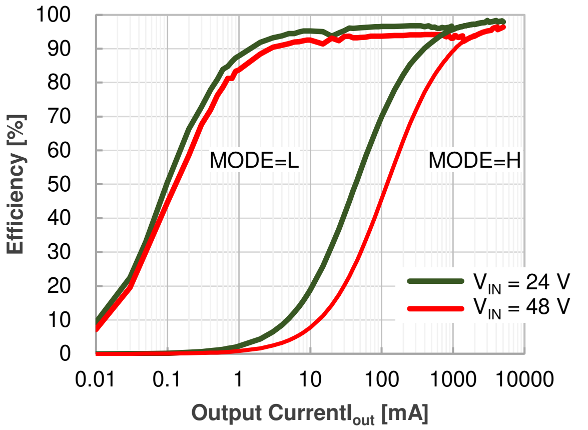


fosc = 600 kHz

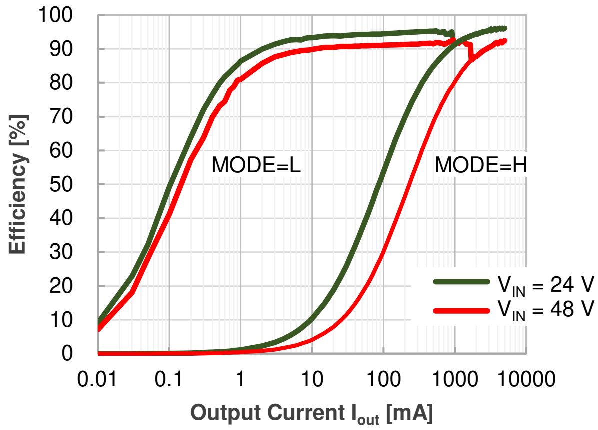


R1260S032A , V_{IN} = 24 V / 48 V , MODE = "High / Low" , V_{OUT} = 12 V

fosc = 250 kHz



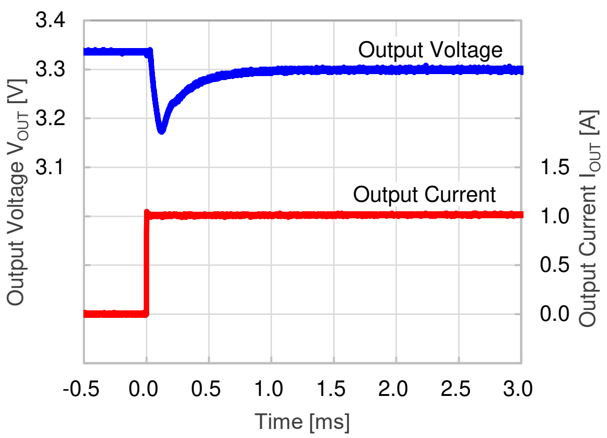
fosc = 600 kHz

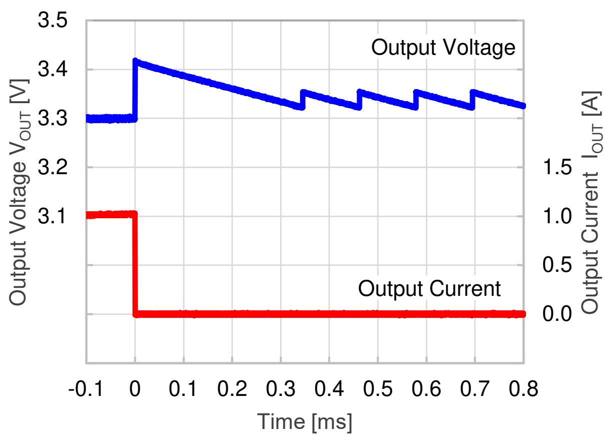


10) Load Transient Response

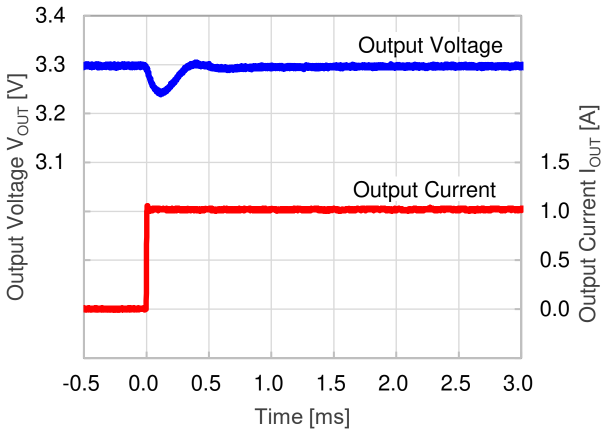
R1260S023A , V_{IN} = 48 V, I_{OUT} = 0 A ⇔ 1 A , fosc = 250 kHz

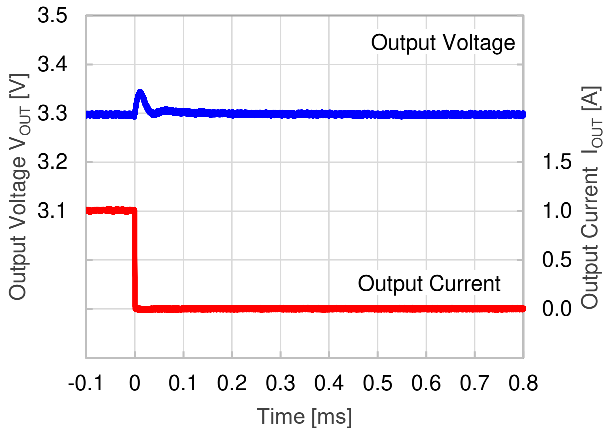
V_{OUT} = 3.3 V , MODE = "Low"



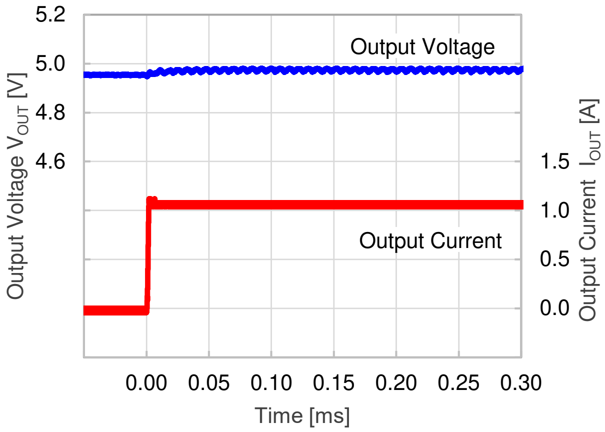


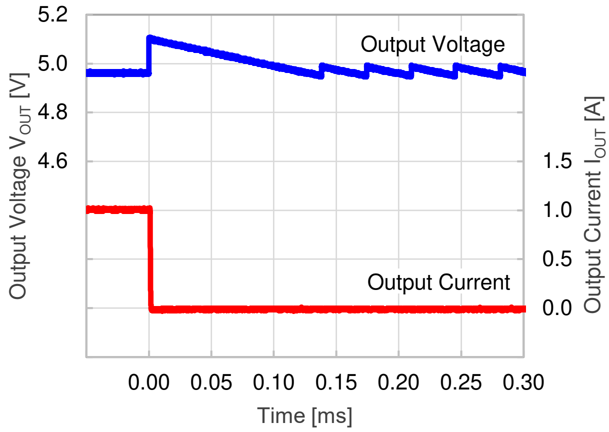
R1260S023A , V_{IN} = 48 V, I_{OUT} = 0 A ⇔ 1 A , fosc = 250 kHz
V_{OUT} = 3.3 V , MODE = "High"



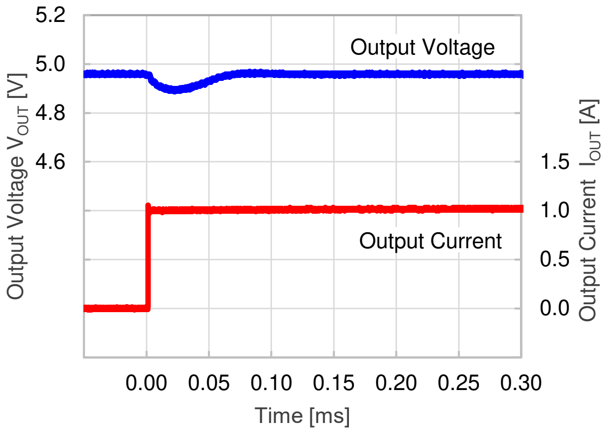


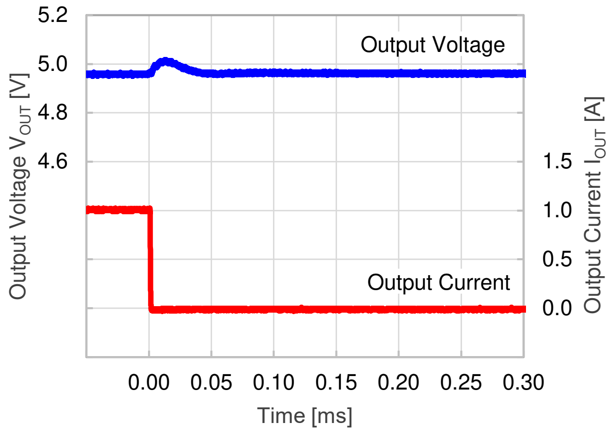
R1260S023A , V_{IN} = 48 V, I_{OUT} = 0 A ⇔ 1 A , fosc = 250 kHz
V_{OUT} = 5.0 V , MODE = "Low"





R1260S023A , V_{IN} = 48 V, I_{OUT} = 0 A ⇔ 1 A , fosc = 250 kHz
V_{OUT} = 5.0 V , MODE = "High"

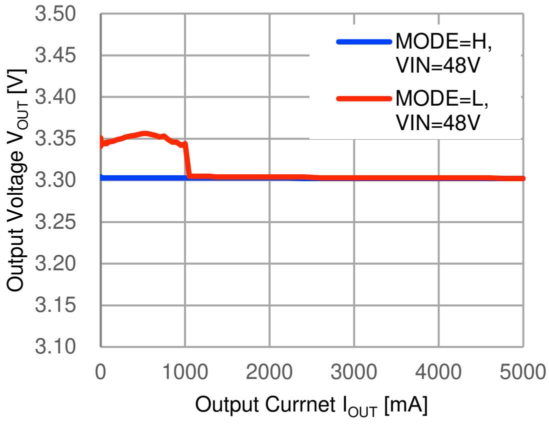




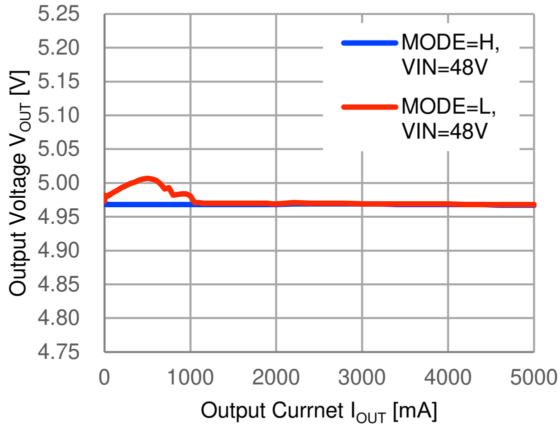
11) Output Voltage vs Output Current

R1260S023A , V_{IN} = 48 V , MODE = "High / Low"

V_{OUT} = 3.3 V , fosc = 250 kHz



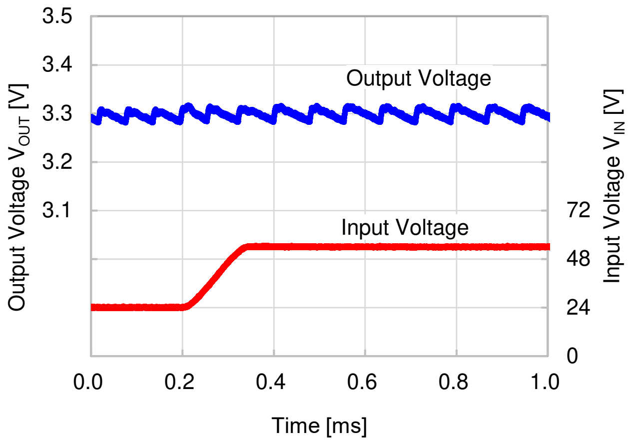
V_{OUT} = 5.0 V , fosc = 500 kHz

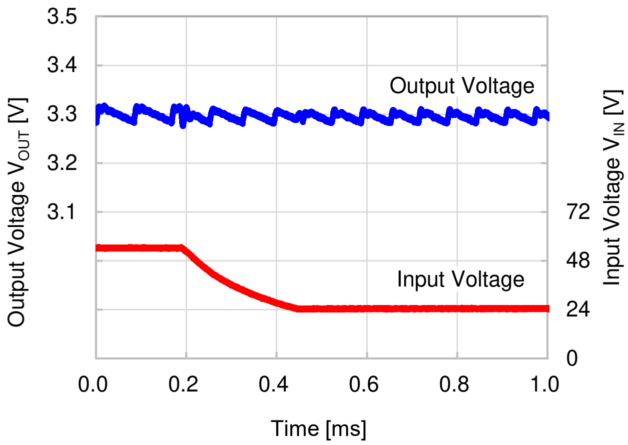


12) Input Transient Response

R1260S023A , V_{IN} = 24 V ⇔ 54 V , V_{OUT} = 3.3 V , fosc = 250 kHz

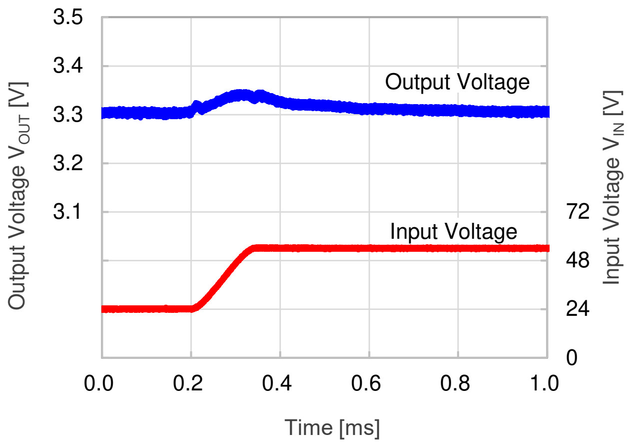
I_{OUT} = 0.1 A , MODE = "Low"

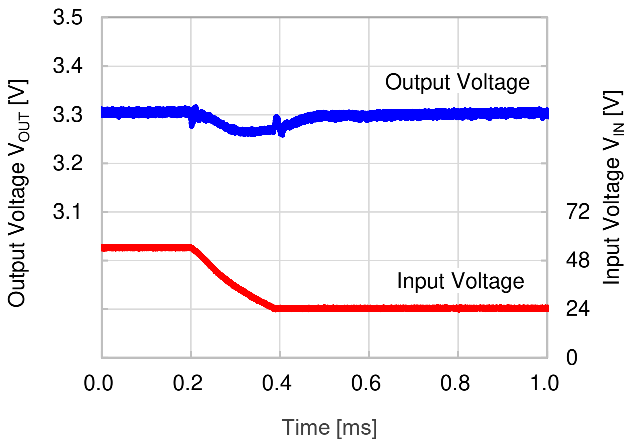




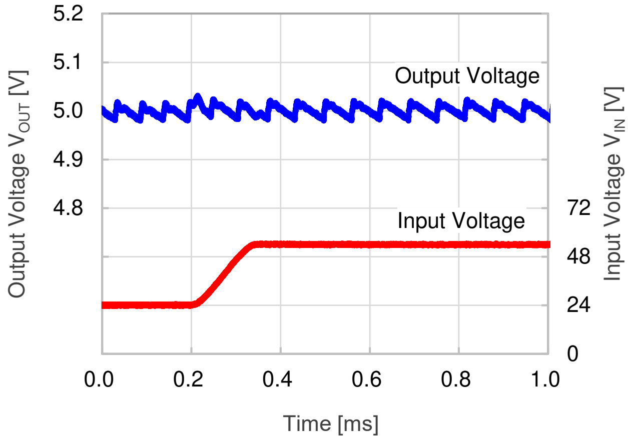
R1260S023A , V_{IN} = 24 V ⇔ 54 V , V_{OUT} = 3.3 V , fosc = 250 kHz

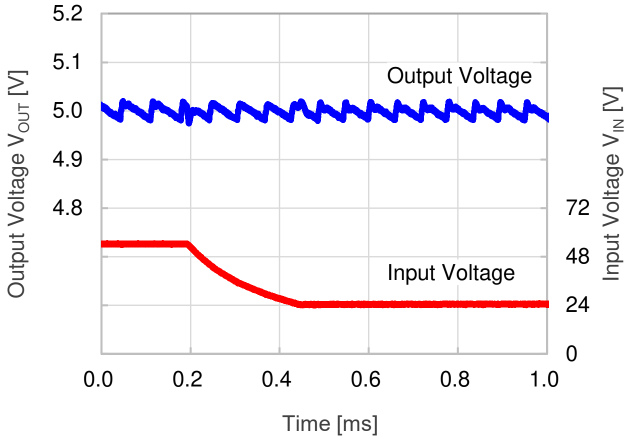
I_{OUT} = 5 A , MODE = "High"



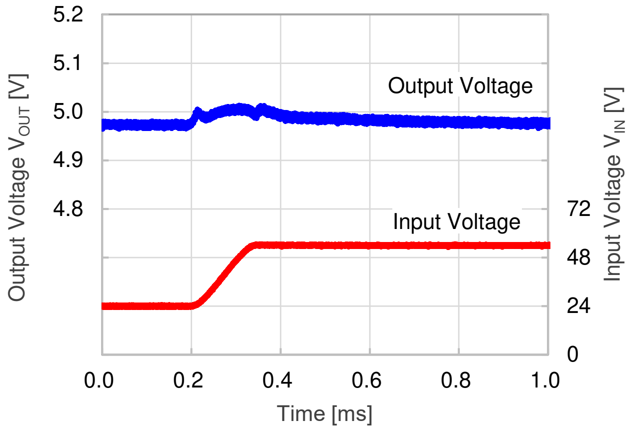


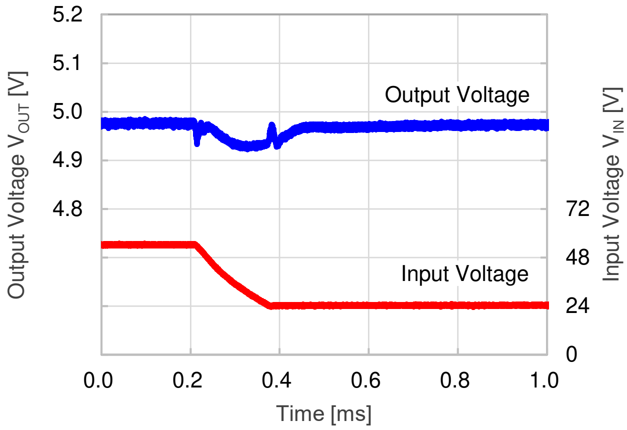
R1260S023A , V_{IN} = 24 V ⇔ 54 V , V_{OUT} = 5.0 V , fosc = 250 kHz
I_{OUT} = 0.1 A , MODE = "Low"





R1260S023A , V_{IN} = 24 V ⇔ 54 V , V_{OUT} = 5.0 V , fosc = 250 kHz
I_{OUT} = 5 A , MODE = "High"

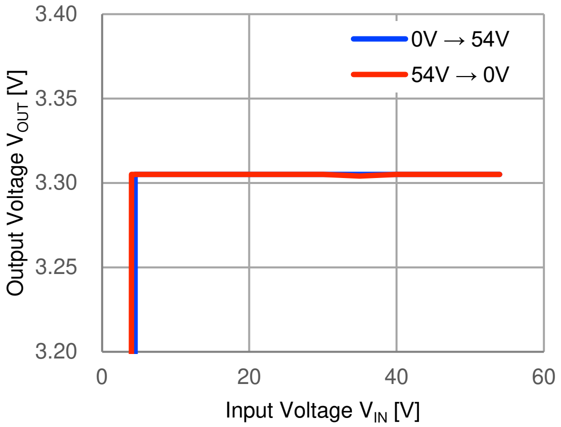




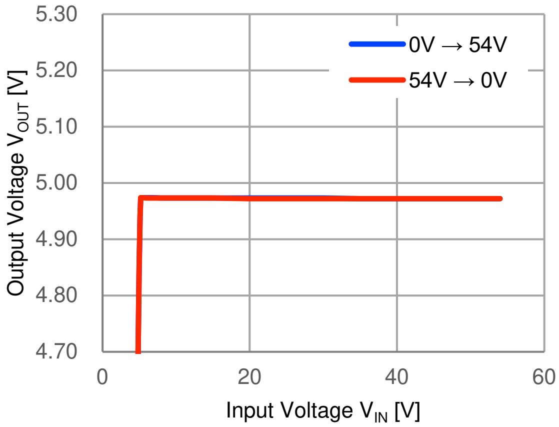
13）Line Regulation

R1260S023A , MODE = "High" , fosc = 250 kHz , I_{OUT} = 0 A

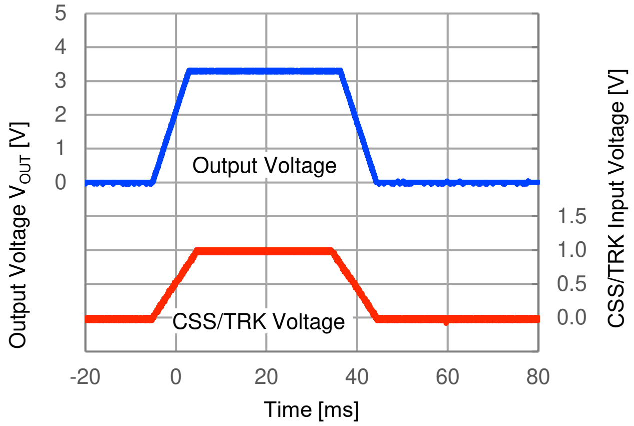
V_{OUT} = 3.3 V



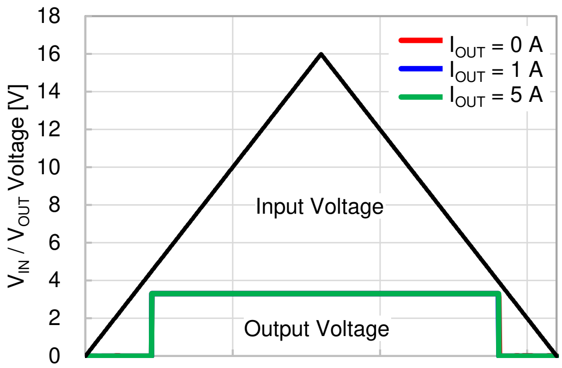
V_{OUT} = 5.0 V



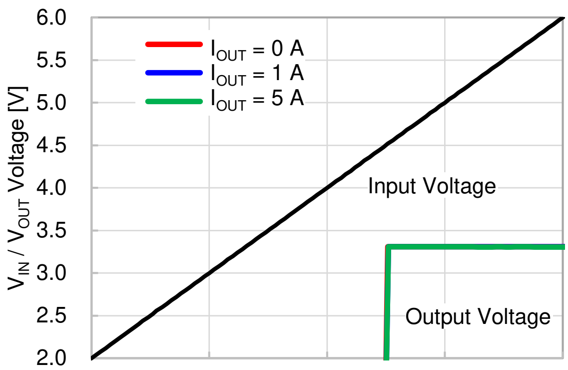
14) Up-Down Tracking
R1260S023A , V_{IN} = 48 V , V_{OUT} = 3.3 V , I_{OUT} = 0 A
fosc = 250 kHz , MODE = "High"



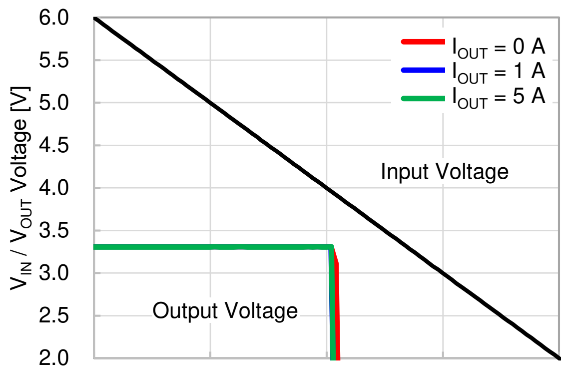
15) Dropout Voltage
R1260S023A , V_{IN} = 0 ⇔ 16 V , V_{OUT} = 3.3 V , MODE = "High" , I_{OUT} = 0 / 1 / 5 A
fosc = 250 kHz



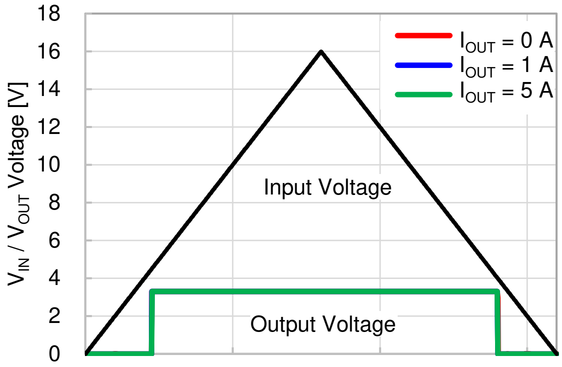
UVLO Release Voltage Zoom-in View



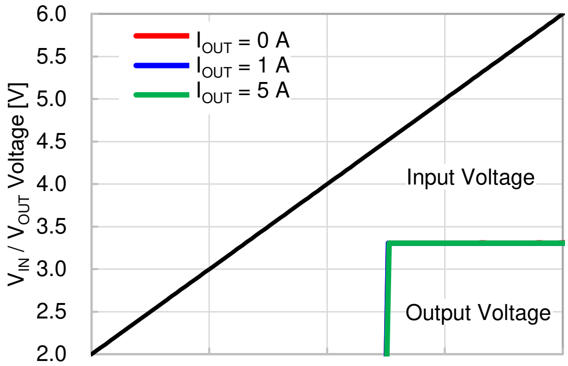
UVLO Detection Voltage Zoom-in View



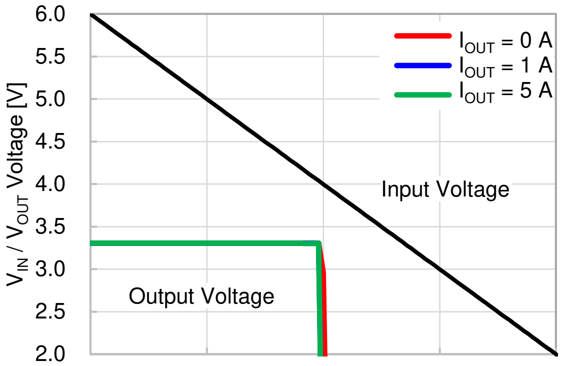
R1260S023A , V_{IN} = 0 ⇔ 16 V , V_{OUT} = 3.3 V , MODE = "High" , I_{OUT} = 0 / 1 / 5 A
fosc =600 kHz



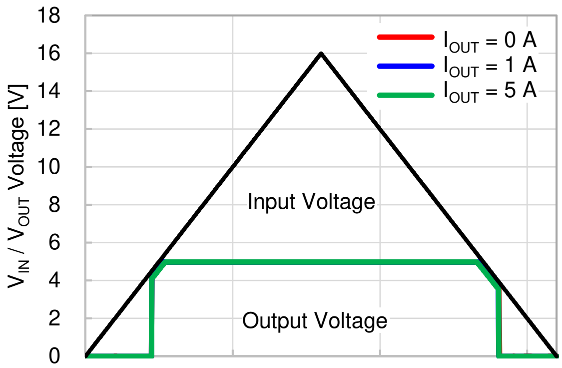
UVLO Release Voltage Zoom-in View



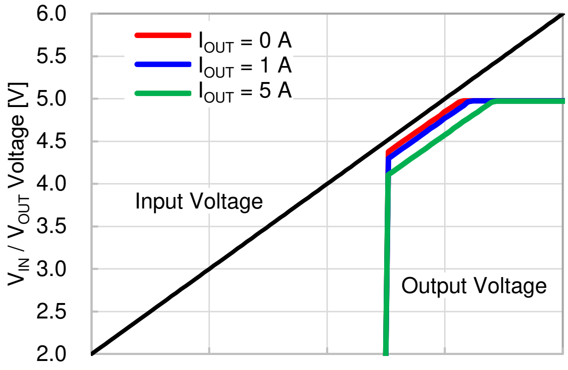
UVLO Detection Voltage Zoom-in View



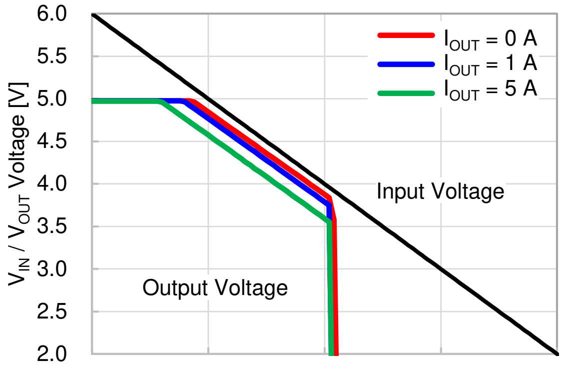
R1260S023A , V_{IN} = 0 ⇔ 16 V , V_{OUT} = 5.0 V , MODE = "High" , I_{OUT} = 0 / 1 / 5 A
fosc = 250 kHz



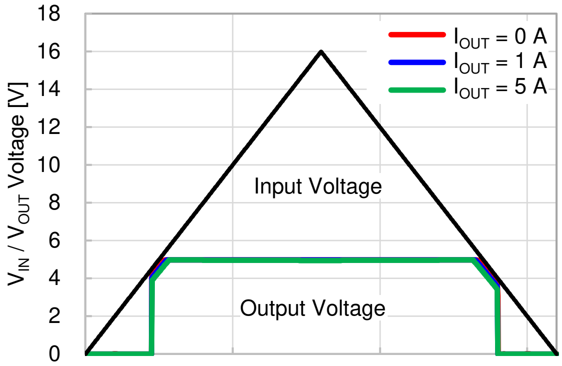
UVLO Release Voltage Zoom-in View



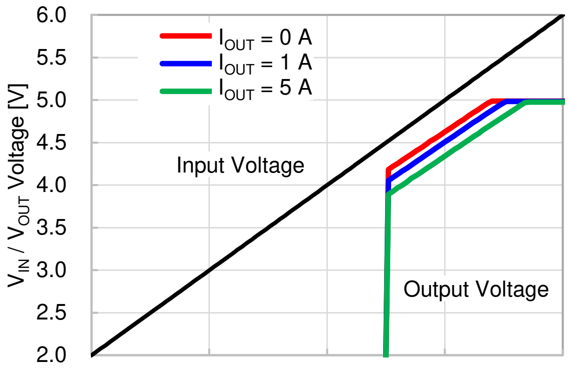
UVLO Detection Voltage Zoom-in View



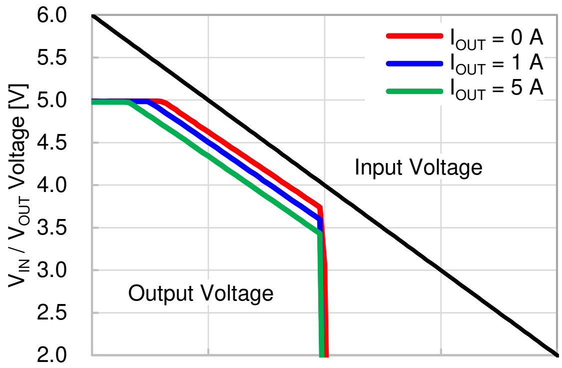
R1260S023A , V_{IN} = 0 ⇔ 16 V , V_{OUT} = 5.0 V , MODE = "High" , I_{OUT} = 0 / 1 / 5 A
fosc =600 kHz



UVLO Release Voltage Zoom-in View



UVLO Detection Voltage Zoom-in View



PD-HSOP-18-(105125)-JE-C

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

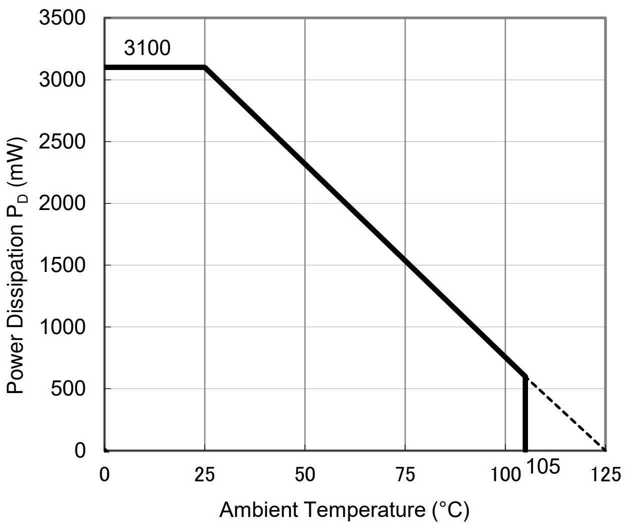
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

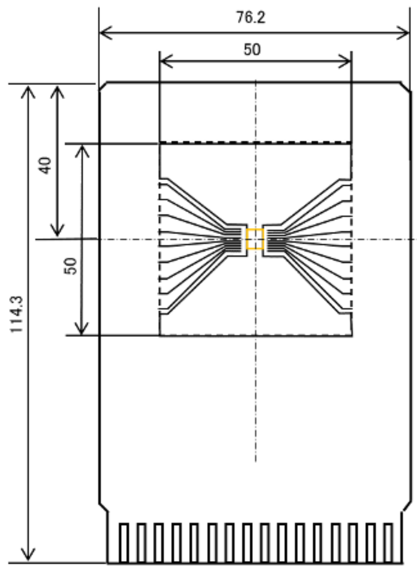
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

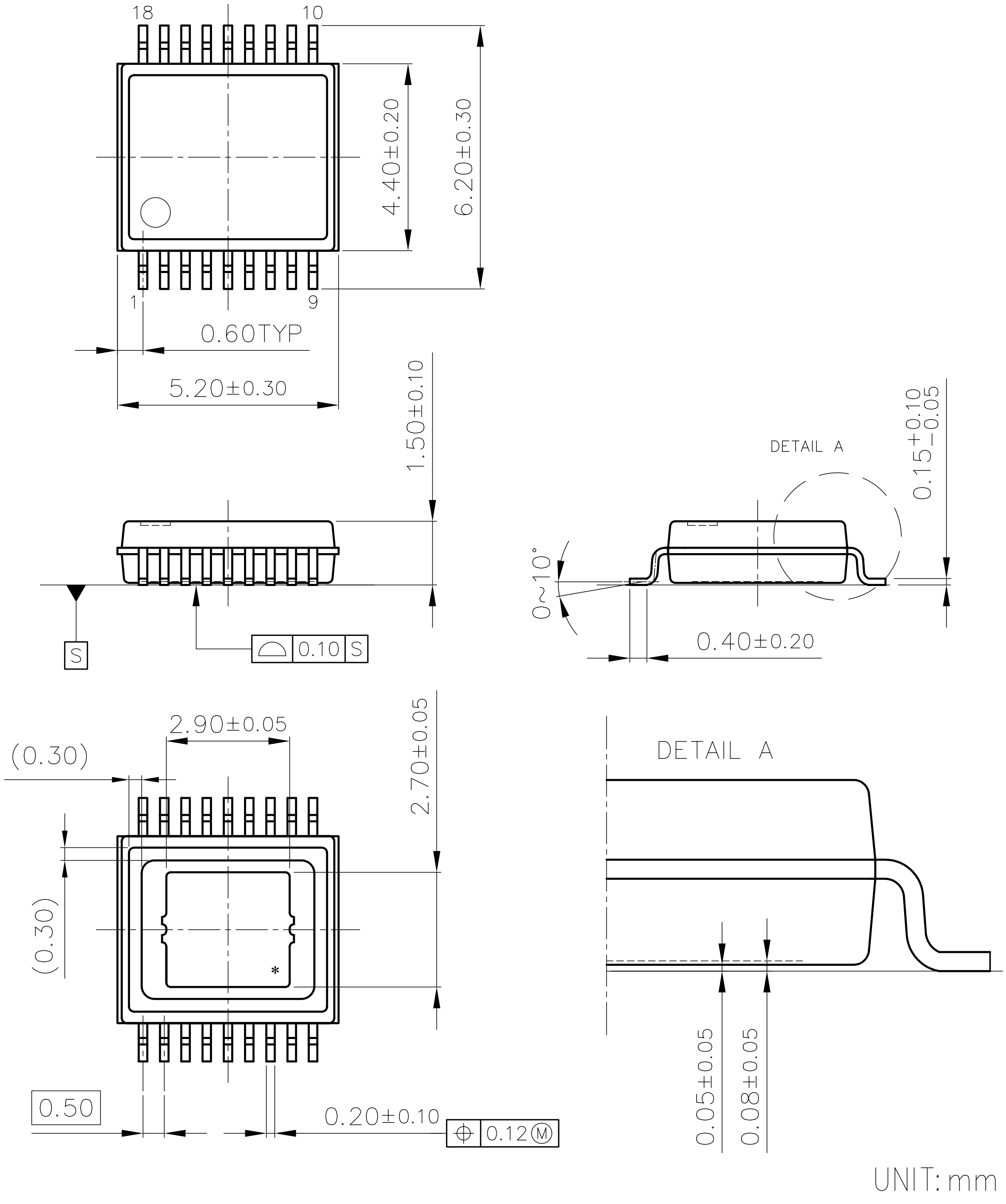


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

DM-HSOP-18-JE-B

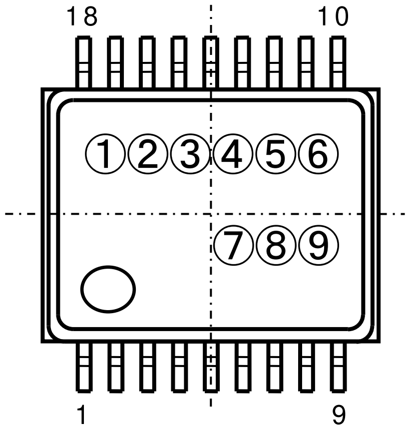


HSOP-18 Package Dimensions

MK-R1260S-JE-A

①②③④⑤⑥: Product Code ··· **Refer to the following table**

⑦⑧⑨: Lot Number ··· Alphanumeric Serial Number



HSOP-18 Marking Specification

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or our distributor before attempting to use AOI.

R1260S Marking List

Product Name	① ② ③ ④ ⑤ ⑥	Product Name	① ② ③ ④ ⑤ ⑥
R1260S011A	R S 1 4 0 A	R1260S011D	R S 1 4 0 V
R1260S012A	R S 1 4 0 B	R1260S012D	R S 1 4 0 W
R1260S013A	R S 1 4 0 C	R1260S013D	R S 1 4 0 X
R1260S021A	R S 1 4 0 D	R1260S021D	R S 1 4 0 Y
R1260S022A	R S 1 4 0 E	R1260S022D	R S 1 4 0 Z
R1260S023A	R S 1 4 0 F	R1260S023D	R S 1 4 1 A
R1260S011B	R S 1 4 0 G	R1260S031A	R S 1 4 2 A
R1260S012B	R S 1 4 0 H	R1260S032A	R S 1 4 2 B
R1260S013B	R S 1 4 0 J	R1260S033A	R S 1 4 2 C
R1260S021B	R S 1 4 0 K	R1260S031B	R S 1 4 2 D
R1260S022B	R S 1 4 0 L	R1260S032B	R S 1 4 2 E
R1260S023B	R S 1 4 0 M	R1260S033B	R S 1 4 2 F
R1260S011C	R S 1 4 0 N	R1260S031C	R S 1 4 2 G
R1260S012C	R S 1 4 0 P	R1260S032C	R S 1 4 2 H
R1260S013C	R S 1 4 0 R	R1260S033C	R S 1 4 2 J
R1260S021C	R S 1 4 0 S	R1260S031D	R S 1 4 2 K
R1260S022C	R S 1 4 0 T	R1260S032D	R S 1 4 2 L
R1260S023C	R S 1 4 0 U	R1260S033D	R S 1 4 2 M

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