Product Specifications		
PART NO.:	VL47D5263A-K0SD-S1	REV: 1.0

General Information

4GB 512Mx64 DDR3 SDRAM LOW VOLTAGE NON-ECC UNBUFFERED SODIMM 204-PIN

Description

The VL47D5263A is a 512Mx64 DDR3 SDRAM high density SODIMM. This dual rank memory module consists of sixteen CMOS 256Mx8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM with thermal sensor in an 8-pin MLF package. This module is a 204-pin small-outline dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

Features

- 204-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rate: PC3-12800
- VDD = VDDQ = 1.35V (1.28V~1.45V) & 1.5V (1.425V~1.575V)
- JEDEC standard 1.35V (1.28V~1.45V) & 1.5V (1.425V~1.575V)
- VDDSPD = 3.0V to 3.6V
- Eight internal component banks for concurrent operation
- 8-bit pre-fetch architecture
- Bi-directional differential data-strobe
- Nominal and dynamic on-die termination (ODT)
- ZQ calibration support
- Programmable CAS# latency: 11 (DDR3-1600)
- Programmable burst; length (8)
- Average refresh period 7.8 us
- Asynchronous reset
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) EEPROM with thermal sensor
- Thermal sensor range: -40°C to +125°C (Max +/-3°C accuracy)
- Lead-free, RoHS compliant
- Gold edge contacts
- PCB: Height 30.00mm (1.181”), double sided component
- Operating temperature (TOPER): -40°C to +95°C (module screening using commercial DRAM)

Notes: Double refresh rate is required when 85°C < TOPER <= 95°C.
TOPER is DRAM case temperature (Tc).

Pin Description

Pin Name	Function
A0~A14	Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Strobes
DQS0#~DQS7#	Data Strobes Complement
DM0~DM7	Data Masks
CK0,CK0#, CK1,CK1#	Clock Input
ODT0, ODT1	On-die Termination Control
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
EVENT#	Temperature Event Output
VREFCA	Reference Voltage for CA
VREFDQ	Reference Voltage for DQ
VDDSPD	SPD Voltage Supply
VTT	Termination Voltage
RESET#	Register and SDRAM Control
NC	No Connect

Order Information:

VL47D5263A - K0 S D - S1

- S1: OPERATING TEMPERATURE
  - S1: Industrial screening
- D: DRAM DIE
  - D-DIE
- S: DRAM MANUFACTURER
  - S - SAMSUNG
- K0: MODULE SPEED
  - K0: PC3-12800 @ CL11
- VL: Lead-free/RoHS

DRAM component: Samsung K4B2G0846D-HYK0

Virtium

Product Specifications		
PART NO.:	VL47D5263A-K0SD-S1	REV: 1.0

Pin Configuration

204-PIN DDR3 SODIMM FRONT

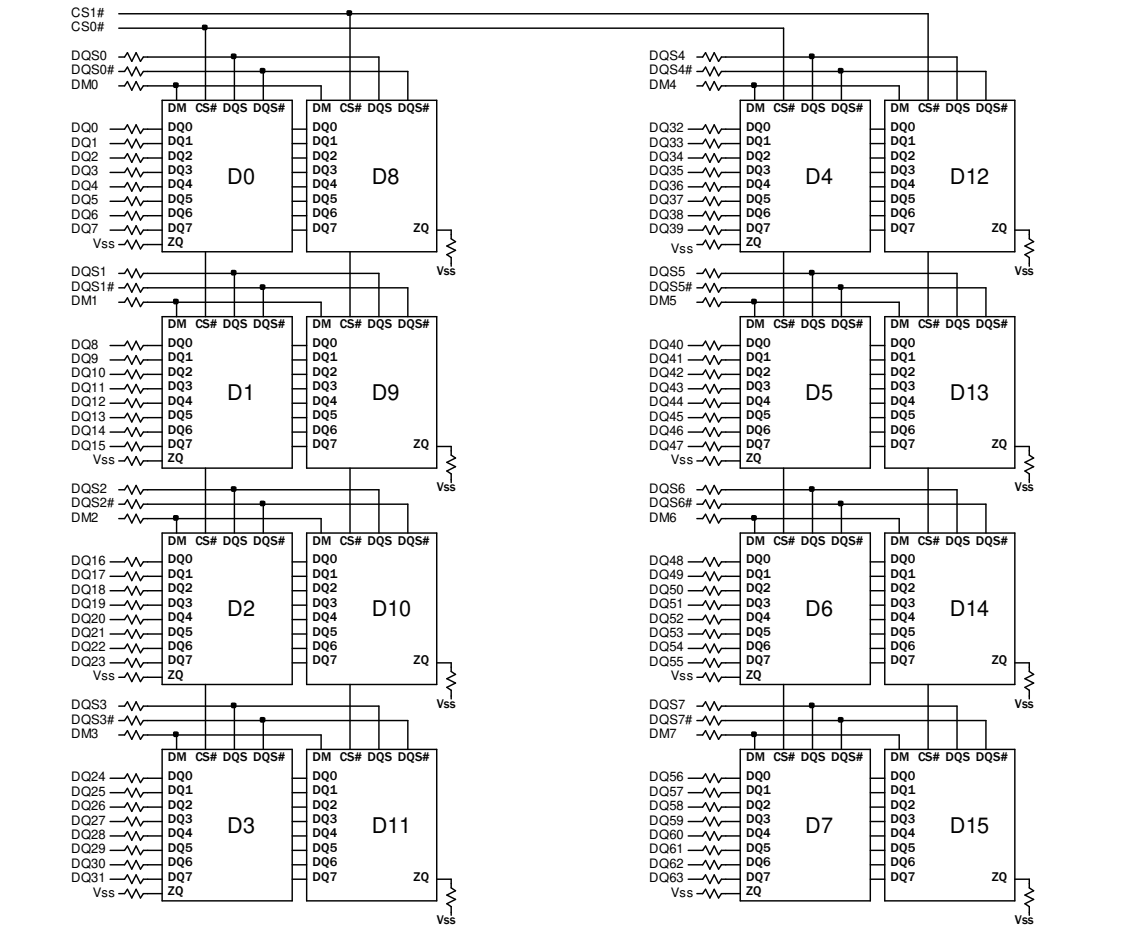
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	53	DQ19	105	VDD	157	DQ42
3	VSS	55	VSS	107	A10	159	DQ43
5	DQ0	57	DQ24	109	BA0	161	VSS
7	DQ1	59	DQ25	111	VDD	163	DQ48
9	VSS	61	VSS	113	WE#	165	DQ49
11	DM0	63	DM3	115	CAS#	167	VSS
13	VSS	65	VSS	117	VDD	169	DQS6#
15	DQ2	67	DQ26	119	A13	171	DQS6
17	DQ3	69	DQ27	121	CS1#	173	VSS
19	VSS	71	VSS	123	VDD	175	DQ50
21	DQ8	73	CKE0	125	NC	177	DQ51
23	DQ9	75	VDD	127	VSS	179	VSS
25	VSS	77	NC	129	DQ32	181	DQ56
27	DQS1#	79	BA2	131	DQ33	183	DQ57
29	DQS1	81	VDD	133	VSS	185	VSS
31	VSS	83	A12	135	DQS4#	187	DM7
33	DQ10	85	A9	137	DQS4	189	VSS
35	DQ11	87	VDD	139	VSS	191	DQ58
37	VSS	89	A8	141	DQ34	193	DQ59
39	DQ16	91	A5	143	DQ35	195	VSS
41	DQ17	93	VDD	145	VSS	197	SA0
43	VSS	95	A3	147	DQ40	199	VDDSPD
45	DQS2#	97	A1	149	DQ41	201	SA1
47	DQS2	99	VDD	151	VSS	203	VTT
49	VSS	101	CK0	153	DM5		
51	DQ18	103	CK0#	155	VSS		

204-PIN DDR3 SODIMM BACK

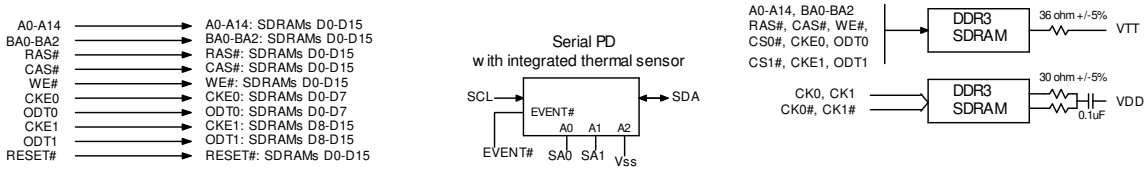
Pin	Name	Pin	Name	Pin	Name	Pin	Name
2	VSS	54	VSS	106	VDD	158	DQ46
4	DQ4	56	DQ28	108	BA1	160	DQ47
6	DQ5	58	DQ29	110	RAS#	162	VSS
8	VSS	60	VSS	112	VDD	164	DQ52
10	DQS0#	62	DQS3#	114	CS0#	166	DQ53
12	DQS0	64	DQS3	116	ODT0	168	VSS
14	VSS	66	VSS	118	VDD	170	DM6
16	DQ6	68	DQ30	120	ODT1	172	VSS
18	DQ7	70	DQ31	122	NC	174	DQ54
20	VSS	72	VSS	124	VDD	176	DQ55
22	DQ12	74	CKE1	126	VREFCA	178	VSS
24	DQ13	76	VDD	128	VSS	180	DQ60
26	VSS	78	A15 *	130	DQ36	182	DQ61
28	DM1	80	A14	132	DQ37	184	VSS
30	RESET#	82	VDD	134	VSS	186	DQS7#
32	VSS	84	A11	136	DM4	188	DQS7
34	DQ14	86	A7	138	VSS	190	VSS
36	DQ15	88	VDD	140	DQ38	192	DQ62
38	VSS	90	A6	142	DQ39	194	DQ63
40	DQ20	92	A4	144	VSS	196	VSS
42	DQ21	94	VDD	146	DQ44	198	EVENT#
44	VSS	96	A2	148	DQ45	200	SDA
46	DM2	98	A0	150	VSS	202	SCL
48	VSS	100	VDD	152	DQS5#	204	VTT
50	DQ22	102	CK1	154	DQS5		
52	DQ23	104	CK1#	156	VSS		

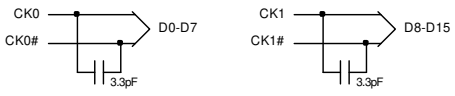
*: These pins are not used in this module.

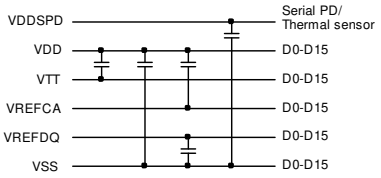
Function Block Diagram



Command, address, control, and clock line terminations







Notes:

1. Unless otherw ise noted, resistor values are 15 ohms +/-5%
2. ZQ resistors are 240 ohms +/-1%

Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
VDD	Voltage on VDD pin relative to VSS		-0.4	1.975	V
VDDQ	Voltage on VDDQ pin relative to VSS		-0.4	1.975	V
VIN, VOUT	Voltage on any pin relative to VSS		-0.4	1.975	V
TSTG	Storage temperature		-55	100	^{0}C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, RAS#, CAS#, WE#, BA	-32	32	uA
		CS#, CKE, ODT, CK, CK#	-16	16	uA
		DM	-4	4	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-10	10	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-16	16	uA

DC Operating Conditions

Symbol	Parameter	Operating Voltage	Min	Typical	Max	Unit	Notes
VDD	Supply Voltage	1.35V	1.283	1.35	1.45	V	1,2
		1.5V	1.425	1.5	1.575		
VDDQ	I/O Supply Voltage	1.35V	1.283	1.35	1.45	V	1,2
		1.5V	1.425	1.5	1.575		
VREFDQ (DC)	I/O reference voltage DQ bus		0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3,4
VREFCA (DC)	Input reference voltage CMD/ADD bus		0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3,4
VTT	Termination Reference Voltage		-0.483 x VDDQ	0.5 x VDDQ	+0.517 x VDDQ	V	5

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/-1% VDD
4. For reference: approximate VDD/2 +/-15mV.
5. VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	-40 to +95	^{0}C	1,2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At -40 to +85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Input DC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
1.35V				
Command and Address				
VIHCA(DC)	Input High (Logic 1)	VREF + 0.090	VDD	V
VILCA(DC)	Input Low (Logic 0)	VSS	VREF - 0.090	V
DQ and DM				
VIHDQ(DC)	Input High (Logic 1)	VREF + 0.090	VDD	V
VILDQ(DC)	Input Low (Logic 0)	VSS	VREF - 0.090	V
1.5V				
Command and Address				
VIHCA(DC)	Input High (Logic 1)	VREF + 0.100	VDD	V
VILCA(DC)	Input Low (Logic 0)	VSS	VREF - 0.100	V
DQ and DM				
VIHDQ(DC)	Input High (Logic 1)	VREF + 0.100	VDD	V
VILDQ(DC)	Input Low (Logic 0)	VSS	VREF – 0.100	V

Input AC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
1.35V				
Command and Address				
VIHCA(AC)	Input High (Logic 1)	VREF + 0.160	-	V
VILCA(AC)	Input Low (Logic 0)	-	VREF - 0.160	V
DQ and DM				
VIHDQ(AC)	Input High (Logic 1)	VREF + 0.135	-	V
VILDQ(AC)	Input Low (Logic 0)	-	VREF - 0.135	V
1.5V				
Command and Address				
VIHCA(AC)	Input High (Logic 1)	VREF + 0.175	-	V
VILCA(AC)	Input Low (Logic 0)	-	VREF - 0.175	V
DQ and DM				
VIHDQ(AC)	Input High (Logic 1)	VREF + 0.150	-	V
VILDQ(AC)	Input Low (Logic 0)	-	VREF - 0.150	V

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	K0 (DDR3-1600)		Unit
		Min	Max	
1.35V				
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	16	24.8	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	10	14.4	pF
Input capacitance (CK0, CK0#), (CK1, CK1#)	CIN3	10.4	15.2	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	CIO	6.4	8.6	pF
1.5V				
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	16	24.8	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	10	14.4	pF
Input capacitance (CK0, CK0#), (CK1, CK1#)	CIN3	10.4	15.2	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	CIO	6.8	8.6	pF

IDD Specification

Condition	Symbol	K0 (DDR3-1600)		Unit
		1.35V	1.5V	
Operating one bank active-precharge current; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	400	456	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); tRCD= tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1*	480	536	mA
Precharge power-down current; All device banks idle; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P-F**	240	240	mA
	IDD2P-S**	160	192	mA
Precharge standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N**	272	320	mA
Precharge quiet standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	272	320	mA
Active power-down current; All device banks open; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P**	272	320	mA
Active standby current; All device banks open; tCK= tCK(IDD); tRP= tRP(IDD); tRAS= tRAS MAX(IDD)); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	480	560	mA
Operating burst read current; All device banks open; Continuous burst reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	600	816	mA
Operating burst write current; All device banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W*	680	856	mA
Burst refresh current; tCK=tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	1840	1920	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6**	160	192	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = tRCD(IDD) - 1*tCK(IDD); tCK= tCK(IDD); tRC= tRC(IDD); tRRD = tRRD(IDD); tRCD = 1*tCK(IDD) ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.	IDD7*	1080	1216	mA

Note: IDD specification is based on Samsung D-die components.
*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
**: Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)		tCK(DLL_OFF)	8	-	8	-	8	-	ns
Average Clock Period		tCK(avg)	1.25	<1.50	1.5	<1.875	1.875	<2.5	ns
Clock Period		tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ns
Average high pulse width		tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width		tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Clock Period Jitter		tJIT(per)	-70	70	-80	80	-90	90	ps
Clock Period Jitter during DLL locking period		tJIT(per, lck)	-60	60	-70	70	-80	80	ps
Cycle to Cycle Period Jitter		tJIT(cc)	140		160		180		ps
Cycle to Cycle Period Jitter during DLL locking period		tJIT(cc, lck)	120		140		160		ps
Cumulative error across 2 cycles		tERR(2per)	-103	103	-118	118	-132	132	ps
Cumulative error across 3 cycles		tERR(3per)	-122	122	-140	140	-157	157	ps
Cumulative error across 4 cycles		tERR(4per)	-136	136	-155	155	-175	175	ps
Cumulative error across 5 cycles		tERR(5per)	-147	147	-168	168	-188	188	ps
Cumulative error across 6 cycles		tERR(6per)	-155	155	-177	177	-200	200	ps
Cumulative error across 7 cycles		tERR(7per)	-163	163	-186	186	-209	209	ps
Cumulative error across 8 cycles		tERR(8per)	-169	169	-193	193	-217	217	ps
Cumulative error across 9 cycles		tERR(9per)	-175	175	-200	200	-224	224	ps
Cumulative error across 10 cycles		tERR(10per)	-180	180	-205	205	-231	231	ps
Cumulative error across 11 cycles		tERR(11per)	-184	184	-210	210	-237	237	ps
Cumulative error across 12 cycles		tERR(12per)	-188	188	-215	215	-242	242	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles		tERR(*n*per)	tERR(*n*per)min =(1+ 0.68ln(*n*))*tJIT(per)min tERR(*n*per)max=(1+ 0.68ln(*n*))*tJIT(per)max						ps
Absolute clock HIGH pulse width		tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)
Absolute clock Low pulse width		tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)
Data Timing									
DQS,DQS# to DQ skew, per group, per access		tDQSQ	-	100	-	125	-	150	ps
DQ output hold time from DQS, DQS#		tQH	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#		tLZ(DQ)	-450	225	-500	250	-600	300	ps
DQ high-impedance time from CK, CK#		tHZ(DQ)	-	225	-	250	-	300	ps
Data setup time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	1.35V	tDS(base) (AC160)	-	-	-	-	40	-	ps
		tDS(base) (AC135)	25	-	45	-	-	-	
Data setup time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	1.5V	tDS(base) (AC175)	-	-	-	-	25	-	ps
		tDS(base) (AC150)	10	-	30	-	-	-	

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
Data hold time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels		tDH(base)	55	-	75	-	110	-	ps
DQ and DM Input pulse width for each input		tDIPW	360	-	400	-	490	-	ps
Data Strobe Timing									
DQS, DQS# READ Preamble		tRPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# differential READ Postamble		tRPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS# output high time		tQSH	0.4	-	0.4	-	0.38	-	tCK(avg)
DQS, DQS# output low time		tQSL	0.4	-	0.4	-	0.38	-	tCK(avg)
DQS, DQS# WRITE Preamble		tWPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# WRITE Postamble		tWPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS# rising edge output access time from rising CK, CK#		tDQSCK	-225	225	-255	255	-300	300	ps
DQS, DQS# low-impedance time (Referenced from RL-1)		tLZ(DQS)	-450	225	-500	250	-600	300	ps
DQS, DQS# high-impedance time (Referenced from RL+BL/ 2)		tHZ(DQS)	-	225	-	250	-	300	ps
DQS, DQS# differential input low pulse width		tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS, DQS# differential input high pulse width		tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS, DQS# rising edge to CK, CK# rising edge		tDQSS	-0.27	0.27	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS,DQS# failing edge setup time to CK, CK# rising edge		tDSS	0.18	-	0.2	-	0.2	-	tCK(avg)
DQS,DQS# failing edge hold time to CK, CK# rising edge		tDSH	0.18	-	0.2	-	0.2	-	tCK(avg)
Command and Address Timing									
DLL locking time		tDLLK	512	-	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay		tRTP	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command		tWTR	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
WRITE recovery time		tWR	15	-	15	-	15	-	ns
Mode Register Set command cycle time		tMRD	4	-	4	-	4	-	nCK
Mode Register Set command update delay		tMOD	max (12tCK,15ns)	-	max (12tCK,15ns)	-	max (12tCK,15ns)	-	
CAS# to CAS# command delay		tCCD	4	-	4	-	4	-	nCK
Auto precharge write recovery + precharge time		tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK
Multi-Purpose Register Recovery Time		tMPRR	1	-	1	-	1	-	nCK
ACTIVE to PRECHARGE command period		tRAS	35	9*tREFI	36	9*tREFI	37.5	9*tREFI	ns
ACTIVE to internal read or write delay time		tRCD	13.75	-	13.5	-	13.13	-	ns
PRECHARGE command period		tRP	13.75	-	13.5	-	13.13	-	ns
ACTIVE to ACTIVE or REF command period		tRC	48.75	-	49.5	-	50.63	-	ns
ACTIVE to ACTIVE command period for 1KB page size		tRRD	max (4tCK, 6ns)	-	max (4tCK, 6ns)	-	max (4tCK, 7.5ns)	-	
ACTIVE to ACTIVE command period for 2KB page size		tRRD	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	
Four activate window for 1KB page size		tFAW	30	-	30	-	37.5	-	ns
Four activate window for 2KB page size		tFAW	40	-	45	-	50	-	ns
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	1.35V	tIS(base) (AC160)	-	-	-	-	140	-	ps
		tIS(base) (AC135)	185	-	205	-	-	-	

AC TIMING PARAMETERS & SPECIFICATIONS

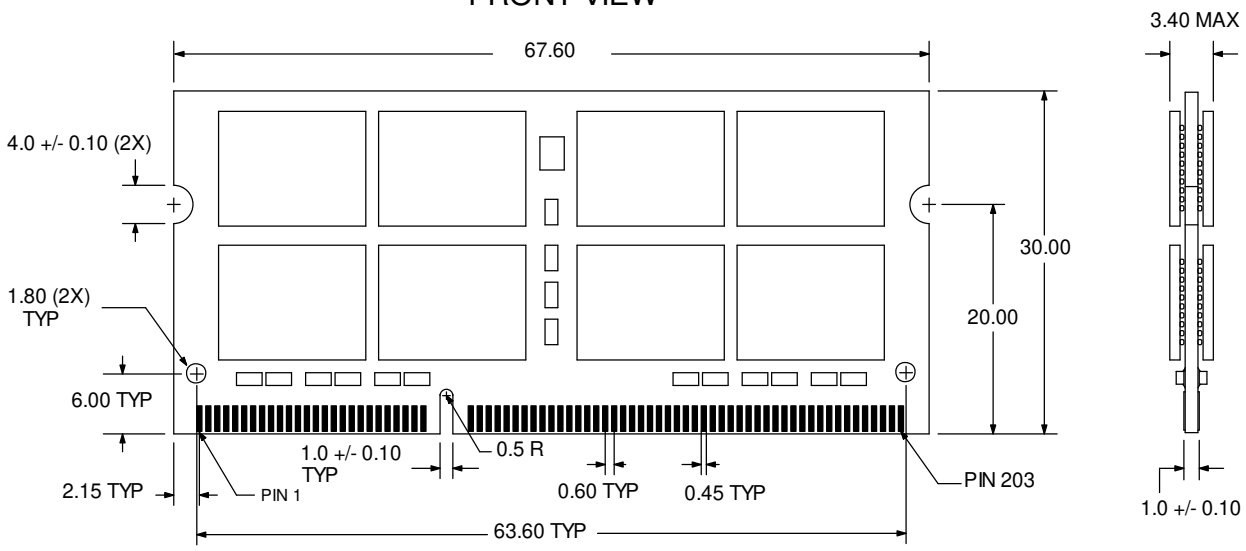
Parameter		Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	1.5V	tIS(base) (AC175)	-	-	-	-	125	-	ps
		tIS(base) (AC150)	170	-	190	-	-	-	
Command and Address hold time from CK, CK# referenced to Vih(ac) / Vil(ac) levels		tIH(base)	130	-	150	-	210	-	ps
Control & Address Input pulse width for each input		tIPW	560	-	620	-	780	-	ps
Refresh Timing									
2Gb REFRESH to REFRESH or REFRESH to ACTIVE command interval		tRFC	160	-	160	-	160	-	ns
Average periodic refresh interval (0°C<= TCASE <= 85 °C)		tREFI	7.8	-	7.8	-	7.8	-	us
Average periodic refresh interval (85°C<= TCASE <= 95 °C)		tREFI	3.9	-	3.9	-	3.9	-	us
Calibration Timing									
Power-up and RESET calibration time		tZQinitI	512	-	512	-	512	-	tCK
Normal operation Full calibration time		tZQoper	256	-	256	-	256	-	tCK
Normal operation Short calibration time		tZQCS	64	-	64	-	64	-	tCK
Reset Timing									
Exit Reset from CKE HIGH to a valid command		tXPR	max (5tCK, tRFC + 10ns)	-	max (5tCK, tRFC + 10ns)	-	max (5tCK, tRFC + 10ns)	-	
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL		tXS	max(5tC, tRFC+10ns)	-	max(5tC, tRFC+10ns)	-	max(5tC, tRFC +10ns)	-	
Exit Self Refresh to commands requiring a locked DLL		tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing		tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)		tCKSRE	max(5tC, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)		tCKSRX	max(5tC, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	
Power Down Timing									
Exit Power Down with DLL to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL		tXP	max (3tCK, 6ns)	-	max (3tCK, 6ns)	-	max (3tCK, 7.5ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL		tXPDLL	max (10tCK,24ns)	-	max (10tCK,24ns)	-	max (10tCK,24ns)	-	
CKE minimum pulse width		tCKE	max (3tCK, 5ns)	-	max (3tCK, 5.625ns)	-	max (3tCK, 5.625ns)	-	
Command pass disable delay		tCPDED	1	-	1	-	1	-	nCK
Power Down Entry to Exit Timing		tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry		tACTPDEN	1	-	1	-	1	-	nCK
Timing of PRE command to Power Down entry		tPRPDEN	1	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry		tRDPDEN	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-	
Timing of WR command to Power Down entry BL8 (OTF, MRS), BL4OTF		tWRPDEN	WL + 4 + (tWR/ tCK(avg))	-	WL + 4 + (tWR/ tCK(avg))	-	WL + 4 + (tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry BL8 (OTF, MRS), BL4OTF		tWRAPDEN	WL+4 +WR+1	-	WL+4 +WR+1	-	WL+4 +WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)		tWRPDEN	WL + 2 + (tWR/ tCK(avg))	-	WL + 2 + (tWR/ tCK(avg))	-	WL + 2 + (tWR/ tCK(avg))	-	nCK

AC TIMING PARAMETERS & SPECIFICATIONS

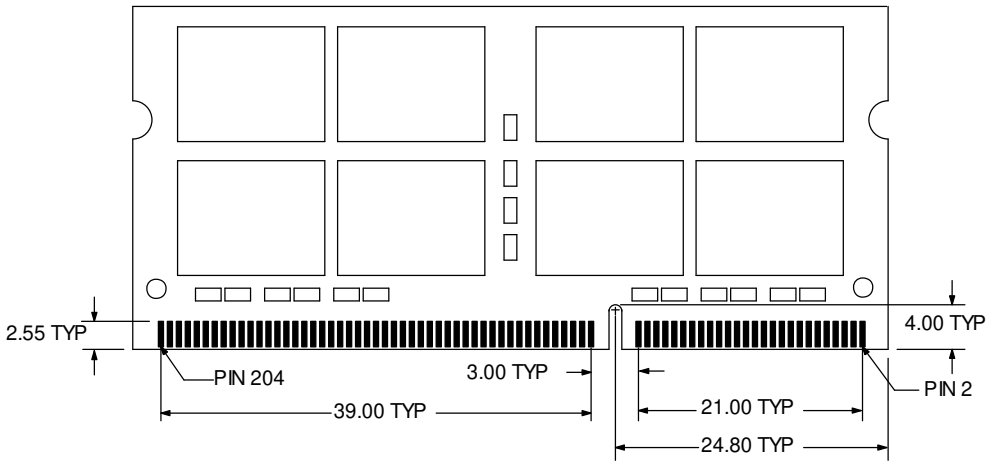
Parameter	Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL+2 +WR+1	-	WL+2 +WR+1	-	WL+2 +WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	
ODT Timing								
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns
ODT turn-on	tAON	-225	225	-250	250	-300	300	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing								
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK
Setup time for tDQSS latch	tWLS	165	-	195	-	245	-	ps
Hold time for tDQSS latch	tWLH	165	-	195	-	245	-	ps
Write leveling output delay	tWLO	0	7.5	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	ns

Package Dimensions

FRONT VIEW



BACK VIEW



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
06/21/2012	1.0	All	Spec released