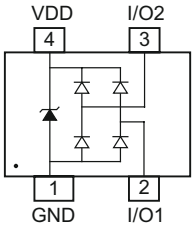
# ESDALD05UJ2

## ESD Protection Diodes Array

Rev.01 - 20 May 2021 Product data sheet

## 1. General description

The ESDALD05UJ2 is a low capacitance TVS (Transient Voltage Suppressor) array designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).




## 2. Features and benefits

- Peak pulse power 136W @ 8/20µs waveform
- Protects two I/O lines and one $V_{CC}$ line
- IEC 61000-4-2 (ESD) ±15kV(air), ±8kV(contact)
- IEC 61000-4-5 (Lightning) 5A (8/20µs)
- Low capacitance
- Low leakage current
- 5V operating voltage
- Solid-state silicon avalanche technology
- Device meets MSL 1 requirements
- Halogen free and RoHS compliant

## 3. Applications

- xDSLI
- USB 2.0
- IEEE 1394 Firewire Ports
- Notebooks & Handhelds
- Projection TV & Monitors
- Set-top box
- Flat Panel Displays

## 4. Ordering information

| Type number | Package Name | Orderable part number | Packing method | Small packing quantity | Marking | Package issue date |
|---|---|---|---|---|---|---|
| ESDALD05UJ2 | SOT143 | ESDALD05UJ2X | Tape and reel | 3000 | R05 | 13-Oct-2020 |

## 5. Absolute maximum ratings

*In accordance with the Absolute Maximum Rating System (IEC 60134).*
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Values | Unit |
|---|---|---|---|---|
| **Absolute maximum rating** | | | | |
| $P_{PPM}$ | peak pulse power | $t_p$ = 8/20 µs | 136 | W |
| $I_{PP}$ | peak pulse current | $t_p$ = 8/20 µs | 8 | A |
| $V_{ESD}$ | ESD per IEC 61000-4-2 (air)<br>ESD per IEC 61000-4-2 (contact) | | ±15<br>±8 | kV<br>kV |
| $T_{stg}$ | storage temperature range | | -55 to 150 | °C |
| $T_j$ | operating temperature range | | -55 to 150 | °C |

## 6. Characteristics

*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse Working Voltage | Any I/O pin to GND | - | - | 5 | V |
| $V_{BR}$ | Reverse Breakdown Voltage | $I_T$ = 1 mA; Any I/O pin to GND | 6 | - | - | V |
| $I_R$ | Reverse Leakage Current | $V_{RWM}$ = 5 V; Any I/O pin to GND | - | - | 100 | nA |
| $V_F$ | Diode Forward Voltage | $I_F$ = 15 mA | - | 0.85 | 1.2 | V |
| $V_C$ | Clamping Voltage | $I_{PP}$ = 1 A; $t_p$ = 8/20 µs; Any I/O pin to GND | - | - | 12 | V |
| | | $I_{PP}$ = 5 A; $t_p$ = 8/20 µs; Any I/O pin to GND | - | - | 15 | V |
| | | $I_{PP}$ = 8 A; $t_p$ = 8/20 µs; Any I/O pin to GND | - | - | 17 | V |
| $C_J$ | Junction Capacitance | $V_R$ = 0 V; f = 1 MHz; Between I/O pins | - | 0.6 | 0.8 | pF |
| | | $V_R$ = 0 V; f = 1 MHz; Any I/O pin to GND | - | 1.35 | - | pF |

Note: I/O pins are pin2,3

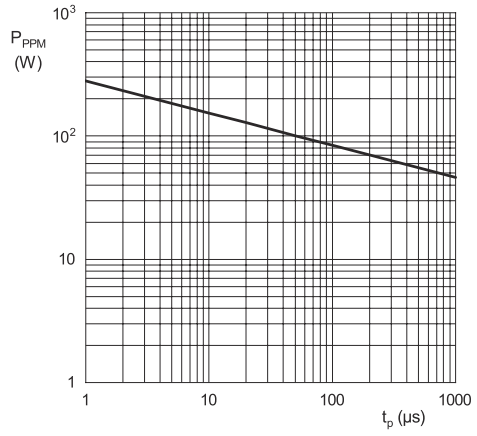



**Fig. 1. Pulse rating curve**

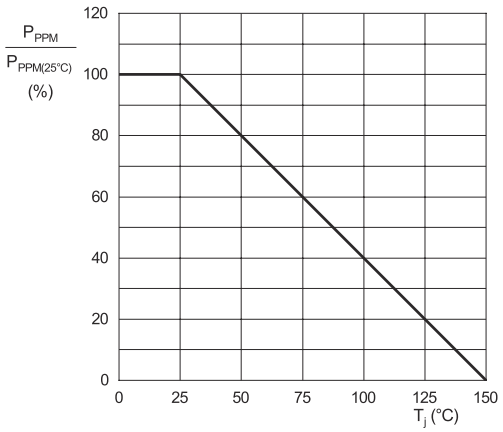



**Fig. 2. Peak pulse power derating curve**

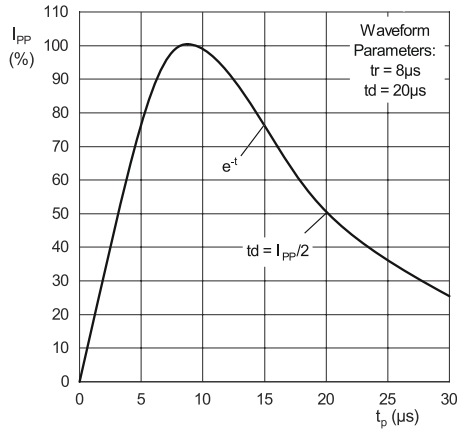



**Fig. 3. Pulse waveform**

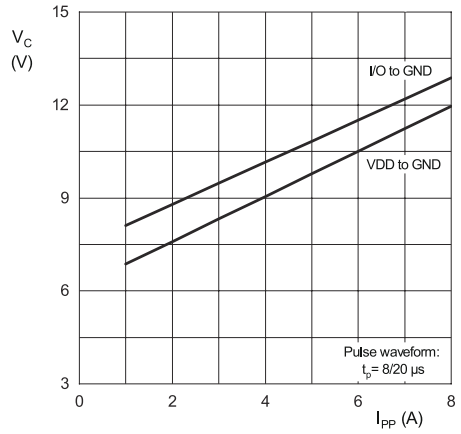



**Fig. 4. Clamping voltage vs Peak pulse current**

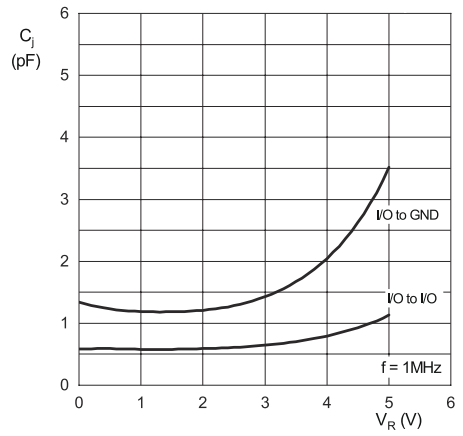



Fig. 5. Capacitance vs Reverse voltage

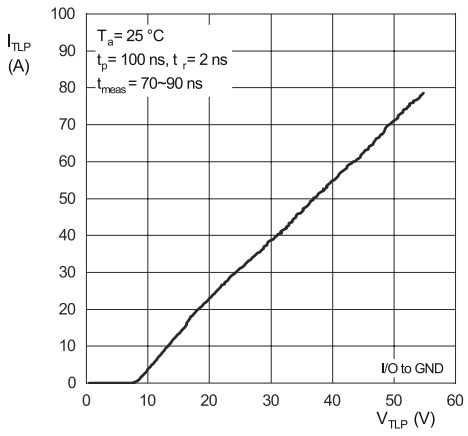



Fig. 6. TLP I-V Curve

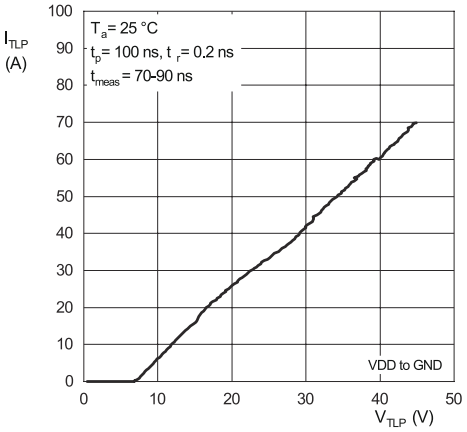



Fig. 7. TLP I-V Curve

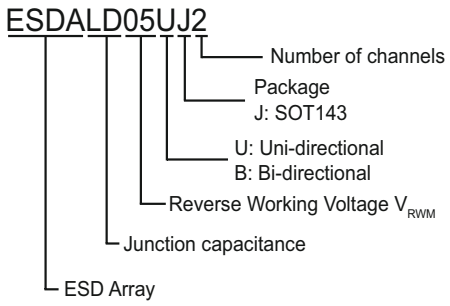
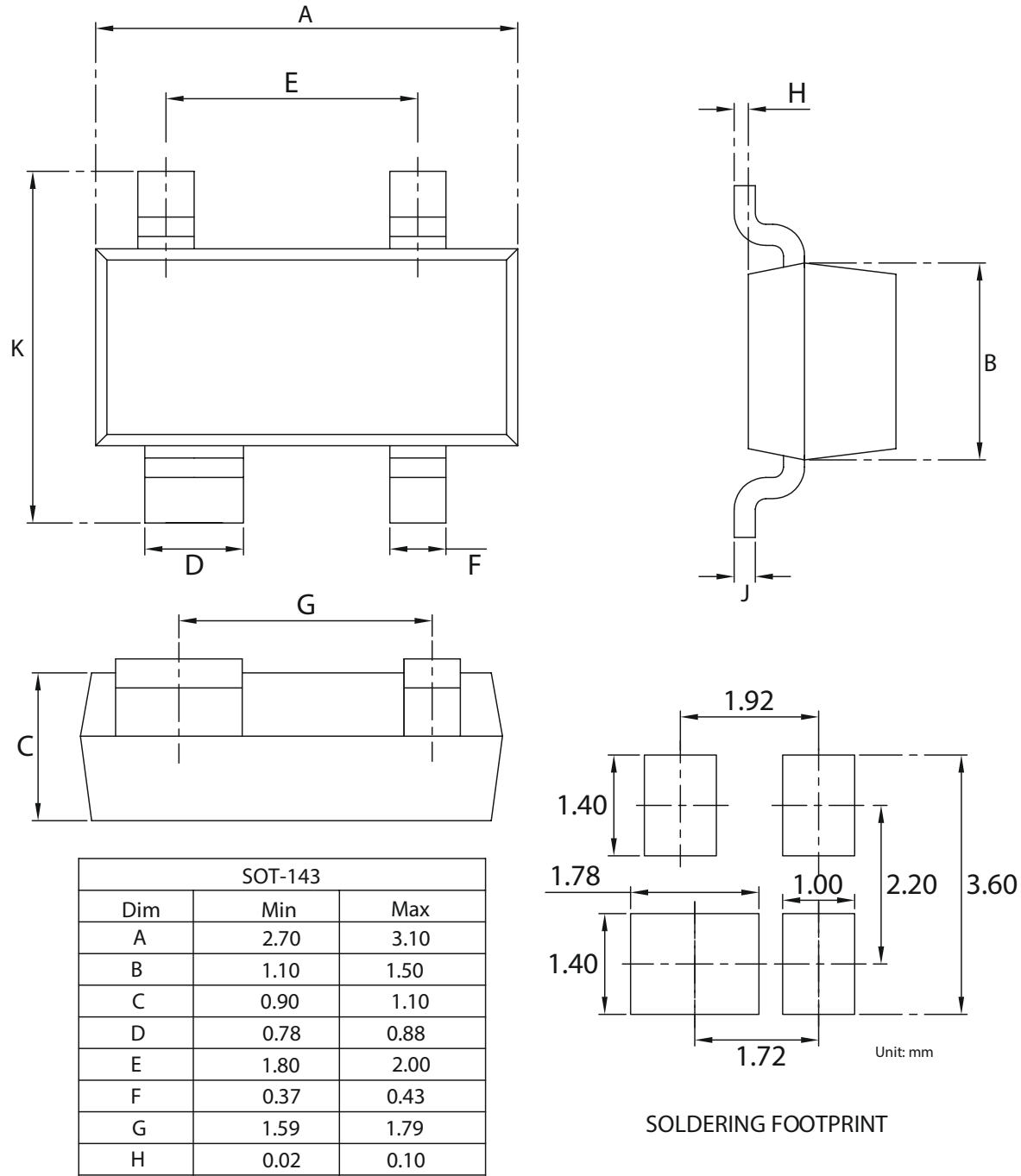



Fig. 8. Part numbering

## 7. Package outline

SOT143




SOLDERING FOOTPRINT

| SOT-143 | | |
|---|---|---|
| Dim | Min | Max |
| A | 2.70 | 3.10 |
| B | 1.10 | 1.50 |
| C | 0.90 | 1.10 |
| D | 0.78 | 0.88 |
| E | 1.80 | 2.00 |
| F | 0.37 | 0.43 |
| G | 1.59 | 1.79 |
| H | 0.02 | 0.10 |
| J | 0.05 | 0.15 |
| K | 2.20 | 2.60 |
| All Dimensions in mm | | |

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## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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[2] The term 'short data sheet' is explained in section "Definitions".
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