

SN74ALVCHR162269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050B – AUGUST 1995 – REVISED JANUARY 1997

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCHR162269 is used in applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed micro-processors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock enable ($\overline{CLKENA}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{SEL}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB1}$, and $\overline{OEB2}$).

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

All outputs are designed to sink up to 12 mA and include 26-Ω resistors to reduce overshoot and undershoot.

The SN74ALVCHR162269 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{OEA}$	1	56	$\overline{OEB2}$
$\overline{OEB1}$	2	55	$\overline{CLKENA2}$
2B3	3	54	2B4
GND	4	53	GND
2B2	5	52	2B5
2B1	6	51	2B6
V_{CC}	7	50	V_{CC}
A1	8	49	2B7
A2	9	48	2B8
A3	10	47	2B9
GND	11	46	GND
A4	12	45	2B10
A5	13	44	2B11
A6	14	43	2B12
A7	15	42	1B12
A8	16	41	1B11
A9	17	40	1B10
GND	18	39	GND
A10	19	38	1B9
A11	20	37	1B8
A12	21	36	1B7
V_{CC}	22	35	V_{CC}
1B1	23	34	1B6
1B2	24	33	1B5
GND	25	32	GND
1B3	26	31	1B4
NC	27	30	$\overline{CLKENA1}$
$\overline{SEL}$	28	29	CLK

NC – No internal connection



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Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE}A$	$\overline{OE}B$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OE}B = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
L	H	↑	L	L	2B ₀ [†]
L	H	↑	H	H	2B ₀ [†]
L	L	↑	L	L	L
L	L	↑	H	H	H
H	L	↑	L	1B ₀ [†]	L
H	L	↑	H	1B ₀ [†]	H
H	H	X	X	1B ₀ [†]	2B ₀ [†]

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OE}A = L$)

INPUTS				OUTPUT A
CLK	$\overline{SEL}$	1B	2B	
X	H	X	X	A ₀ [†]
X	L	X	X	A ₀ [†]
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

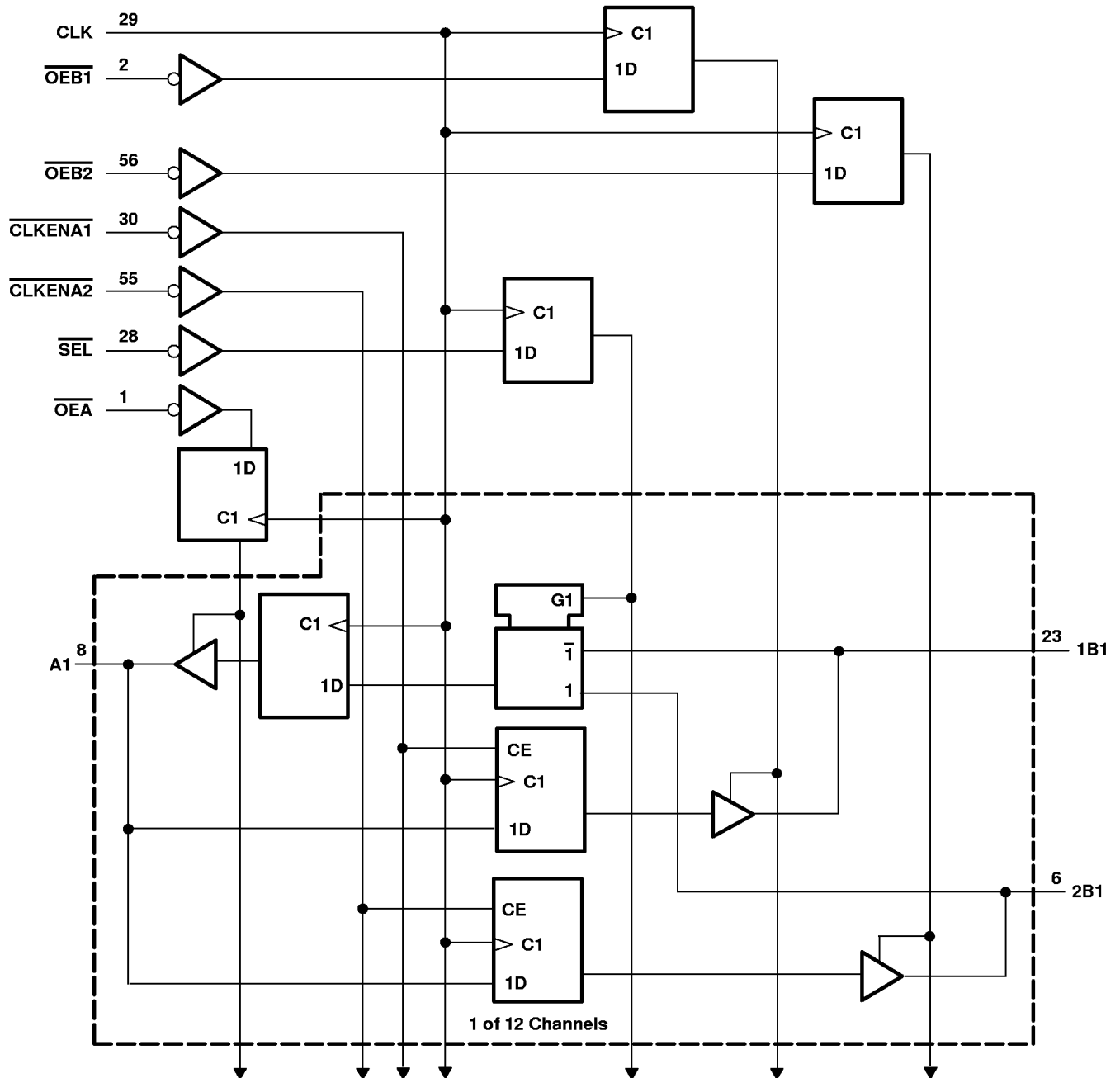
† Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.3 V		−6	mA
		V _{CC} = 2.7 V		−8	
		V _{CC} = 3 V		−12	
I _{OL}	Low-level output current	V _{CC} = 2.3 V		6	mA
		V _{CC} = 2.7 V		8	
		V _{CC} = 3 V		12	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = −100 μA			2.3 V to 3.6 V	V _{CC} −0.2			V
	I _{OH} = −4 mA	V _{IH} = 1.7 V		2.3 V	1.9			
		V _{IH} = 2 V		2.7 V	2.2			
	I _{OH} = −6 mA	V _{IH} = 1.7 V		2.3 V	1.7			
		V _{IH} = 2 V		3 V	2.4			
	I _{OH} = −8 mA,		V _{IH} = 2 V		2.7 V	2		
I _{OH} = −12 mA,		V _{IH} = 2 V		3 V	2			
V _{OL}	I _{OL} = 100 μA			2.3 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	V _{IL} = 0.7 V		2.3 V			0.4	
		V _{IL} = 0.8 V		2.7 V			0.4	
	I _{OL} = 6 mA	V _{IL} = 0.7 V		2.3 V			0.55	
		V _{IL} = 0.8 V		3 V			0.55	
	I _{OL} = 8 mA,		V _{IL} = 0.8 V		2.7 V			
I _{OL} = 12 mA,		V _{IL} = 0.8 V		3 V			0.8	
I _I	V _I = V _{CC} or GND			3.6 V			±5	μA
I _I (hold)	V _I = 0.7 V			2.3 V	45			μA
	V _I = 1.7 V		−45					
	V _I = 0.8 V			3 V	75			
	V _I = 2 V		−75					
	V _I = 0 to 3.6 V			3.6 V	±500			
I _{OZ} §	V _O = V _{CC} or GND‡			3.6 V	±10		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0			3.6 V	40		μA	
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND			3 V to 3.6 V	750		μA	
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V	3.5		pF	
C _{io}	A or B ports	V _O = V _{CC} or GND		3.3 V	9		pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	135	0	135	0	135	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t_{su}	A data before CLK $\uparrow$	2		2		1.7		ns
	B data before CLK $\uparrow$	2.2		2.1		1.8		
	$\overline{\text{SEL}}$ before CLK $\uparrow$	1.6		1.6		1.3		
	CLKENA1 or CLKENA2 before CLK $\uparrow$	1		1.2		0.9		
	$\overline{\text{OE}}$ before CLK $\uparrow$	1.5		1.6		1.3		
t_h	A data after CLK $\uparrow$	0.7		0.6		0.6		ns
	B data after CLK $\uparrow$	0.7		0.6		0.6		
	$\overline{\text{SEL}}$ after CLK $\uparrow$	1.1		0.7		0.7		
	CLKENA1 or CLKENA2 after CLK $\uparrow$	1		0.8		1.1		
	$\overline{\text{OE}}$ after CLK $\uparrow$	0.8		0.8		0.8		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			135		135		135		MHz
t_{pd}	CLK	B	1.5	9.2	7.9		1.6	6.7	ns
		A	1.5	7.4	6.4		1.6	5.5	
t_{en}	CLK	B	1.5	8.8	7.3		1.6	6.6	ns
		A	1.5	8.5	6.8		1.6	6.4	
t_{dis}	CLK	B	1.8	8.7	7.5		1.6	6.5	ns
		A	1.9	8.1	7.4		1.6	6	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	87	120	pF
		Outputs disabled		80.5	118	



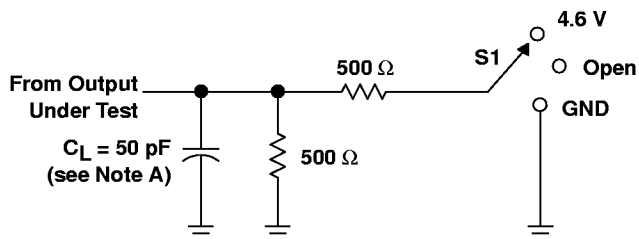
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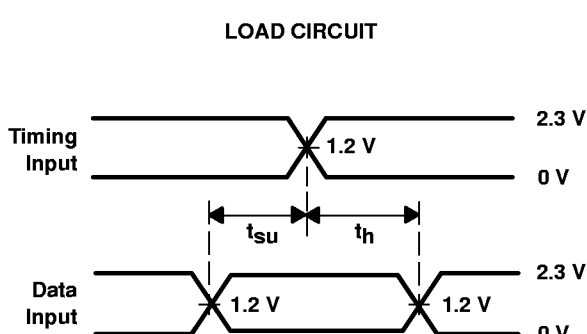
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

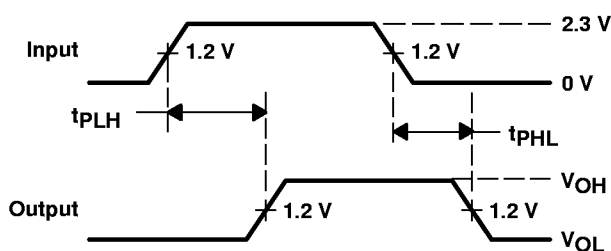


LOAD CIRCUIT

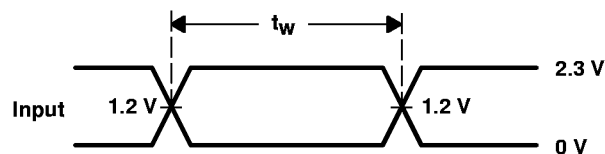
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



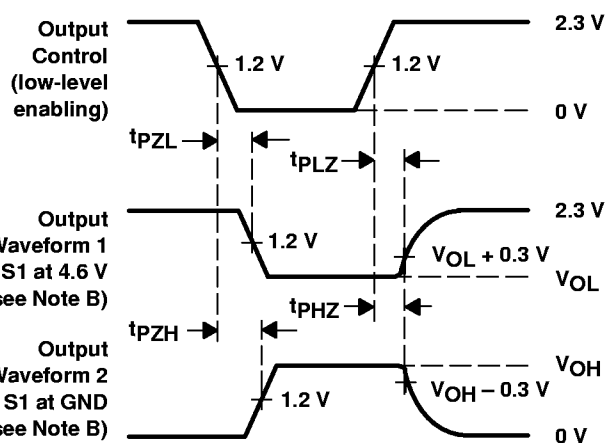
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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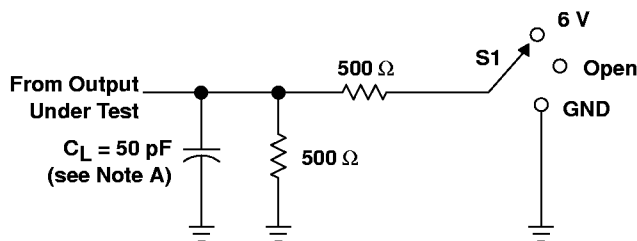
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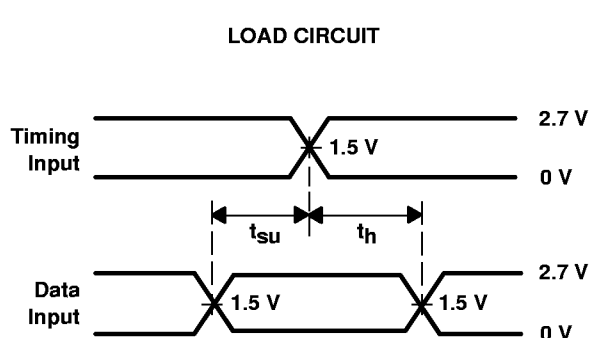
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

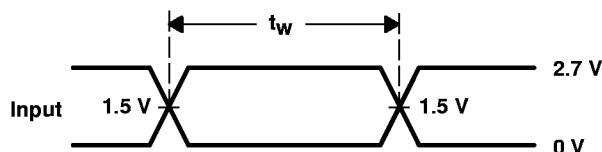


LOAD CIRCUIT

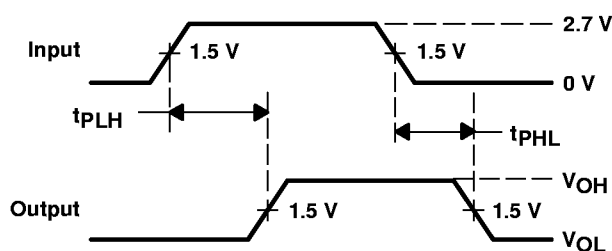
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



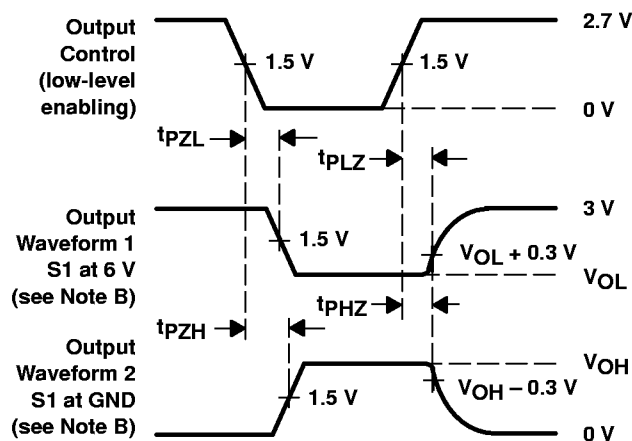
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms