CS4220
CS4221

24-Bit Stereo Audio Codec with 3V Interface

Features

- 100 dB Dynamic Range A/D Converters
- 100 dB Dynamic Range D/A Converters
- 110 dB DAC Signal-to-Noise Ratio (EIAJ)
- Analog Volume Control (CS4221 only)
- Differential Inputs
- Differential Outputs
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32, 44.1 and 48 kHz
- Supports Master and Slave Modes
- Single +5 V power supply
- On-Chip Crystal Oscillator
- 3 - 5 V Digital Interface

Description

The CS4220/1 is a highly integrated, high performance, 24-bit, audio codec providing stereo analog-to-digital and stereo digital-to-analog converters using delta-sigma conversion techniques. The device operates from a single +5 V power supply, and features low power consumption. Selectable de-emphasis filter for 32, 44.1, and 48 kHz sample rates is also included.

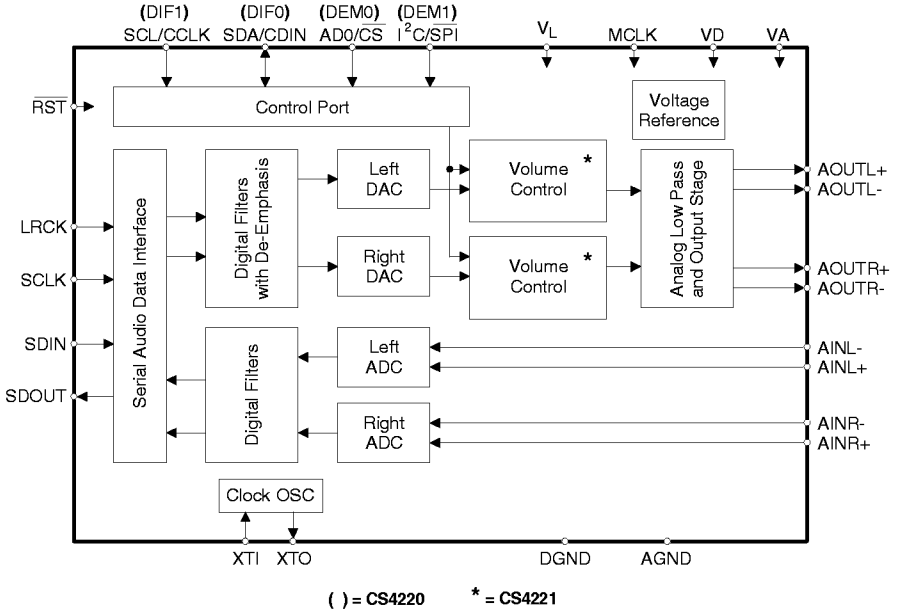
The CS4220/1 also includes an analog volume control capable of 113.5 dB attenuation in 0.5 dB steps. The analog volume control architecture preserves dynamic range during attenuation. Volume control changes are implemented using a "soft" ramping or zero crossing technique.

Applications include digital effects processors, DAT, and multitrack recorders.

The CS4220/1 is packaged in a 28-pin plastic SSOP.

ORDERING INFORMATION

CS4220-KS	-10 to +70 °C	28-pin SSOP
CS4221-KS	-10 to +70 °C	28 pin SSOP
CDB4220/1		Evaluation Board



( ) = CS4220 * = CS4221

Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25 °C; VA, VD = +5 V; Full Scale Input Sine wave, 997 Hz; Fs = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figures 4 and 5; SPI® mode, Format 0, unless otherwise specified.)

Parameter			Symbol	Min	Typ	Max	Unit
Analog Input Characteristics							
ADC Resolution				-	-	24	Bits
Total Harmonic Distortion			THD	-	0.003	-	%
Dynamic Range		A-weighted unweighted		TBD TBD	100 97	- -	dB
Total Harmonic Distortion + Noise	-1 dB	(Note 1)	THD+N	-	-90	TBD	dB
Interchannel Isolation	1 kHz			-	90	-	dB
Interchannel Gain Mismatch				-	0.1	-	dB
Offset Error		with High Pass Filter HPF defeated with CAL		- -	- TBD	0 -	LSB
Full Scale Input Voltage (Differential)				1.9	2.0	2.1	Vrms
Gain Drift				-	100	-	ppm/°C
Input Resistance				10	-	-	kΩ
Input Capacitance				-	-	15	pF
Common Mode Input Voltage				-	2.3	-	V
A/D Decimation Filter Characteristics							
Passband		(Note 2)		0	-	21.8	kHz
Passband Ripple				-	-	±0.01	dB
Stopband		(Note 2)		30	-	6114	kHz
Stopband Attenuation		(Note 3)		80	-	-	dB
Group Delay (Fs = Output Sample Rate)		(Note 4)	t_{gd}	-	15/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0	µs
High Pass Filter Characteristics							
Frequency Response	-3 dB -0.1 dB	(Note 2)		- -	3.7 20	- -	Hz
Phase Deviation	@ 20 Hz	(Note 2)		-	10	-	Degree
Passband Ripple				-	-	0	dB

Notes:
1. Referenced to typical full-scale differential input voltage (2 Vrms).
2. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.
3. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).
4. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312 µs.

* Parameter definitions are given at the end of this data sheet.
Specifications are subject to change without notice

ANALOG CHARACTERISTICS (Continued)

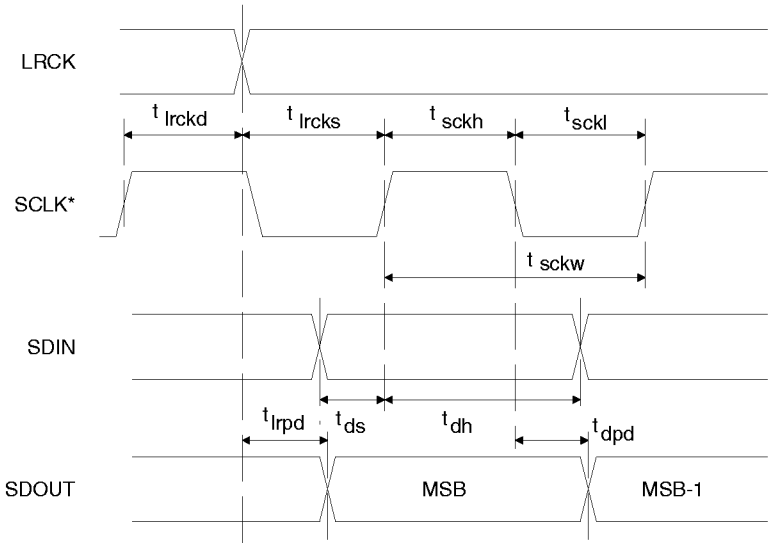
Parameter		Symbol	Min	Typ	Max	Unit
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 100 pF load; unless otherwise specified.						
DAC Resolution			-	-	24	Bits
Signal-to-Noise, Idle-Channel Noise (CS4221 only) DAC muted, A-weighted			TBD	110	-	dB
Dynamic Range	DAC not muted, A-weighted DAC not muted, unweighted		TBD TBD	100 97	- -	dB
Total Harmonic Distortion		THD	-	0.003	-	%
Total Harmonic Distortion + Noise		THD+N	-	-88	TBD	dB
Interchannel Isolation	1 kHz		-	90	-	dB
Interchannel Gain Mismatch			-	0.1	-	dB
Attenuation Step Size	All Outputs		0.35	0.5	0.65	dB
Programmable Output Attenuation Span			110	113.5	-	dB
Differential Offset Voltage			-	±10	-	mV
Common Mode Output Voltage			-	2.3	-	V
Full Scale Output Voltage			1.9	2.0	2.1	Vrms
Gain Drift			-	100	-	ppm/°C
Out-of-Band Energy	Fs/2 to 2 Fs		-	-60	-	dBFs
Analog Output Load	Resistance Capacitance		10 -	- -	- 100	kΩ pF
Combined Digital and Analog Filter Characteristics						
Frequency Response	10 Hz to 20 kHz		-	±0.1	-	dB
Deviation from Linear Phase			-	±0.5	-	Degree
Passband: to 0.01 dB corner	(Notes 5 and 6)		0	-	21.8	kHz
Passband Ripple	(Note 6)		-	-	±0.01	dB
Stopband	(Notes 5 and 6)		26.2	-	-	kHz
Stopband Attenuation	(Note 7)		70	-	-	dB
Group Delay (Fs = Input Word Rate)		t_{gd}	-	16/Fs	-	s
Power Supply						
Power Supply Current	VA VD VL Total Power Down		- - - -	60 20 4 0.8	TBD TBD - -	mA
Power Supply Rejection Ratio	1 kHz, 10 mVrms		-	50	-	dB

Notes:
5. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.5465x Fs.
6. Digital filter characteristics.
7. Measurement bandwidth is 10 Hz to 3 Fs.

SWITCHING CHARACTERISTICS (T_A = 25 °C; VA, VD = +5 V ±5%; outputs loaded with 30 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Audio ADC's & DAC's Sample Rate		Fs	4	-	50	kHz
XTI Frequency	XTI = 256, 384, or 512 Fs		1.024	-	26	MHz
XTI Pulse Width High	XTI = 512 Fs XTI = 384 Fs XTI = 256 Fs		10 21 31	- - -	- - -	ns
XTI Pulse Width Low	XTI = 512 Fs XTI = 384 Fs XTI = 256 Fs		10 21 31	- - -	- - -	ns
XTI Jitter Tolerance			-	500	-	ps
$\overline{\text{RST}}$ Low Time	(Note 8)		10	-	-	psRMS
SCLK falling edge to SDOUT output valid	DSCK = 0	t_{dpd}	-	-	$\frac{1}{(384)\,Fs} + 20$	ns
LRCK edge to MSB valid		t_{lrpd}	-	-	25	ns
SDIN setup time before SCLK rising edge	DSCK = 0	t_{ds}	-	-	25	ns
SDIN hold time after SCLK rising edge	DSCK = 0	t_{dh}	-	-	25	ns
SCLK Period		t_{sckw}	$\frac{1}{(128)\,Fs}$	-	-	ns
SCLK High Time		t_{sckh}	40	-	-	ns
SCLK Low Time		t_{sckl}	40	-	-	ns
SCLK rising to LRCK edge	DSCK = 0	t_{lrckd}	20	-	-	ns
LRCK edge to SCLK rising	DSCK = 0	t_{lrcks}	40	-	-	ns

Notes: 8. After powering up the CS4220/1, PDN should be held low for 10 ms to allow the power supply to settle.



*SCLK shown for DSCK = 0, SCLK inverted for DSCK = 1.

Figure 1. Serial Audio Port Data I/O Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE (T_A = 25 °C; VA, VD = +5 V ±5%; Inputs: logic 0 = DGND, logic 1 = VD; C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode (SPI/I2C = 0)					
CCLK Clock Frequency.		f_{sck}	-	6	MHz
$\overline{RST}$ rising edge to $\overline{CS}$ falling.		t_{srs}	500	-	ns
CCLK edge to $\overline{CS}$ falling.	(Note 9)	t_{spi}	500	-	ns
$\overline{CS}$ High Time between transmissions.		t_{csh}	1.0	-	µs
$\overline{CS}$ falling to CCLK edge.		t_{css}	20	-	ns
CCLK Low Time.		t_{scl}	66	-	ns
CCLK High Time.		t_{sch}	66	-	ns
CDIN to CCLK rising setup time.		t_{dsu}	40	-	ns
CCLK rising to DATA hold time.	(Note 10)	t_{dh}	15	-	ns
Rise time of CCLK and CDIN.	(Note 11)	t_{r2}	-	100	ns
Fall time of CCLK and CDIN.	(Note 11)	t_{f2}	-	100	ns

Notes: 9. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

10. Data must be held for sufficient time to bridge the transition time of CCLK.

11. For F_{SCK} < 1 MHz.

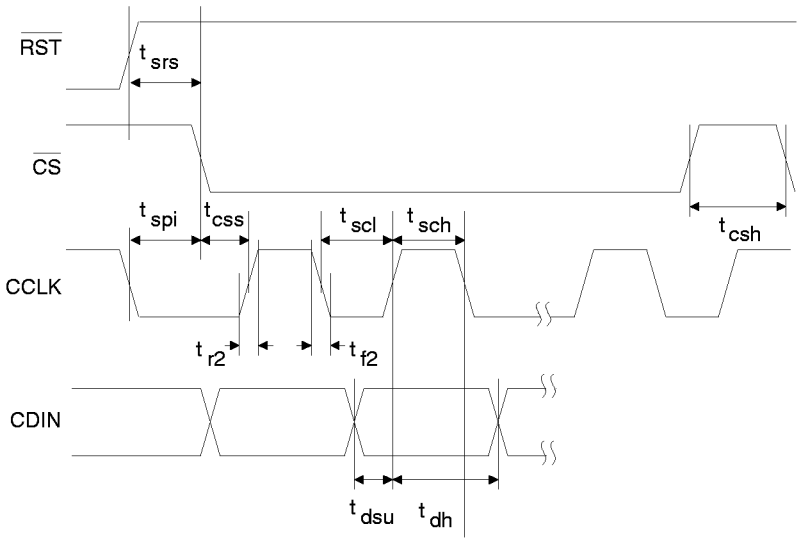


Figure 2. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE (T_A = 25 °C; VA, VD = +5 V ±5%; Inputs: logic 0 = DGND, logic 1 = VD; C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
I²C® Mode ($\overline{SPI}$/I2C = 1)				
SCL Clock Frequency.	f_{scl}	-	100	kHz
$\overline{RST}$ rising edge to Start.	t_{irs}	500	-	ns
Bus Free Time between transmissions.	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse).	t_{hdst}	4.0	-	µs
Clock Low Time.	t_{low}	4.7	-	µs
Clock High Time.	t_{high}	4.0	-	µs
Setup time for repeated Start Condition.	t_{sust}	4.7	-	µs
SDA hold time for SCL falling. (Note 12)	t_{hdd}	0	-	µs
SDA setup time to SCL rising.	t_{sud}	250	-	ns
Rise time of both SDA and SCL lines.	t_r	-	1	µs
Fall time of both SDA and SCL lines.	t_f	-	300	ns
Setup time for Stop Condition.	t_{susp}	4.7	-	µs

Notes: 12. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

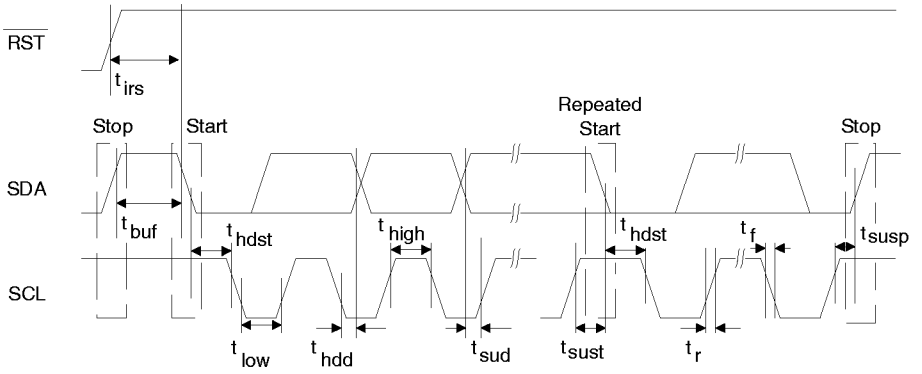


Figure 3. I²C Control Port Timing

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Unit
Power Supplies	Digital Analog	VD VA	-0.3 -0.3	6.0 6.0	V
Input Current	(Note 13)		-	±10	mA
Analog Input Voltage	(Note 14)		-0.7	VA + 0.7	V
Digital Input Voltage	(Note 14)		-0.7	VD + 0.7	V
Ambient Temperature	Power Applied		-55	+125	°C
Storage Temperature			-65	+150	°C

Notes: 13. Any pin except supplies. Transient currents of up to 100 mA on the analog input pins will not cause SCR latch-up.

14. The maximum over or under voltage is limited by the input current.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Digital Analog Digital | VA - VD |	VD VA VL	4.75 4.75 2.7 -	5.0 5.0 5.0 -	5.25 5.25 5.25 0.4	V
Ambient Operating Temperature		T_A	-10	25	70	°C

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA, VD = +5 V ±5%)

Parameter		Symbol	Min	Max	Unit
High-level Input Voltage	VL = 5V VL = 3V	V_{IH}	2.8 2.0	VD + 0.3 VD + 0.3	V V
Low-level Input Voltage		V_{IL}	-0.3	0.8	V
High-level Output Voltage at I_O = -2.0 mA		V_{OH}	VD - 1.0	-	V
Low-level Output Voltage at I_O = 2.0 mA		V_{OL}	-	0.4	V
Input Leakage Current	Digital Inputs		-	10	µA
Output Leakage Current	High Impedance Digital Outputs		-	10	µA

2. TYPICAL CONNECTION DIAGRAM — CS4220

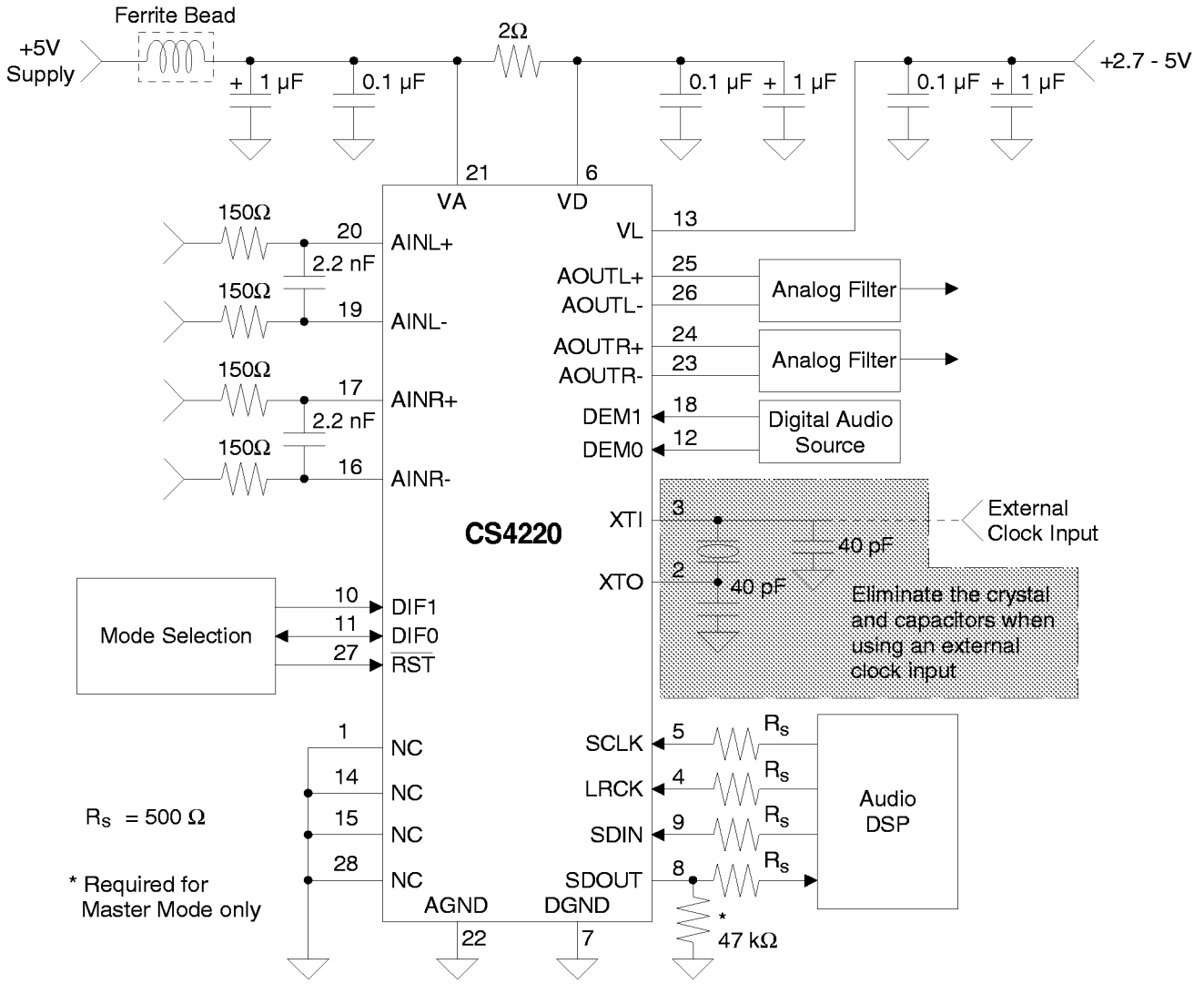


Figure 4. CS4220 Recommended Connection Diagram
(Also see Recommended Layout Diagram, Figure 15)

3. TYPICAL CONNECTION DIAGRAM — CS4221

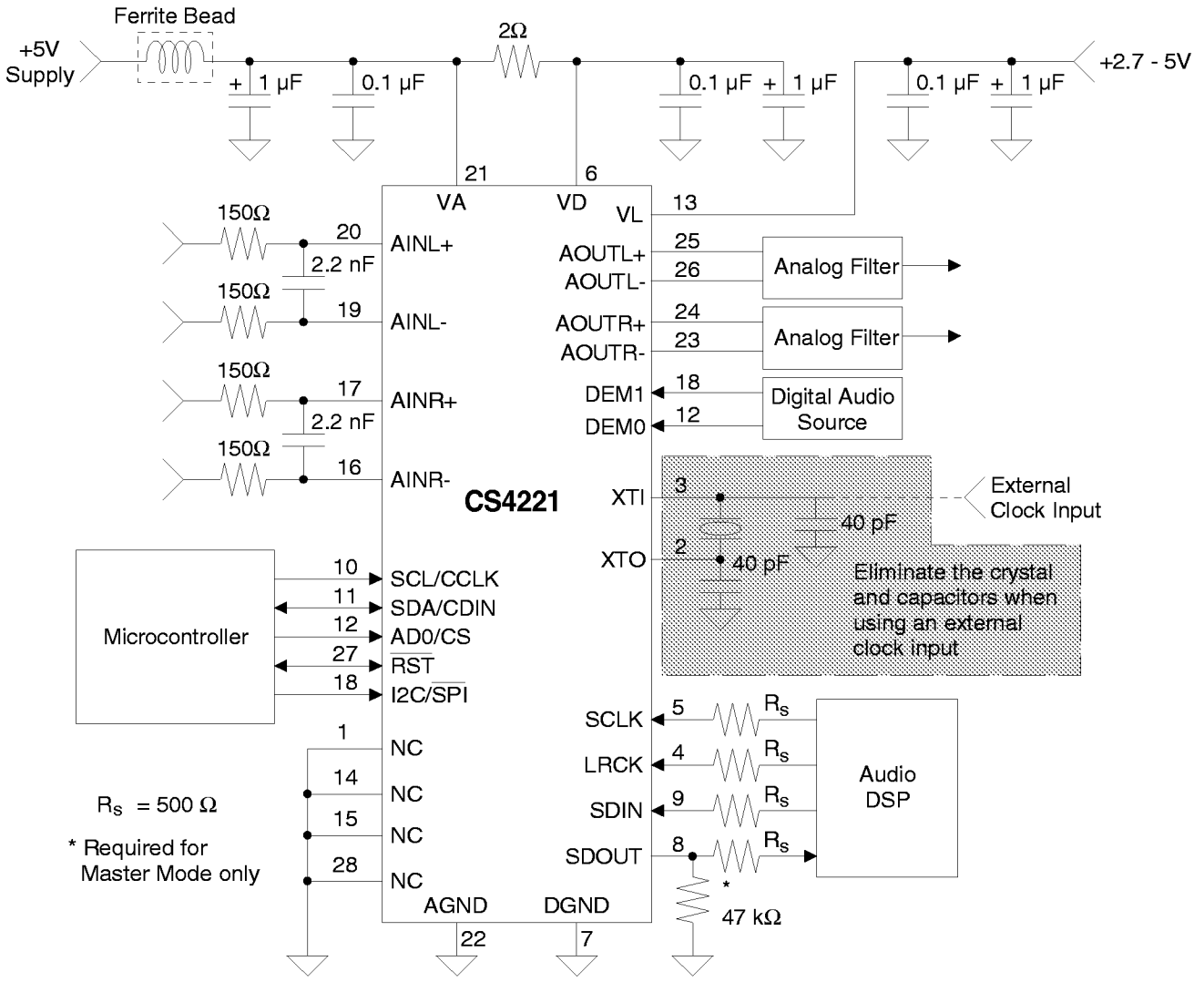


Figure 5. CS4221 Recommended Connection Diagram
(Also see Recommended Layout Diagram, Figure 15)

4. FUNCTIONAL DESCRIPTION

4.1 Overview

The CS4220/1 has 2 channels of 24-bit analog-to-digital conversion and 2 channels of 24-bit digital-to-analog conversion. All ADCs and DACs are delta-sigma converters. The DAC outputs on the CS4221 have adjustable output attenuation implemented in 0.5 dB step resolution. The device also includes digital de-emphasis for 32, 44.1, and 48 kHz.

Digital audio data for the DACs and from the ADCs is communicated over separate serial ports. This allows concurrent writing to and reading from the device. The CS4220 is a stand-alone device controlled via pins. Control for the functions available on the CS4221 are communicated over a serial microcontroller interface. Figures 4 and 5 show the recommended connection diagram for the CS4220 and CS4221.

The CS4221 supports additional functions through the control port interface as outlined in Table 1.

CS4221	CS4220
Volume control	-
Adjustable Mute ramp rate	-
Enable zero crossing detect	-
Enable/Disable mute on zero input	-
De-emphasis	De-emphasis
Mute DAC outputs	-
ADC Input Peak Level Detect	-
20, 24 bit Interface	20, 24 bit Interface
Codec power down	Codec power down
Cal on command	Cal on power-up
High pass enable/disable	High pass enabled

Table 1. CS4221 vs. CS4220

4.2 Analog Inputs

4.2.1 Line Level Inputs

AINR-, AINR+, AINL-, and AINL+ are the differential line level input pins (See Figures 4 and 5). Figure 6 shows an AC coupled optional input buffer which combines level shifting with single-ended to differential conversion. Analog inputs may be AC coupled or DC coupled into the CS4220/1 with a 2.3 V common mode input voltage. Any DC offset at the input to the CS4220/1 will be removed by the internal high-pass filters (see Figure 7 for the differential input signal description). The CS4220/1 may also be driven with a single-ended input as illustrated in Figure 7. The ADC outputs in the CS4221 may be muted (set to zero) by writing the ADMR and ADML bits. ADMR, ADML, and PDN are all located in the ADC control byte (#1).

4.2.2 Input Level Monitoring (CS4221 only)

The CS4221 includes independent Peak Input Level Monitoring for each channel. The analog-to-digital converter continually monitors the peak digital signal for both channels, prior to the digital limiter, and records these values in the LVL2-0 (left channel) and LVR2-0 (right channel) bits in the Converter Status Report Byte (#6). These bits indicate whether the input level is clipping, -1 to -6 dB from full scale in 1 dB resolution, or below -6 dB from full scale. The LVL/LVR bits are "sticky" bits and are reset to zero when read.

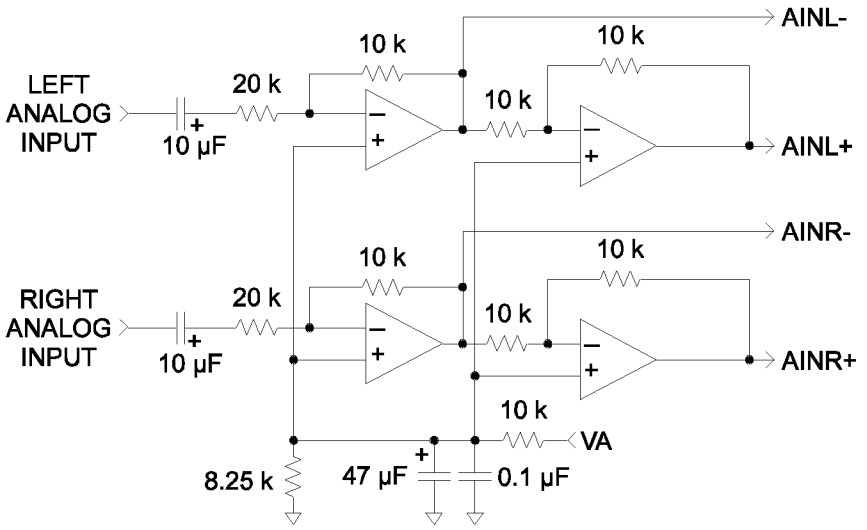


Figure 6. Optional Line Input Buffer

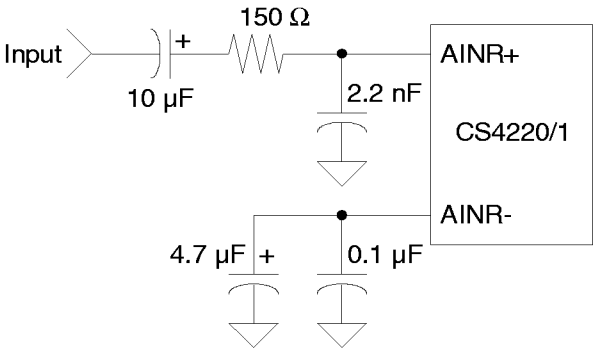


Figure 7. Single-ended Input Application

4.2.3 High Pass Filter

The operational amplifiers in the input circuitry driving the CS4220/1 may generate a small DC offset into the A/D converter. The CS4220/1 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. The characteristics of this first-order high pass filter are outlined below for Fs equal to 48 kHz. The filter response scales linearly with sample rate. The high pass filter in the CS4221 may be defeated independently for the left and right channels by writing HPDR and HPDL in the ADC control byte (#1).

Frequency Response	-3 dB @ 3.7 Hz -0.1 dB @ 20 Hz
Phase Deviation	10 degrees @ 20 Hz
Passband Ripple	None

Table 2. High Pass Filter Characteristics

4.3 Analog Outputs

4.3.1 Line Level Outputs

The CS4220/1 contains an on-chip buffer amplifier producing differential outputs capable of driving 10 kΩ loads. Each output (AOUTL+, AOUTL-, AOUTR+, AOUTR-) will produce a nominal 2.83 Vpp (1 Vrms) output with a 2.3 volt common mode for a full scale digital input. This is equivalent to a 5.66 Vpp (2 Vrms) differential signal as shown in Figure 8. The recommended off-chip analog filter is either a 2nd order Butterworth or a 3rd order Butterworth, if greater out-of-band noise filtering is desired. The CS4220/1 DAC interpolation filter has been pre-compensated for an external 2nd order Butterworth filter with a 3 dB corner at Fs, or a 3rd order Butterworth filter with a 3 dB corner at 0.75 Fs to provide a flat frequency response and linear phase over the passband (see Figure 9 for Fs = 48 kHz). If the recommended filter is not used, small frequency response magnitude and phase errors will occur. In addition to providing out-of-band noise attenuation, the output filters shown in Figure 9 provide differential to single-ended conversion.

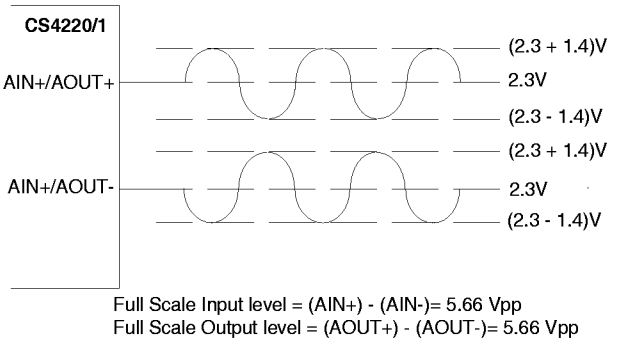


Figure 8. Full Scale Input/Output Voltage

4.3.2 Analog/Digital Volume Control (CS4221 only)

The DAC outputs are each routed through an attenuator which is adjustable in 0.5 dB steps. Output attenuation is available through the Output Attenuator Data Bytes (#3 & #4). Level changes are implemented with an analog volume control until the residual output noise is equal to the noise floor in the mute state at which point volume changes are performed digitally. This technique is superior to purely digital volume control techniques as the noise is attenuated by the same amount as the signal, thus preserving dynamic range (see Figure 10).

The CS4221 implements a "soft" volume control whereby level changes are achieved by ramping from the current level to the new level in 0.5 dB steps. The default rate of volume change is 8 LRCK cycles for each 0.5 dB step (equivalent to 647 µs at Fs = 48 kHz). The rate of volume change is adjustable to 4, 16, or 32 LRCK cycles with the RMP1/0 bits in the DAC control byte (#2).

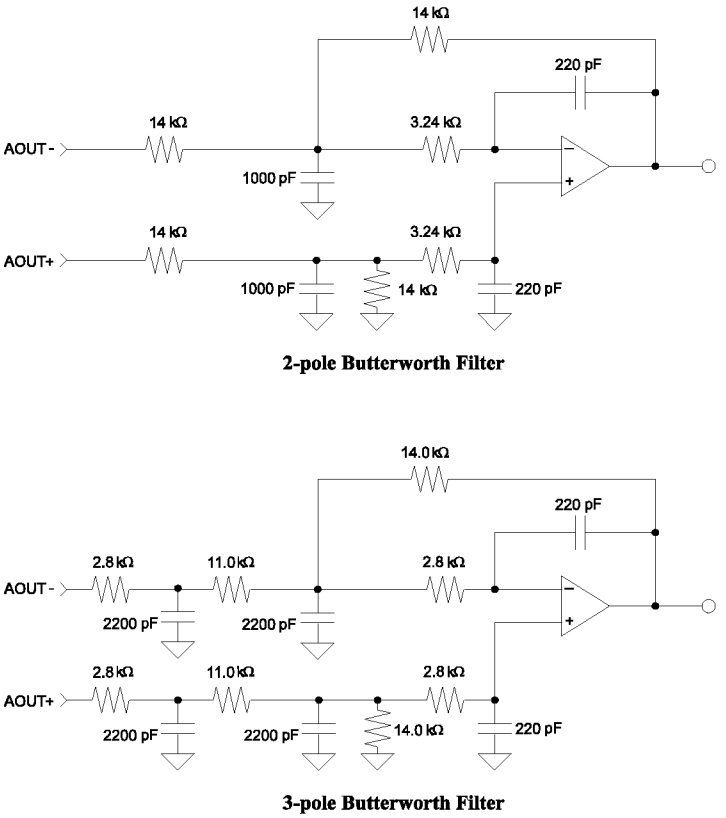


Figure 9. 2- and 3-Pole Butterworth Filters

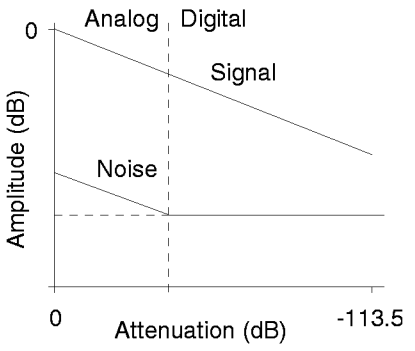


Figure 10. Hybrid Analog/Digital Attenuation

"Soft" volume control may be disabled through the SOFT bit in the DAC bit Control Byte (#2). When "soft" volume control is defeated, level changes step from the current level to the new level in a single step. The volume change takes effect on a zero crossing to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate). There is a separate zero crossing detector for each channel. ACCR and ACCL bits in the Converter Status Report Byte (#6) give feedback on when a volume control change has taken effect for the right and left channel. This bit goes high when a new setting is loaded and returns low when it has taken effect.

4.3.3 Soft Mute/Mute on Zero Input Data (CS4221 only)

Muting is achieved by software control. Under software control, each output can be independently muted via mute control bits, MUTR and MUTL, in the DAC Control Byte (#2). Soft mute output level will ramp down in 0.5 dB steps to a muted state or zero crossing mute will be implemented depending on the state of the SOFT bit in the DAC Control Byte (#2). When "soft" mute is defeated, muting occurs on zero crossings or after a time-out period, similar to the volume control changes.

Muting on consecutive zero input data is also provided where all DAC outputs will mute if they receive between 512 and 1024 consecutive zeros (or -1 code). Detection and muting is done independently for left and right channels. A single non-zero value will immediately unmute the DAC output. This feature is disabled on power-up, and it may be enabled with the MUTC bit in the DAC Control Byte (#2).

4.4 Master Clock Generation

The Master Clock, XTI, is used to operate the digital filters and the delta-sigma modulator. XTI must be either 256x, 384x, or 512x the desired Input Sample Rate, Fs. Fs is the frequency at which digital audio samples for each channel are input to the DAC or output from the ADC and is equal to the LRCK frequency. The XTI to LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of XTI transitions during a single LRCK period. Internal dividers are then set to generate the proper clocks for the digital filters, delta-sigma modulators and switched-capacitor filter. Table 3 illustrates the standard audio sample rates and the required XTI frequencies. If XTI stops for 10 µs, the CS4220/1 will enter a power down state until the clock returns. The control port registers will maintain their current settings. It is required to have SCLK and LRCK derived from the master clock.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 3. Common Clock Frequencies

4.5 Master vs. Slave Mode

The CS4220/1 may be operated in both Master (LRCK and SCLK are outputs) and Slave modes. When a 47 kΩ pulldown resistor is present on SDOUT at startup or after reset, the part will operate in master mode (see Figure 5). Table 4 outlines the

4.6 Serial Audio Data Interface

4.6.1 Serial Audio Interface Signals

The serial interface clock, SCLK, is used for transmitting and receiving audio data. Data is valid on the rising edge of SCLK for both input and output data in the CS4220. In the CS4221, the active edge of SCLK is chosen by setting the DSCK bit in the DSP Port Mode Byte (#5). Data is valid on the rising edge for both input and output upon power up default. SCLK is an input from an external source and at least 24 SCLK's per half period of LRCK are required for proper operation.

The Left/Right clock (LRCK) is used to indicate left and right data and the start of a new sample period. The frequency of LRCK must be equal to the system sample rate, Fs.

SDIN is the data input pin which drives a pair of DACs. SDOUT is the output data pin from the ADC's.

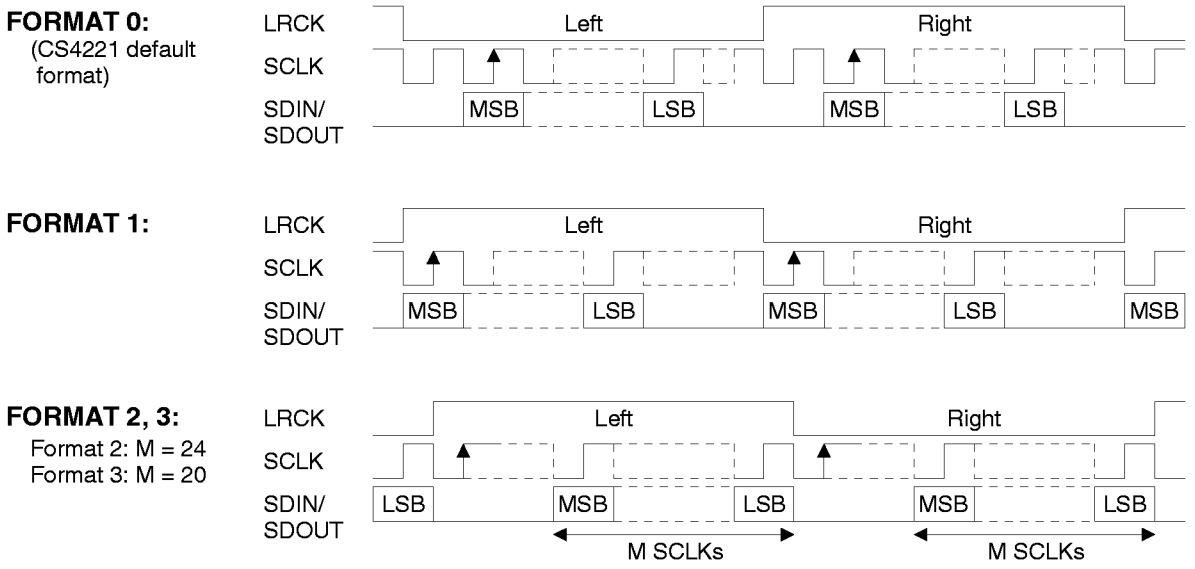
4.6.2 Serial Audio Interface Formats

The serial audio port supports 4 input and 4 output formats, shown in Figure 11. With the CS4220, the interface formats are chosen via the DIF0/DIF1 pins. With the CS4221, these formats are chosen through the DSP Port Mode Byte (#5) with the DDO and DDI2/1/0 bits. The data output format is 24 bits and may be left justified or I^2S compatible depending on the state of the DDO bit. The input data format is set with the DDI bits to be left or right justified or I^2S compatible. When using right-justified mode for SDOUT, SCLK must be 64 Fs in slave mode. In addition, the polarity of the SCLK edge used to clock in/out data from the CS4221 may be set via the DSCK bit in the DSP Port Mode Byte (#5). The default input and output format for the CS4221is I^2S compatible.

	CS4220	CS4221
Slave Mode	XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48, 64, 128 Fs	XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48, 64, 128 Fs
Master Mode	XTI = 256 Fs LRCK = 4 to 50 kHz SCLK = 64 Fs	XTI = Default to 256 Fs (can be changed in Control Port) (Note 15) LRCK = 4 to 50 kHz SCLK = 64 Fs

Table 4. Master Mode vs. Slave Mode Clocking

Notes: 15. Register #7 must be programmed within 1 ms after $\overline{RST}$ de-asserted.



Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.
SCLK must be 64 Fs for Right Justified SDOUT (Formats 2 and 3.)
SDIN and SDOUT can be set to different formats through the Control Port in the CS4221.

Figure 11. Audio DSP Data Input Formats.

4.7 Control Port Interface (CS4221 only)

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI® and I²C®, with the CS4221 operating as a slave device. The control port interface format is selected by the SPI/I2C pin.

4.7.1 SPI Mode

In SPI mode, CS is the CS4221 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 12 shows the operation of the control port in SPI mode. To write to a register, bring CS low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/W), which must be low to write. Register reading from the CS4221 is not supported in the SPI mode. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into a register designated by the MAP.

The CS4221 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive writes. If INCR is set to a 1, then MAP will auto increment after each byte is written, allowing block writes of successive registers. Register reading from the CS4221 is not supported in the SPI mode.

4.7.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 13. There is no CS pin. Pin AD0 forms the partial chip address and should be tied to VD or DGND as desired. The upper 6 bits of the 7 bit address field must be 001000. In order to communicate with the CS4221, the LSB of the chip address field (first byte sent to the CS4221) should match the setting of the AD0 pin. The eighth bit of the address byte is the R/W bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

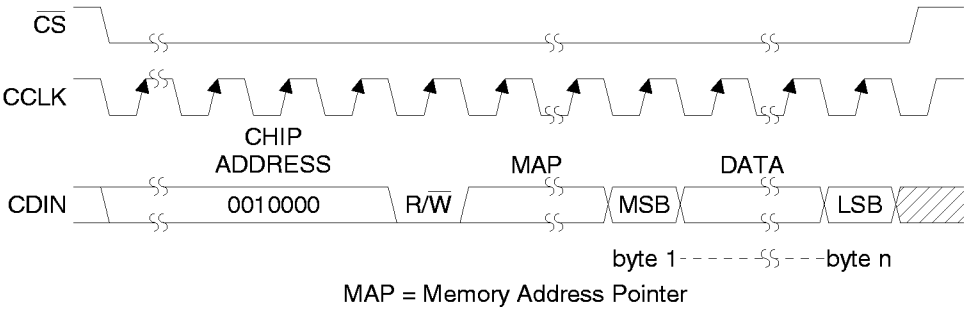


Figure 12. Control Port Timing, SPI mode

4.7.3 Control Port Bit Definitions

All registers can be written and read in I^2C mode, except the Converter Status Report Byte (#6) and the CLKE and CALP bits in the ADC control byte (#1) which are read only. SPI mode only allows for register writing (see the following bit definition tables for bit assignment information).

4.8 De-Emphasis

The CS4220/1 is capable of digital de-emphasis for 32, 44.1, or 48 kHz sample rates. Implementation of digital de-emphasis requires reconfiguration of the digital filter to maintain the filter response at multiple sample rates (see Figure 14).

De-emphasis control is achieved with the DEM1/0 pins on the CS4220 or through the DEM1-0 bits in the DSP Port Mode Byte (#5) on the CS4221. The CS4220 de-emphasis control is defined in Table 5.

DEM 1	DEM 0	De-emphasis
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	OFF

Table 5. CS4220 De-Emphasis filter control

4.9 Power-up/Reset/Power Down/Calibration

Upon power up, the user should hold $\overline{RST}$ = 0 for approximately 10 ms. In this state, the control port is reset to its default settings and the part remains in the power down mode. At the end of $\overline{RST}$, the device performs an offset calibration which lasts approximately 50 ms after which the device enters normal operation. In the CS4221, a calibration may also be initiated via the CAL bit in the ADC Control Byte (#1). The CALP bit in the ADC Control Byte is a read only bit indicating the status of the calibration.

Reset/Power Down is achieved by lowering the $\overline{RST}$ pin causing the part to enter power down. Once $\overline{RST}$ goes high, the control port is functional and the desired settings should be loaded.

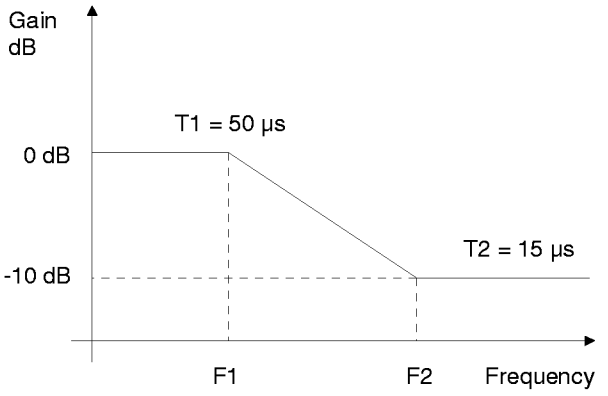


Figure 14. De-emphasis Curve.

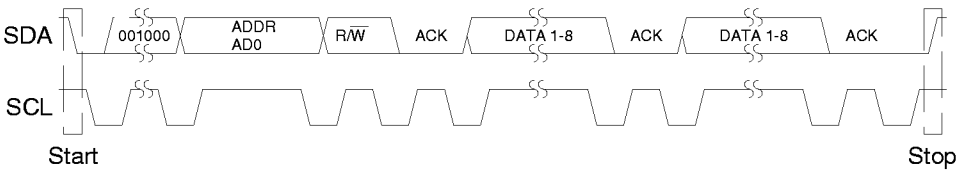


Figure 13. Control Port Timing, I^2C mode

The CS4220/1 will also enter power down mode if the master clock source stops for approximately 10 µs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings.

If PDN is set to 1, the chip will power down. The control port will retain its current settings.

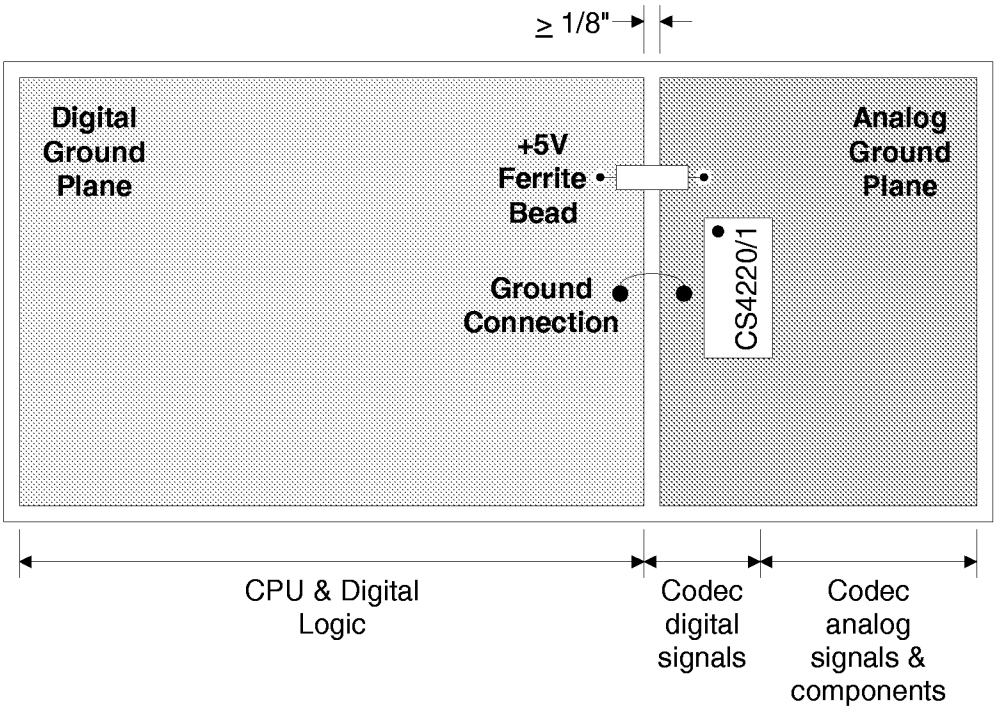
The CS4220/1 will mute the analog outputs and enter the power down mode if the supply drops below approximately 4 volts.

4.10 Power Supply, Layout and Grounding

The CS4220/1 should be located on the analog ground plane along with associated analog circuitry and should be positioned near the split between ground planes (see Figure 15). Preferably, the device should also have its own power plane. The +5 V supply should be connected to the CS4220/1 via a ferrite bead, positioned closer than 1" to the device. A single connection between the CS4220/1 ground and the board ground should be positioned as shown in Figure 15. See the CDB4220/1 evaluation board data sheet for recommended layout of the decoupling components.

4.11 ADC and DAC Filter Response Plots

Figures 16 through 21 show the overall frequency response, passband ripple and transition band for the CS4220/1 ADC's and DAC's.



Note that the CS4220/1 is oriented with its digital pins towards the digital end of the board.

Figure 15. Suggested Layout Guideline (See CDB4220/21 Data Sheet)

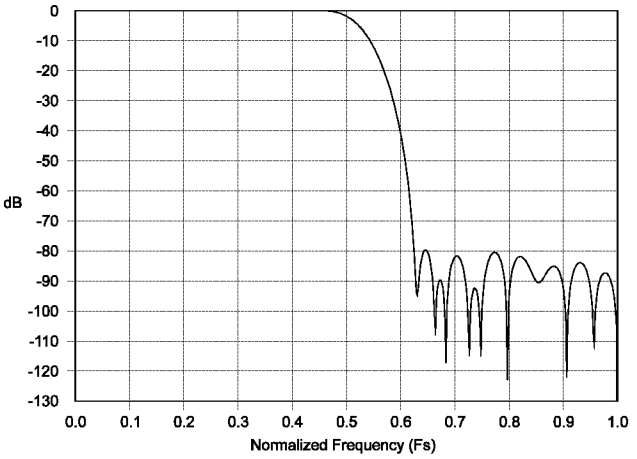


Figure 16. ADC Filter Response

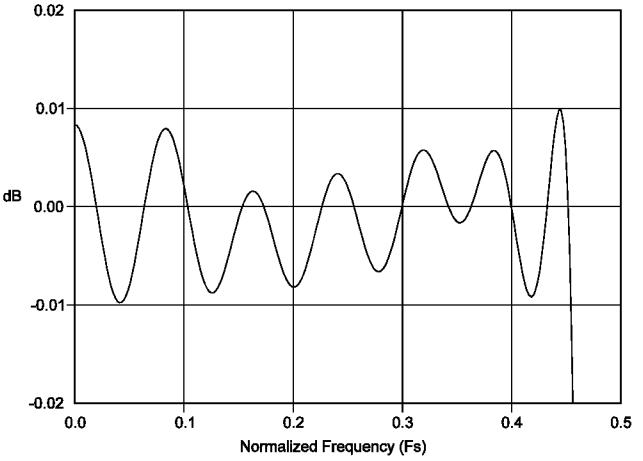


Figure 17. ADC Passband Ripplee

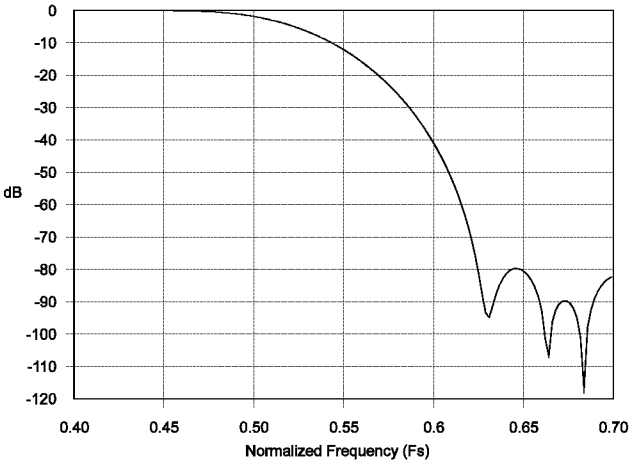


Figure 18. ADC Transition Band

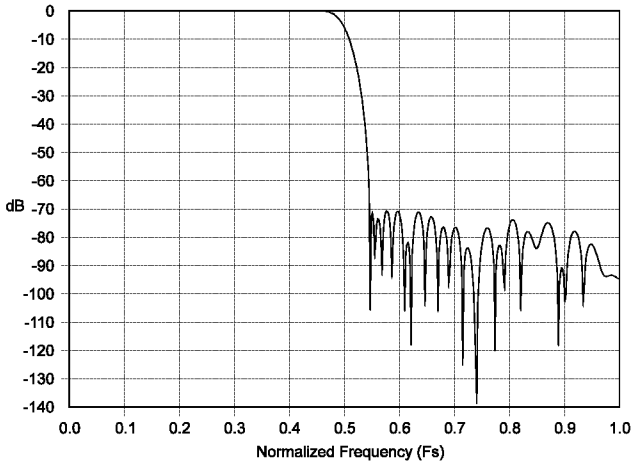


Figure 19. DAC Filter Response

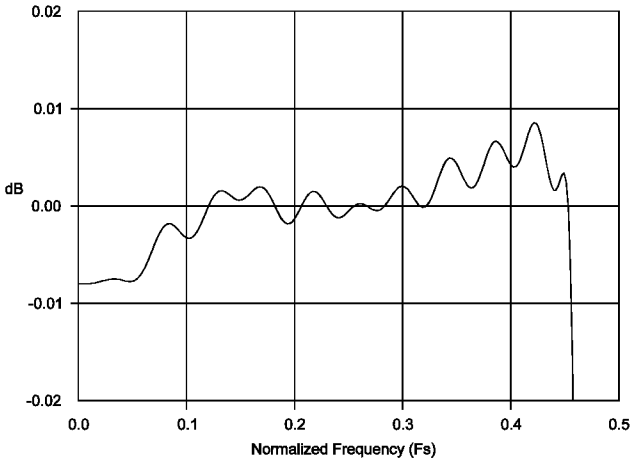


Figure 20. DAC Passband Ripple

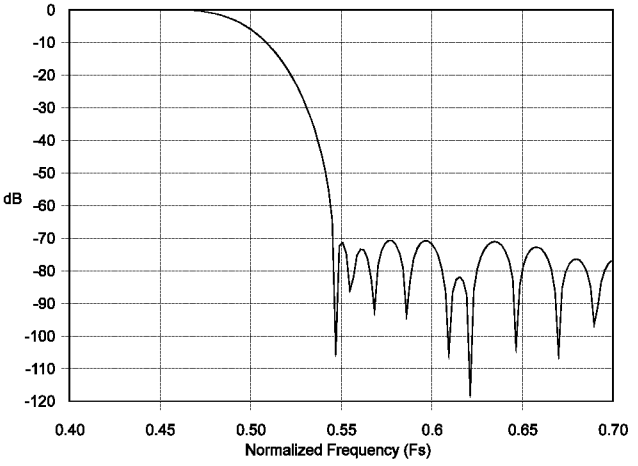


Figure 21. DAC Transition Band

5. REGISTER DESCRIPTIONS

Memory Address Pointer (MAP)

B7	B6	B5	B4	B3	B2	B1	B0
INCR	0	0	0	0	MAP2	MAP1	MAP0

MAP2-MAP0 Register Pointer

INCR Auto Increment Control Bit
0 - No auto increment
1 - Auto increment on

This register defaults to 00h.

Reserved Byte (0)

This byte is reserved for internal use and must be set to 00h for normal operation.

This register defaults to 00h.

ADC Control Byte (1)

B7	B6	B5	B4	B3	B2	B1	B0
PDN	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE

PDN Power Down ADC
0 - Normal
1 - Power Down

HPDR-HPDL High pass filter defeat, right and left
0 - High pass filters active
1 - High pass filters defeated

ADMR-ADML ADC Muting, right and left
0 - Normal
1 - Output muted

CAL Calibration control bit
0 - Normal operation
1 - Rising edge initiates calibration

The following bits are read only:

CALP Calibration status
0 - Calibration done
1 - Calibration in progress

CLKE Clocking Error
0 - No error
1 - error

This register defaults to 00h.

DAC Control Byte (2)

B7	B6	B5	B4	B3	B2	B1	B0
0	MUTC	MUTR	MUTL	SOFT	0	RMP1	RMP0

MUTC — Controls mute on consecutive zeros function
0 -DAC output will not mute on zeros.
1 -512 consecutive zeros will mute DAC

MUTR-MUTL — Mute control bits
0 - Normal output level
1 - Selected DAC output muted

SOFT — Soft Mute Control
0 - Volume control changes, muting and mute-on-zeros occur with "ramp"
1 - Volume control changes, muting and mute-on-zeros occur on zero crossings

RMP1-0 — Soft Volume 0.5 dB step rate
0 - 1 step per 8 LRCK's
1 - 1 step per 4 LRCK's
2 - 1 step per 16 LRCK's
3 - 1 step per 32 LRCK's

This register defaults to 00h.

Output Attenuator Data Byte (3, 4)

B7	B6	B5	B4	B3	B2	B1	B0
ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

ATT7-ATT0 — Sets attenuator level
0 - No attenuation
227 - 113.5 dB attenuation
>227 - DAC muted
ATT0 represents 0.5 dB of attenuation

This register defaults to 00h.

DSP Port Mode Byte (5)

B7	B6	B5	B4	B3	B2	B1	B0
0	DEM1	DEM0	DSCK	DOF1	DOF0	DIF1	DIF0

DEM1-0 Selects de-emphasis control source
0 - 44.1 kHz de-emphasis setting
1 - 48 kHz de-emphasis setting
2 - 32 kHz de-emphasis setting
3 - De-emphasis disabled

DSCK Sets the polarity of clocking data for both input and output
0 - Data valid on rising edge of SCLK
1 - Data valid on falling edge of SCLK

DOF1-DOF0 Data output format
0 - I^2S compatible
1 - Left justified
2 - Right Justified, 24-bit
3 - Right Justified, 20-bit

DIF1-DIF0 Data input format
0 - I^2S compatible
1 - Left justified
2 - Right justified, 24-bit
3 - Right justified, 20-bit

This register defaults to 00h.

Converter Status Report Byte (Read Only) (6)

B7	B6	B5	B4	B3	B2	B1	B0
ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL2	LVL0

ACCR-ACCL Acceptance bit
0 - ATT7-0 has been accepted
1 - New setting waiting for zero crossing

LVL2-0,LVR2-0 Left and Right ADC output level
0 - Normal output levels
1 - -6 dB level
2 - -5 dB level
3 - -4 dB level
4 - -3 dB level
5 - -2 dB level
6 - -1 dB level
7 - Clipping

LVL2-0 and LVR2-0 bits are 'sticky'. They constantly monitor the ADC output for the peak levels and hold the maximum output. They are reset to 0 when read.

This register is read only.

Clock/Output Control Byte (7)

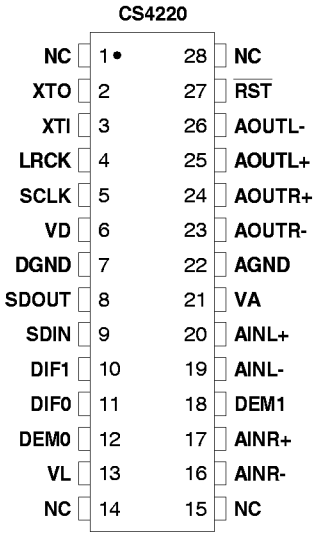
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	MCK1	MCK0

MCK1-0 Master Clock Control
0 - XTI = 256 for Master Mode
1 - XTI = 384 for Master Mode
2 - XTI = 512 for Master Mode

The setting of these bits are not valid in Slave Mode.

This register defaults to 0.

6. PIN DESCRIPTIONS — CS4220



Power Supply

Positive Analog Power — VA

Pin 21

Function:

Positive analog supply. Nominally +5 volts.

Positive Digital Power — VD

Pin 6

Function:

Positive supply for the digital section. Nominally +5 volts.

Positive Digital Logic Power — VL

Pin 13

Function:

Positive supply for the digital interface section. Nominally 3-5 volts.

Analog Ground — AGND

Pin 22

Function:

Analog ground reference.

Digital Ground — DGND

Pin 7

Function:

Digital ground for the digital section.

Analog Inputs

Differential Right Channel Analog Input — AINR-, AINR+

Pins 16 and 17

Function:

Analog input connections of the right channel differential inputs. Typically 2 Vrms differential (1 Vrms for each input pin) for a full-scale analog input signal.

Differential Left Channel Analog Input — AINL-, AINL+

Pins 19 and 20

Function:

Analog input connections of the left channel differential inputs. Typically 2 Vrms differential (1 Vrms for each input pin) for a full-scale analog input signal.

Analog Outputs

Differential Right Channel Analog Outputs — AOUTR-, AOUTR+

Pins 23 and 24

Function:

Analog output connections for the Right channel differential outputs. Nominally 2 Vrms (differential) for full-scale digital input signal.

Differential Left Channel Analog Outputs — AOUTL-, AOUTL+

Pins 25 and 26

Function:

Analog output connections for the Left channel differential outputs. Nominally 2 Vrms (differential) for full-scale digital input signal.

Digital Inputs

Crystal Connections — XTI, XTO

Pins 3, 2

Function:

Input and output connections for the crystal used to clock the CS4220. Alternatively a clock may be input into XTI. This is the clock source for the delta-sigma modulator sampling and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs in Slave Mode and 256x in Master Mode.

Left/Right Clock — LRCK

Pin 4

Function:

LRCK determines which channel, left or right, is to be input/output on SDIN/SDOUT. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. LRCK is an input clock whose frequency must be equal to Fs.

Serial Data Clock — SCLK

Pin 5

Function:

Clocks the individual bits of the serial data out from SDOUT and in from SDIN.

Serial Data Input — SDIN

Pin 9

Function:

Two's complement MSB-first serial data of either 20 or 24 bits is input on this pin. The data is clocked into the CS4220 via the SCLK clock and the channel is determined by the LRCK clock. The interface format is selected by the DIF0 and DIF1 pins.

De-Emphasis Select — DEM0, DEM1

Pins 12 and 18

Function:

Controls the activation of the standard 50/15 µs de-emphasis filter. 32, 44.1, or 48 kHz sample rate selection defined in Table 5.

Digital Input Format — DIF0, DIF1

Pins 11 and 10

Function:

These pins select one of four formats for the input/output serial data stream. These pins set the format of the SCLK and LRCK clocks with respect to SDATA. The formats are shown in Figure 11.

Digital Outputs

Serial Data Output — SDOUT

Pin 8

Function:

Two's complement MSB-first serial data of 20-24 bits is output on this pin. The data is clocked out via the SCLK clock and the channel is determined by LRCK.

Miscellaneous Pins

Reset — $\overline{\text{RST}}$

Pin 27

Function:

When low, the CS4220 enters a low power mode and all internal states are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

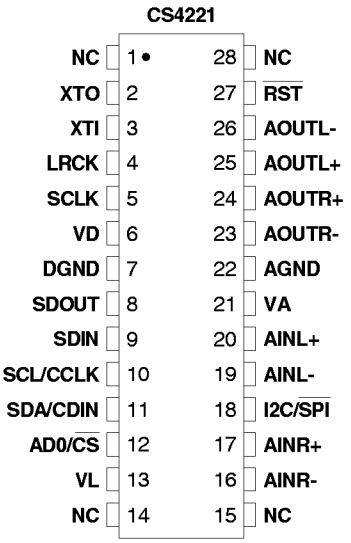
No Connect — NC

Pins 1, 14, 15 and 28

Function:

These pins are not connected internally and should be tied to DGND to minimize noise coupling.

7. PIN DESCRIPTIONS — CS4221



Power Supply

Positive Analog Power — VA

Pin 21

Function:

Positive analog supply. Nominally +5 volts.

Positive Digital Power — VD

Pin 6

Function:

Positive supply for the digital section. Nominally +5 volts.

Positive Digital Logic Power — VL

Pin 13

Function:

Positive supply for the digital interface section. Nominally 3-5 volts.

Analog Ground — AGND

Pin 22

Function:

Analog ground reference.

Digital Ground — DGND

Pin 7

Function:

Digital ground for the digital section.

Analog Inputs

Differential Right Channel Analog Input — AINR-, AINR+

Pins 16 and 17

Function:

Analog input connections of the right channel differential inputs. Typically 2 Vrms differential (1 Vrms for each input pin) for a full-scale analog input signal.

Differential Left Channel Analog Input — AINL-, AINL+

Pins 19 and 20

Function:

Analog input connections of the left channel differential inputs. Typically 2 Vrms differential (1 Vrms for each input pin) for a full-scale analog input signal.

Analog Outputs

Differential Right Channel Analog Outputs — AOUTR-, AOUTR+

Pins 23 and 24

Function:

Analog output connections for the Right channel differential outputs. Nominally 2 Vrms (differential) for full-scale digital input signal.

Differential Left Channel Analog Outputs — AOUTL-, AOUTL+

Pins 25 and 26

Function:

Analog output connections for the Left channel differential outputs. Nominally 2 Vrms (differential) for full-scale digital input signal.

Digital Inputs

Crystal Connections — XTI, XTO

Pins 3, 2

Function:

Input and output connections for the crystal used to clock the CS4221. Alternatively a clock may be input into XTI. This is the clock source for the delta-sigma modulator sampling and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs. The default XTI setting in Master Mode is 256x, but this may be changed to 384x or 512x through the Control Port.

Left/Right Clock — LRCK

Pin 4

Function:

LRCK determines which channel, left or right, is to be input/output on SDIN/SDOUT. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. LRCK is an input clock whose frequency must be equal to Fs.

Serial Data Clock — SCLK

Pin 5

Function:

Clocks the individual bits of the serial data out from SDOUT and in from SDIN.

Serial Data Input — SDIN

Pin 9

Function:

Two's complement MSB-first serial data of either 20 or 24 bits is input on this pin. The data is clocked into the CS4221 via the SCLK clock and the channel is determined by the LRCK clock. The default interface format on power-up is an I^2S compatible 24-bit interface. This may be changed by writing the control port (DSP Port Mode Byte #5).

Control Port Format — I^2C / $\overline{SPI}$

Pin 18

Function:

When this pin is high, I^2C mode is selected, when low, $\overline{SPI}$ is selected.

Digital Outputs

Serial Data Output — SDOUT

Pin 8

Function:

Two's complement MSB-first serial data of 24 bits is output on this pin. The data is clocked out via the SCLK clock and the channel is determined by LRCK.

Control Port Signals

Serial Control Interface Clock — SCL/CCLK

Pin 10

Function:

SCL/CCLK is the serial control interface clock and is used to clock control bits into and out of the CS4221.

Address Bit/Control Port Chip Select — AD0/$\overline{CS}$

Pin 12

Function:

In I^2C mode, AD0 is a chip address bit. In SPI mode, $\overline{CS}$ is used to enable the control port interface on the CS4221. The CS4221 control port interface is defined by the $\overline{SPI}$/I2C pin.

Serial Control Data In — SDA/CDIN

Pin 11

Function:

SDA/CDIN is the input data line for the control port interface.

Miscellaneous Pins

Reset — $\overline{\text{RST}}$

Pin 27

Function:

When low, the CS4221 enters a low power mode and all internal states are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

No Connect — NC

Pins 1, 14, 15 and 28

Function:

These pins are not connected internally and should be tied to DGND to minimize noise coupling.

8. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFS as suggested in AES17-1991 Annex A and DACs are measured at 0 dBFS.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1 kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

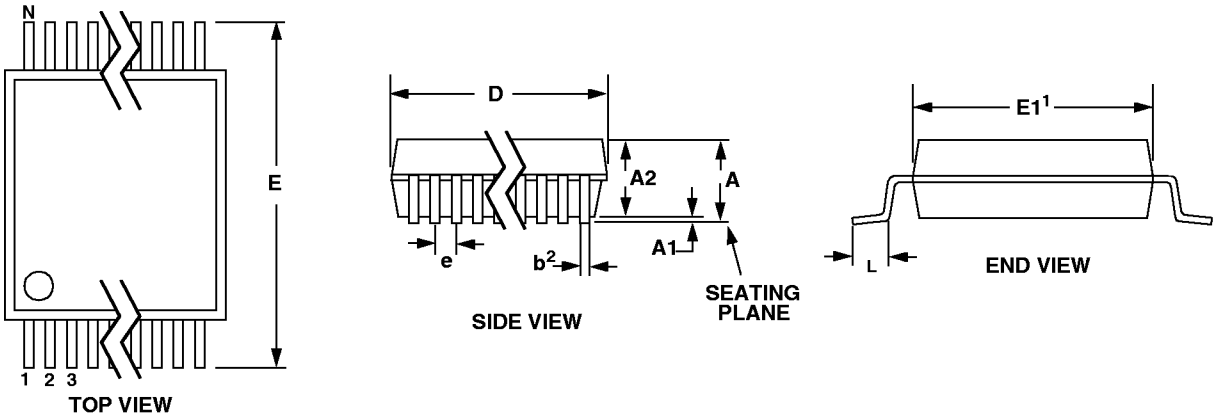
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected inputs tied to a common potential. For the DAC's, the differential output voltage with mid-scale input code. Units are in volts.

9. PACKAGE DIMENSIONS

28 PIN SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	17,18
D	0.390	0.413	9.90	10.50	16
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	16
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
µ	0°	8°	0°	8°	

Notes: 16. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

17. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

18. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.