# Features

- **High Performance, Low Power AVR® 8-Bit Microcontroller**
- **Advanced RISC Architecture**
  - **130 Powerful Instructions – Most Single Clock Cycle Execution**
  - **32 x 8 General Purpose Working Registers**
  - **Fully Static Operation**
  - **Up to 16 MIPS Throughput at 16 MHz**
  - **On-Chip 2-cycle Multiplier**
- **Non-volatile Program and Data Memories**
  - **16K bytes of In-System Self-Programmable Flash**
    - **Endurance: 10,000 Write/Erase Cycles**
  - **Optional Boot Code Section with Independent Lock Bits**
    - **In-System Programming by On-chip Boot Program**
    - **True Read-While-Write Operation**
  - **512 bytes EEPROM**
    - **Endurance: 100,000 Write/Erase Cycles**
  - **1K byte Internal SRAM**
  - **Programming Lock for Software Security**
- **JTAG (IEEE std. 1149.1 compliant) Interface**
  - **Boundary-scan Capabilities According to the JTAG Standard**
  - **Extensive On-chip Debug Support**
  - **Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface**
- **Peripheral Features**
  - **4 x 25 Segment LCD Driver**
  - **Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode**
  - **One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode**
  - **Real Time Counter with Separate Oscillator**
  - **Four PWM Channels**
  - **8-channel, 10-bit ADC**
  - **Programmable Serial USART**
  - **Master/Slave SPI Serial Interface**
  - **Universal Serial Interface with Start Condition Detector**
  - **Programmable Watchdog Timer with Separate On-chip Oscillator**
  - **On-chip Analog Comparator**
  - **Interrupt and Wake-up on Pin Change**
- **Special Microcontroller Features**
  - **Power-on Reset and Programmable Brown-out Detection**
  - **Internal Calibrated Oscillator**
  - **External and Internal Interrupt Sources**
  - **Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby**
- **I/O and Packages**
  - **53 Programmable I/O Lines**
  - **64-lead TQFP and 64-pad MLF**
- **Operating Voltage:**
  - **1.8 - 5.5V for ATmega169V**
  - **2.7 - 5.5V for ATmega169L**
  - **4.5 - 5.5V for ATmega169**
- **Temperature range:**
  - **-40°C to 85°C Industrial**

# 8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

## ATmega169V
## ATmega169L
## ATmega169

## Advance Information

## Summary

Rev. **2514HS–AVR–05/03**

## Features (Continued)

- **Speed Grade:**
  - **0 - 1 MHz for ATmega169V**
  - **0 - 8 MHz for ATmega169L**
  - **0 - 16 MHz for ATmega169**
- **Ultra-Low Power Consumption**
  - **Active Mode:**
    - **1 MHz, 1.8V: 400µA**
    - **32 kHz, 1.8V: 20µA (including Oscillator)**
    - **32 kHz, 1.8V: 40µA (including Oscillator and LCD)**
  - **Power-down Mode:**
    - **0.5µA at 1.8V**

## Pin Configurations

**Figure 1.** Pinout ATmega169
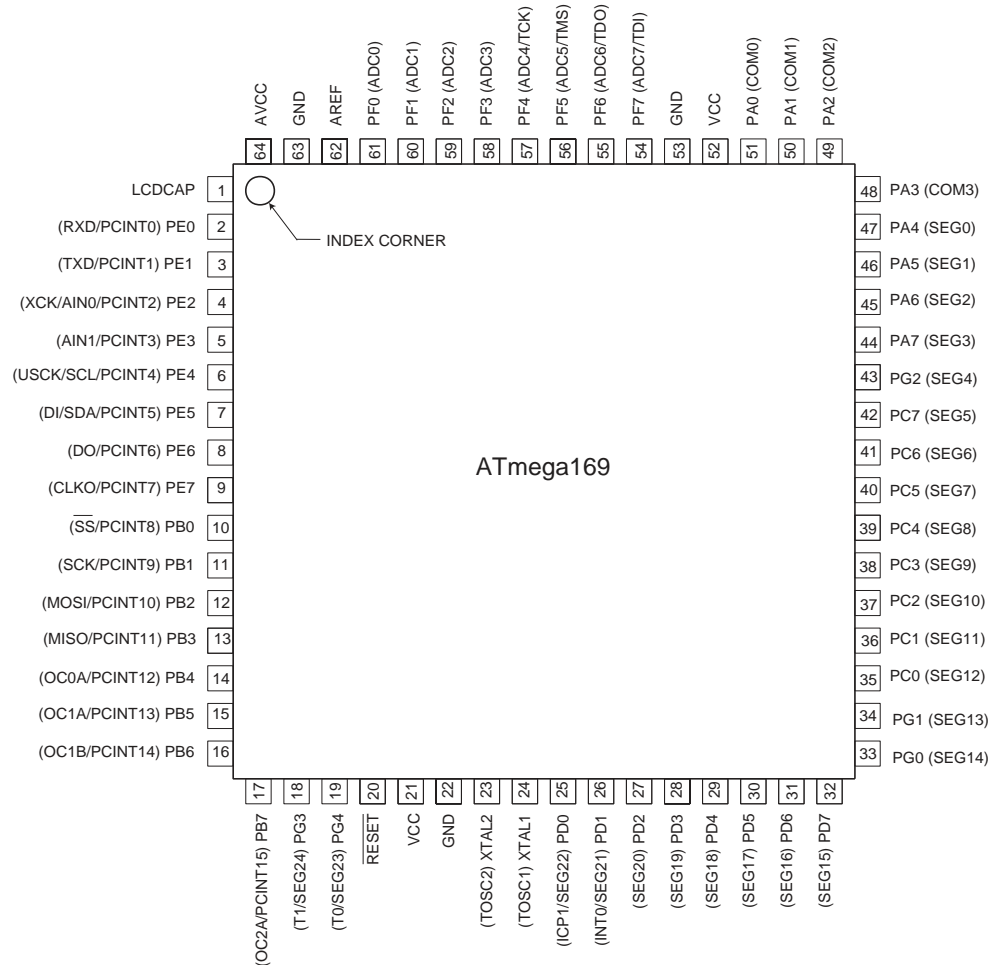


**Disclaimer**

Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

## Overview

The ATmega169 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega169 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## Block Diagram

**Figure 2.** Block Diagram
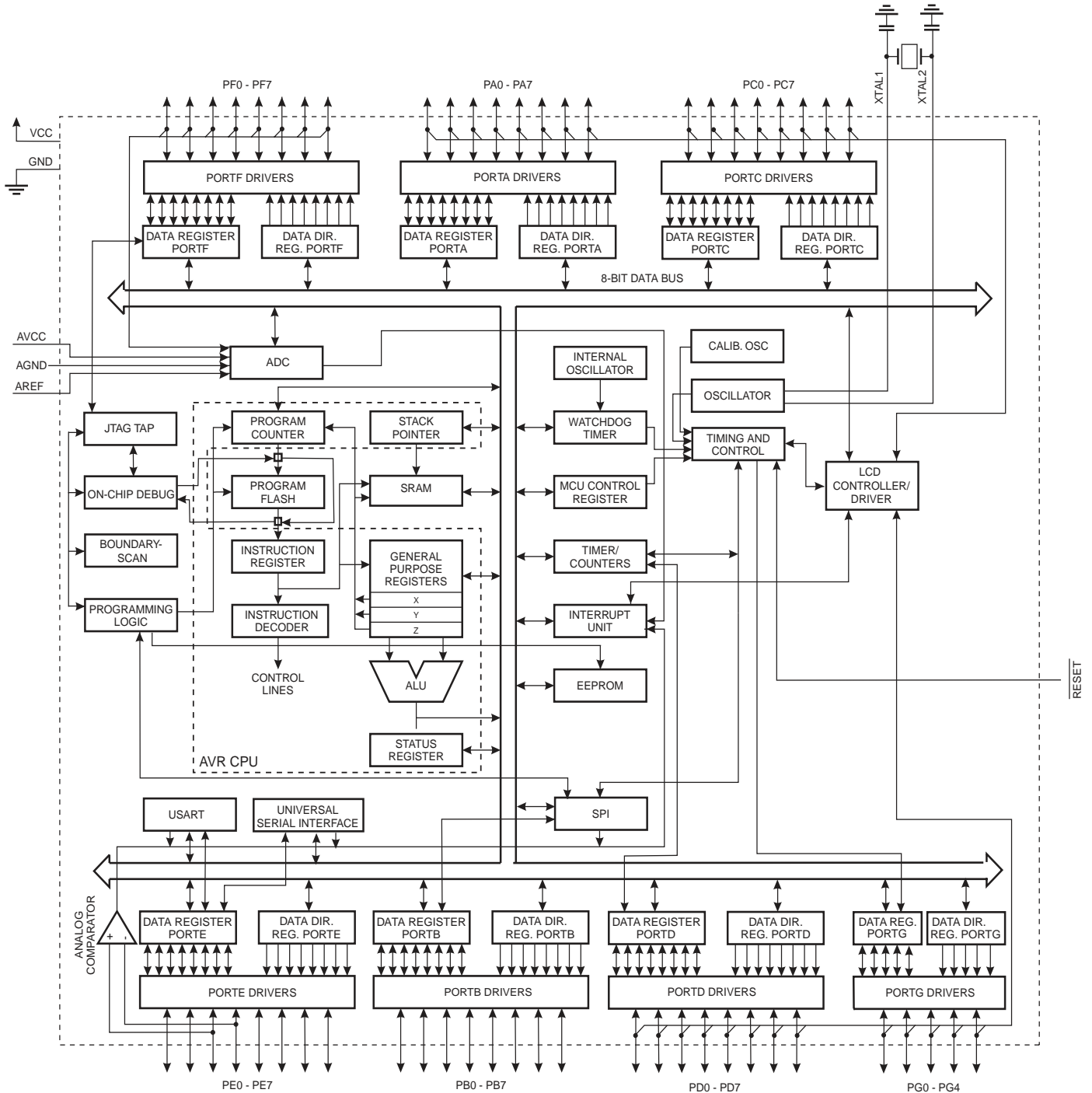
The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega169 provides the following features: 16K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 1K byte SRAM, 53 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, a complete On-chip LCD controller with internal step-up voltage, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, an 8-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer and the LCD controller continues to run, allowing the user to maintain a timer base and operate the LCD display while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer, LCD controller and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega169 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega169 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

## Pin Descriptions

**VCC**            Digital supply voltage.

**GND**            Ground.

**Port A (PA7..PA0)**    Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega169 as listed on page 59.

**Port B (PB7..PB0)**    Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the ATmega169 as listed on page 60.

**Port C (PC7..PC0)**    Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the ATmega169 as listed on page 63.

**Port D (PD7..PD0)**    Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega169 as listed on page 65.

**Port E (PE7..PE0)**    Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega169 as listed on page 67.

**Port F (PF7..PF0)**    Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output

buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

**Port G (PG4..PG0)**     Port G is a 5-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega169 as listed on page 67.

**RESET**     Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 16 on page 37. Shorter pulses are not guaranteed to generate a reset.

**XTAL1**     Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

**XTAL2**     Output from the inverting Oscillator amplifier.

**AVCC**     AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to $V_{CC}$, even if the ADC is not used. If the ADC is used, it should be connected to $V_{CC}$ through a low-pass filter.

**AREF**     This is the analog reference pin for the A/D Converter.

# About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

# Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| (0xFF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFE) | LCDDR18 | – | – | – | – | – | – | – | SEG324 | 224 |
| (0xFD) | LCDDR17 | SEG323 | SEG322 | SEG321 | SEG320 | SEG319 | SEG318 | SEG317 | SEG316 | 224 |
| (0xFC) | LCDDR16 | SEG315 | SEG314 | SEG313 | SEG312 | SEG311 | SEG310 | SEG309 | SEG308 | 224 |
| (0xFB) | LCDDR15 | SEG307 | SEG306 | SEG305 | SEG304 | SEG303 | SEG302 | SEG301 | SEG300 | 224 |
| (0xFA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF9) | LCDDR13 | – | – | – | – | – | – | – | SEG224 | 224 |
| (0xF8) | LCDDR12 | SEG223 | SEG222 | SEG221 | SEG220 | SEG219 | SEG218 | SEG217 | SEG216 | 224 |
| (0xF7) | LCDDR11 | SEG215 | SEG214 | SEG213 | SEG212 | SEG211 | SEG210 | SEG209 | SEG208 | 224 |
| (0xF6) | LCDDR10 | SEG207 | SEG206 | SEG205 | SEG204 | SEG203 | SEG202 | SEG201 | SEG200 | 224 |
| (0xF5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF4) | LCDDR8 | – | – | – | – | – | – | – | SEG124 | 224 |
| (0xF3) | LCDDR7 | SEG123 | SEG122 | SEG121 | SEG120 | SEG119 | SEG118 | SEG117 | SEG116 | 224 |
| (0xF2) | LCDDR6 | SEG115 | SEG114 | SEG113 | SEG112 | SEG111 | SEG110 | SEG109 | SEG108 | 224 |
| (0xF1) | LCDDR5 | SEG107 | SEG106 | SEG105 | SEG104 | SEG103 | SEG102 | SEG101 | SEG100 | 224 |
| (0xF0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEF) | LCDDR3 | – | – | – | – | – | – | – | SEG024 | 224 |
| (0xEE) | LCDDR2 | SEG023 | SEG022 | SEG021 | SEG020 | SEG019 | SEG018 | SEG017 | SEG016 | 224 |
| (0xED) | LCDDR1 | SEG015 | SEG014 | SEG013 | SEG012 | SEG011 | SEG010 | SEG09 | SEG008 | 224 |
| (0xEC) | LCDDR0 | SEG007 | SEG006 | SEG005 | SEG004 | SEG003 | SEG002 | SEG001 | SEG000 | 224 |
| (0xEB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE7) | LCDCCR | – | – | – | – | LCDCC3 | LCDCC2 | LCDCC1 | LCDCC0 | 224 |
| (0xE6) | LCDFRR | – | LCDPS2 | LCDPS1 | LCDPS0 | – | LCDCD2 | LCDCD1 | LCDCD0 | 222 |
| (0xE5) | LCDCRB | LCDCS | LCD2B | LCDMUX1 | LCDMUX0 | – | LCDPM2 | LCDPM1 | LCDPM0 | 220 |
| (0xE4) | LCDCRA | LCDEN | LCDAB | – | LCDIF | LCDIE | – | – | LCDBL | 220 |
| (0xE3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC6) | UDR | USART I/O Data Register | | | | | | | | 169 |
| (0xC5) | UBRRH | | | | | USART Baud Rate Register High | | | | 173 |
| (0xC4) | UBRRL | USART Baud Rate Register Low | | | | | | | | 173 |
| (0xC3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC2) | UCSRC | – | UMSEL | UPM1 | UPM0 | USBS | UCSZ1 | UCSZ0 | UCPOL | 169 |
| (0xC1) | UCSRB | RXCIE | TXCIE | UDRIE | RXEN | TXEN | UCSZ2 | RXB8 | TXB8 | 169 |
| (0xC0) | UCSRA | RXC | TXC | UDRE | FE | DOR | UPE | U2X | MPCM | 169 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| (0xBF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xBE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xBD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xBC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xBB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xBA) | USIDR | USI Data Register | | | | | | | | 184 |
| (0xB9) | USISR | USISIF | USIOIF | USIPF | USIDC | USICNT3 | USICNT2 | USICNT1 | USICNT0 | 185 |
| (0xB8) | USICR | USISIE | USIOIE | USIWM1 | USIWM0 | USICS1 | USICS0 | USICLK | USITC | 186 |
| (0xB7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB6) | ASSR | – | – | – | EXCLK | AS2 | TCN2UB | OCR2UB | TCR2UB | 138 |
| (0xB5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB3) | OCR2A | Timer/Counter2 Output Compare Register A | | | | | | | | 137 |
| (0xB2) | TCNT2 | Timer/Counter2 (8-bit) | | | | | | | | 137 |
| (0xB1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB0) | TCCR2A | FOC2A | WGM20 | COM2A1 | COM2A0 | WGM21 | CS22 | CS21 | CS20 | 135 |
| (0xAF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA0) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9F) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9E) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9C) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9B) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9A) | Reserved | – | – | – | – | – | – | – | – | |
| (0x99) | Reserved | – | – | – | – | – | – | – | – | |
| (0x98) | Reserved | – | – | – | – | – | – | – | – | |
| (0x97) | Reserved | – | – | – | – | – | – | – | – | |
| (0x96) | Reserved | – | – | – | – | – | – | – | – | |
| (0x95) | Reserved | – | – | – | – | – | – | – | – | |
| (0x94) | Reserved | – | – | – | – | – | – | – | – | |
| (0x93) | Reserved | – | – | – | – | – | – | – | – | |
| (0x92) | Reserved | – | – | – | – | – | – | – | – | |
| (0x91) | Reserved | – | – | – | – | – | – | – | – | |
| (0x90) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8F) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8E) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8C) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8B) | OCR1BH | Timer/Counter1 - Output Compare Register B High Byte | | | | | | | | 121 |
| (0x8A) | OCR1BL | Timer/Counter1 - Output Compare Register B Low Byte | | | | | | | | 121 |
| (0x89) | OCR1AH | Timer/Counter1 - Output Compare Register A High Byte | | | | | | | | 121 |
| (0x88) | OCR1AL | Timer/Counter1 - Output Compare Register A Low Byte | | | | | | | | 121 |
| (0x87) | ICR1H | Timer/Counter1 - Input Capture Register High Byte | | | | | | | | 122 |
| (0x86) | ICR1L | Timer/Counter1 - Input Capture Register Low Byte | | | | | | | | 122 |
| (0x85) | TCNT1H | Timer/Counter1 - Counter Register High Byte | | | | | | | | 121 |
| (0x84) | TCNT1L | Timer/Counter1 - Counter Register Low Byte | | | | | | | | 121 |
| (0x83) | Reserved | – | – | – | – | – | – | – | – | |
| (0x82) | TCCR1C | FOC1A | FOC1B | – | – | – | – | – | – | 120 |
| (0x81) | TCCR1B | ICNC1 | ICES1 | – | WGM13 | WGM12 | CS12 | CS11 | CS10 | 119 |
| (0x80) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | – | – | WGM11 | WGM10 | 117 |
| (0x7F) | DIDR1 | – | – | – | – | – | – | AIN1D | AIN0D | 191 |
| (0x7E) | DIDR0 | ADC7D | ADC6D | ADC5D | ADC4D | ADC3D | ADC2D | ADC1D | ADC0D | 209 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| (0x7D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x7C) | ADMUX | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | 205 |
| (0x7B) | ADCSRB | – | ACME | – | – | – | ADTS2 | ADTS1 | ADTS0 | 209 |
| (0x7A) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | 207 |
| (0x79) | ADCH | ADC Data Register High byte | | | | | | | | 208 |
| (0x78) | ADCL | ADC Data Register Low byte | | | | | | | | 208 |
| (0x77) | Reserved | – | – | – | – | – | – | – | – | |
| (0x76) | Reserved | – | – | – | – | – | – | – | – | |
| (0x75) | Reserved | – | – | – | – | – | – | – | – | |
| (0x74) | Reserved | – | – | – | – | – | – | – | – | |
| (0x73) | Reserved | – | – | – | – | – | – | – | – | |
| (0x72) | Reserved | – | – | – | – | – | – | – | – | |
| (0x71) | Reserved | – | – | – | – | – | – | – | – | |
| (0x70) | TIMSK2 | – | – | – | – | – | – | OCIE2A | TOIE2 | 140 |
| (0x6F) | TIMSK1 | – | – | ICIE1 | – | – | OCIE1B | OCIE1A | TOIE1 | 122 |
| (0x6E) | TIMSK0 | – | – | – | – | – | – | OCIE0A | TOIE0 | 92 |
| (0x6D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x6C) | PCMSK1 | PCINT15 | PCINT14 | PCINT13 | PCINT12 | PCINT11 | PCINT10 | PCINT9 | PCINT8 | 78 |
| (0x6B) | PCMSK0 | PCINT7 | PCINT6 | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | 78 |
| (0x6A) | Reserved | – | – | – | – | – | – | – | – | |
| (0x69) | EICRA | – | – | – | – | – | – | ISC01 | ISC00 | 76 |
| (0x68) | Reserved | – | – | – | – | – | – | – | – | |
| (0x67) | Reserved | – | – | – | – | – | – | – | – | |
| (0x66) | OSCCAL | Oscillator Calibration Register | | | | | | | | 28 |
| (0x65) | Reserved | – | – | – | – | – | – | – | – | |
| (0x64) | Reserved | – | – | – | – | – | – | – | – | |
| (0x63) | Reserved | – | – | – | – | – | – | – | – | |
| (0x62) | Reserved | – | – | – | – | – | – | – | – | |
| (0x61) | CLKPR | CLKPCE | – | – | – | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | 30 |
| (0x60) | WDTCR | – | – | – | WDCE | WDE | WDP2 | WDP1 | WDP0 | 43 |
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | 9 |
| 0x3E (0x5E) | SPH | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | 11 |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 11 |
| 0x3C (0x5C) | Reserved | | | | | | | | | |
| 0x3B (0x5B) | Reserved | | | | | | | | | |
| 0x3A (0x5A) | Reserved | | | | | | | | | |
| 0x39 (0x59) | Reserved | | | | | | | | | |
| 0x38 (0x58) | Reserved | | | | | | | | | |
| 0x37 (0x57) | SPMCSR | SPMIE | RWWSB | – | RWWSRE | BLBSET | PGWRT | PGERS | SPMEN | 257 |
| 0x36 (0x56) | Reserved | – | – | – | – | – | – | – | – | |
| 0x35 (0x55) | MCUCR | JTD | – | – | PUD | – | – | IVSEL | IVCE | 236 |
| 0x34 (0x54) | MCUSR | – | – | – | JTRF | WDRF | BORF | EXTRF | PORF | 236 |
| 0x33 (0x53) | SMCR | – | – | – | – | SM2 | SM1 | SM0 | SE | 32 |
| 0x32 (0x52) | Reserved | – | – | – | – | – | – | – | – | |
| 0x31 (0x51) | OCDR | IDRD/OCD | OCDR6 | OCDR5 | OCDR4 | OCDR3 | OCDR2 | OCDR1 | OCDR0 | 231 |
| 0x30 (0x50) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | 189 |
| 0x2F (0x4F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x2E (0x4E) | SPDR | SPI Data Register | | | | | | | | 149 |
| 0x2D (0x4D) | SPSR | SPIF | WCOL | – | – | – | – | – | SPI2X | 149 |
| 0x2C (0x4C) | SPCR | SPIE | SPE | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | 147 |
| 0x2B (0x4B) | GPIOR2 | General Purpose I/O Register 2 | | | | | | | | 22 |
| 0x2A (0x4A) | GPIOR1 | General Purpose I/O Register 1 | | | | | | | | 22 |
| 0x29 (0x49) | Reserved | – | – | – | – | – | – | – | – | |
| 0x28 (0x48) | Reserved | – | – | – | – | – | – | – | – | |
| 0x27 (0x47) | OCR0A | Timer/Counter0 Output Compare Register A | | | | | | | | 92 |
| 0x26 (0x46) | TCNT0 | Timer/Counter0 (8 Bit) | | | | | | | | 91 |
| 0x25 (0x45) | Reserved | – | – | – | – | – | – | – | – | |
| 0x24 (0x44) | TCCR0A | FOC0A | WGM00 | COM0A1 | COM0A0 | WGM01 | CS02 | CS01 | CS00 | 89 |
| 0x23 (0x43) | GTCCR | TSM | – | – | – | – | – | PSR2 | PSR10 | 94 |
| 0x22 (0x42) | EEARH | – | – | – | – | – | – | – | EEAR8 | 18 |
| 0x21 (0x41) | EEARL | EEPROM Address Register Low Byte | | | | | | | | 18 |
| 0x20 (0x40) | EEDR | EEPROM Data Register | | | | | | | | 18 |
| 0x1F (0x3F) | EECR | – | – | – | – | EERIE | EEMWE | EEWE | EERE | 18 |
| 0x1E (0x3E) | GPIOR0 | General Purpose I/O Register 0 | | | | | | | | 22 |
| 0x1D (0x3D) | EIMSK | PCIE1 | PCIE0 | – | – | – | – | – | INT0 | 77 |
| 0x1C (0x3C) | EIFR | PCIF1 | PCIF0 | – | – | – | – | – | INTF0 | 77 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1B (0x3B) | Reserved | – | – | – | – | – | – | – | – | |
| 0x1A (0x3A) | Reserved | – | – | – | – | – | – | – | – | |
| 0x19 (0x39) | Reserved | – | – | – | – | – | – | – | – | |
| 0x18 (0x38) | Reserved | – | – | – | – | – | – | – | – | |
| 0x17 (0x37) | TIFR2 | – | – | – | – | – | – | OCF2A | TOV2 | 141 |
| 0x16 (0x36) | TIFR1 | – | – | ICF1 | – | – | OCF1B | OCF1A | TOV1 | 123 |
| 0x15 (0x35) | TIFR0 | – | – | – | – | – | – | OCF0A | TOV0 | 92 |
| 0x14 (0x34) | PORTG | – | – | – | PORTG4 | PORTG3 | PORTG2 | PORTG1 | PORTG0 | 75 |
| 0x13 (0x33) | DDRG | – | – | – | DDG4 | DDG3 | DDG2 | DDG1 | DDG0 | 75 |
| 0x12 (0x32) | PING | – | – | PING5 | PING4 | PING3 | PING2 | PING1 | PING0 | 75 |
| 0x11 (0x31) | PORTF | PORTF7 | PORTF6 | PORTF5 | PORTF4 | PORTF3 | PORTF2 | PORTF1 | PORTF0 | 74 |
| 0x10 (0x30) | DDRF | DDF7 | DDF6 | DDF5 | DDF4 | DDF3 | DDF2 | DDF1 | DDF0 | 74 |
| 0x0F (0x2F) | PINF | PINF7 | PINF6 | PINF5 | PINF4 | PINF3 | PINF2 | PINF1 | PINF0 | 75 |
| 0x0E (0x2E) | PORTE | PORTE7 | PORTE6 | PORTE5 | PORTE4 | PORTE3 | PORTE2 | PORTE1 | PORTE0 | 74 |
| 0x0D (0x2D) | DDRE | DDE7 | DDE6 | DDE5 | DDE4 | DDE3 | DDE2 | DDE1 | DDE0 | 74 |
| 0x0C (0x2C) | PINE | PINE7 | PINE6 | PINE5 | PINE4 | PINE3 | PINE2 | PINE1 | PINE0 | 74 |
| 0x0B (0x2B) | PORTD | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | 74 |
| 0x0A (0x2A) | DDRD | DDD7 | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | 74 |
| 0x09 (0x29) | PIND | PIND7 | PIND6 | PIND5 | PIND4 | PIND3 | PIND2 | PIND1 | PIND0 | 74 |
| 0x08 (0x28) | PORTC | PORTC7 | PORTC6 | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | 73 |
| 0x07 (0x27) | DDRC | DDC7 | DDC6 | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | 73 |
| 0x06 (0x26) | PINC | PINC7 | PINC6 | PINC5 | PINC4 | PINC3 | PINC2 | PINC1 | PINC0 | 74 |
| 0x05 (0x25) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | 73 |
| 0x04 (0x24) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | 73 |
| 0x03 (0x23) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | 73 |
| 0x02 (0x22) | PORTA | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | 73 |
| 0x01 (0x21) | DDRA | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | 73 |
| 0x00 (0x20) | PINA | PINA7 | PINA6 | PINA5 | PINA4 | PINA3 | PINA2 | PINA1 | PINA0 | 73 |

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.

3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATmega169 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

# Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| **ARITHMETIC AND LOGIC INSTRUCTIONS** | | | | | |
| ADD | Rd, Rr | Add two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | Rdl,K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | Rdl,K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \cdot Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \cdot K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \text{ v } Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \text{ v } K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow 0xFF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow 0x00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | $Rd \leftarrow Rd \text{ v } K$ | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | $Rd \leftarrow Rd \cdot (0xFF - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \cdot Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow 0xFF$ | None | 1 |
| MUL | Rd, Rr | Multiply Unsigned | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| MULS | Rd, Rr | Multiply Signed | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| MULSU | Rd, Rr | Multiply Signed with Unsigned | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| FMUL | Rd, Rr | Fractional Multiply Unsigned | $R1:R0 \leftarrow (Rd \times Rr) << 1$ | Z,C | 2 |
| FMULS | Rd, Rr | Fractional Multiply Signed | $R1:R0 \leftarrow (Rd \times Rr) << 1$ | Z,C | 2 |
| FMULSU | Rd, Rr | Fractional Multiply Signed with Unsigned | $R1:R0 \leftarrow (Rd \times Rr) << 1$ | Z,C | 2 |
| **BRANCH INSTRUCTIONS** | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| JMP | k | Direct Jump | $PC \leftarrow k$ | None | 3 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| CALL | k | Direct Subroutine Call | $PC \leftarrow k$ | None | 4 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | $Rd - Rr$ | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | $Rd - Rr - C$ | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | $Rd - K$ | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if $(SREG(s) = 1)$ then $PC \leftarrow PC+k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if $(SREG(s) = 0)$ then $PC \leftarrow PC+k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if $(Z = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if $(Z = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if $(N = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if $(N = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if $(N \oplus V= 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if $(N \oplus V= 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if $(H = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if $(H = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if $(T = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if $(T = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if $(V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if $(V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| BRIE | k | Branch if Interrupt Enabled | if ( I = 1) then PC $\leftarrow$ PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if ( I = 0) then PC $\leftarrow$ PC + k + 1 | None | 1/2 |
| **BIT AND BIT-TEST INSTRUCTIONS** | | | | | |
| SBI | P,b | Set Bit in I/O Register | I/O(P,b) $\leftarrow$ 1 | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | I/O(P,b) $\leftarrow$ 0 | None | 2 |
| LSL | Rd | Logical Shift Left | Rd(n+1) $\leftarrow$ Rd(n), Rd(0) $\leftarrow$ 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) $\leftarrow$ Rd(n+1), Rd(7) $\leftarrow$ 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0)$\leftarrow$C,Rd(n+1)$\leftarrow$ Rd(n),C$\leftarrow$Rd(7) | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | Rd(7)$\leftarrow$C,Rd(n)$\leftarrow$ Rd(n+1),C$\leftarrow$Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) $\leftarrow$ Rd(n+1), n=0..6 | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | Rd(3..0)$\leftarrow$Rd(7..4),Rd(7..4)$\leftarrow$Rd(3..0) | None | 1 |
| BSET | s | Flag Set | SREG(s) $\leftarrow$ 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) $\leftarrow$ 0 | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | T $\leftarrow$ Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) $\leftarrow$ T | None | 1 |
| SEC | | Set Carry | C $\leftarrow$ 1 | C | 1 |
| CLC | | Clear Carry | C $\leftarrow$ 0 | C | 1 |
| SEN | | Set Negative Flag | N $\leftarrow$ 1 | N | 1 |
| CLN | | Clear Negative Flag | N $\leftarrow$ 0 | N | 1 |
| SEZ | | Set Zero Flag | Z $\leftarrow$ 1 | Z | 1 |
| CLZ | | Clear Zero Flag | Z $\leftarrow$ 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I $\leftarrow$ 1 | I | 1 |
| CLI | | Global Interrupt Disable | I $\leftarrow$ 0 | I | 1 |
| SES | | Set Signed Test Flag | S $\leftarrow$ 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S $\leftarrow$ 0 | S | 1 |
| SEV | | Set Twos Complement Overflow. | V $\leftarrow$ 1 | V | 1 |
| CLV | | Clear Twos Complement Overflow | V $\leftarrow$ 0 | V | 1 |
| SET | | Set T in SREG | T $\leftarrow$ 1 | T | 1 |
| CLT | | Clear T in SREG | T $\leftarrow$ 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H $\leftarrow$ 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H $\leftarrow$ 0 | H | 1 |
| **DATA TRANSFER INSTRUCTIONS** | | | | | |
| MOV | Rd, Rr | Move Between Registers | Rd $\leftarrow$ Rr | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | Rd+1:Rd $\leftarrow$ Rr+1:Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd $\leftarrow$ K | None | 1 |
| LD | Rd, X | Load Indirect | Rd $\leftarrow$ (X) | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | Rd $\leftarrow$ (X), X $\leftarrow$ X + 1 | None | 2 |
| LD | Rd, - X | Load Indirect and Pre-Dec. | X $\leftarrow$ X - 1, Rd $\leftarrow$ (X) | None | 2 |
| LD | Rd, Y | Load Indirect | Rd $\leftarrow$ (Y) | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | Rd $\leftarrow$ (Y), Y $\leftarrow$ Y + 1 | None | 2 |
| LD | Rd, - Y | Load Indirect and Pre-Dec. | Y $\leftarrow$ Y - 1, Rd $\leftarrow$ (Y) | None | 2 |
| LDD | Rd,Y+q | Load Indirect with Displacement | Rd $\leftarrow$ (Y + q) | None | 2 |
| LD | Rd, Z | Load Indirect | Rd $\leftarrow$ (Z) | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | Rd $\leftarrow$ (Z), Z $\leftarrow$ Z+1 | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | Z $\leftarrow$ Z - 1, Rd $\leftarrow$ (Z) | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | Rd $\leftarrow$ (Z + q) | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | Rd $\leftarrow$ (k) | None | 2 |
| ST | X, Rr | Store Indirect | (X) $\leftarrow$ Rr | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | (X) $\leftarrow$ Rr, X $\leftarrow$ X + 1 | None | 2 |
| ST | - X, Rr | Store Indirect and Pre-Dec. | X $\leftarrow$ X - 1, (X) $\leftarrow$ Rr | None | 2 |
| ST | Y, Rr | Store Indirect | (Y) $\leftarrow$ Rr | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | (Y) $\leftarrow$ Rr, Y $\leftarrow$ Y + 1 | None | 2 |
| ST | - Y, Rr | Store Indirect and Pre-Dec. | Y $\leftarrow$ Y - 1, (Y) $\leftarrow$ Rr | None | 2 |
| STD | Y+q,Rr | Store Indirect with Displacement | (Y + q) $\leftarrow$ Rr | None | 2 |
| ST | Z, Rr | Store Indirect | (Z) $\leftarrow$ Rr | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | (Z) $\leftarrow$ Rr, Z $\leftarrow$ Z + 1 | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | Z $\leftarrow$ Z - 1, (Z) $\leftarrow$ Rr | None | 2 |
| STD | Z+q,Rr | Store Indirect with Displacement | (Z + q) $\leftarrow$ Rr | None | 2 |
| STS | k, Rr | Store Direct to SRAM | (k) $\leftarrow$ Rr | None | 2 |
| LPM | | Load Program Memory | R0 $\leftarrow$ (Z) | None | 3 |
| LPM | Rd, Z | Load Program Memory | Rd $\leftarrow$ (Z) | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | Rd $\leftarrow$ (Z), Z $\leftarrow$ Z+1 | None | 3 |
| SPM | | Store Program Memory | (Z) $\leftarrow$ R1:R0 | None | - |
| IN | Rd, P | In Port | Rd $\leftarrow$ P | None | 1 |
| OUT | P, Rr | Out Port | P $\leftarrow$ Rr | None | 1 |
| PUSH | Rr | Push Register on Stack | STACK $\leftarrow$ Rr | None | 2 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| POP | Rd | Pop Register from Stack | Rd ← STACK | None | 2 |
| **MCU CONTROL INSTRUCTIONS** | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

## Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 1 | 1.8 - 5.5V | ATmega169V-1AI<br>ATmega169V-1MI | 64A<br>64M1 | Industrial<br>(-40°C to 85°C) |
| 8 | 2.7 - 5.5V | ATmega169L-8AI<br>ATmega169L-8MI | 64A<br>64M1 | Industrial<br>(-40°C to 85°C) |
| 16 | 4.5 - 5.5V | ATmega169-16AI<br>ATmega169-16MI | 64A<br>64M1 | Industrial<br>(-40°C to 85°C) |

Note:    This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

| Package Type | |
|---|---|
| **64A** | 64-Lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP) |
| **64M1** | 64-pad, 9 x 9 x 1.0 mm body, lead pitch 0.50 mm, Micro Lead Frame Package (MLF) |

# Packaging Information

## 64A



Notes: 1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------|------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 15.75 | 16.00 | 16.25 | |
| D1 | 13.90 | 14.00 | 14.10 | Note 2 |
| E | 15.75 | 16.00 | 16.25 | |
| E1 | 13.90 | 14.00 | 14.10 | Note 2 |
| B | 0.30 | – | 0.45 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.80 TYP | | | |

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| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| **/ATMEL** 2325 Orchard Parkway San Jose, CA 95131 | **64A,** 64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | 64A | B |

**64M1**
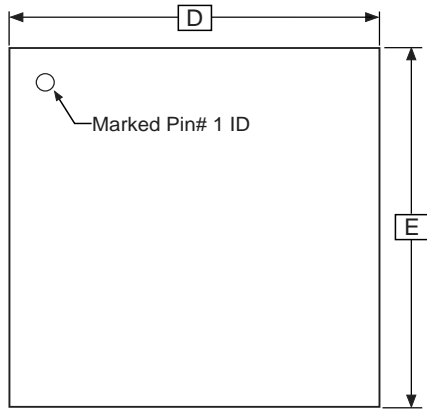


**TOP VIEW**

Marked Pin# 1 ID

D

E

**SIDE VIEW**

C SEATING PLANE

A1

A

△ 0.08 C

**BOTTOM VIEW**

L

D2

E2

b

e

Pin #1 Corner

1
2
3
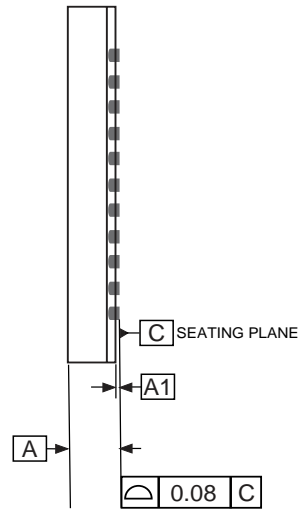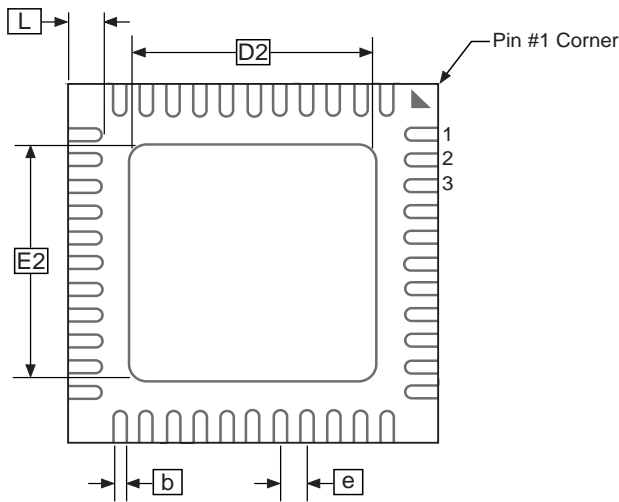
**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------|---------|------|------|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | – | 0.02 | 0.05 | |
| b | 0.23 | 0.25 | 0.28 | |
| D | | 9.00 BSC | | |
| D2 | 5.20 | 5.40 | 5.60 | |
| E | | 9.00 BSC | | |
| E2 | 5.20 | 5.40 | 5.60 | |
| e | | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.45 | |

Note: JEDEC Standard MO-220, Fig. 1, VMMD.

01/15/03

| ATMEL 2325 Orchard Parkway San Jose, CA 95131 | **TITLE** **64M1**, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm Micro Lead Frame Package (MLF) | **DRAWING NO.** 64M1 | **REV.** C |
|---|---|---|---|

# Errata

**ATmega169 Rev B**
- **Internal Oscillator Runs at 4 MHz**
- **LCD Contrast Voltage is not Correct**
- **External Oscillator is Non-functional**
- **USART**
- **ADC Measures with Lower Accuracy than Specified**
- **Serial Downloading**

## 6. Internal Oscillator Runs at 4 MHz

The Internal Oscillator runs at 4 MHz instead of the specified 8 MHz. Therefore, all Flash/EEPROM programming times are twice as long as specified. This includes Chip Erase, Byte programming, Page programming, Fuse programming, Lock bit programming, EEPROM write from the CPU, and Flash Self-Programming.

For this reason, rev-B samples are shipped with the CKDIV8 Fuse unprogrammed.

**Problem Fix/Workaround**

If 8 MHz operation is required, apply an external clock (this will be fixed in rev. C).

## 5. LCD Contrast Voltage is not Correct

The LCD contrast voltage between 1.8V and 3.1V is incorrect. When the $V_{CC}$ is between 1.8V and 3.1V, the LCD contrast voltage drops approx. 0.5V. The current consumption in this interval is higher than expected.

**Problem Fix/Workaround**

Contrast will be wrong, but display will still be readable, can be partly compensated for using the contrast control register (this will be fixed in rev. C).

## 4. External Oscillator is Non-functional

The external oscillator does not run with the setup described in the data sheet.

**Problem Fix/Workaround**

Use other clock source (this will be fixed in rev. C).

**Alternative Problem Fix/Workaround**

Adding a pull-down on XTAL1 will start the Oscillator.

## 3. USART

Writing TXEN to zero during transmission causes the transmission to suddenly stop. The data sheet description tells that the transmission should complete before stopping the USART when TXEN is written to zero.

**Problem Fix/Workaround**

Ensure that the transmission is complete before writing TXEN to zero (this will be fixed in rev. C).

## 2. ADC Measures with Lower Accuracy than Specified

The ADC does not work as intended. There is a positive offset in the result.

**Problem Fix/Workaround**

This will be fixed in rev. C.

1.  **Serial downloading**

    When entering Serial Programming mode the second byte will not echo back as described in the Serial Programming algorithm.

    **Problem Fix/Workaround**

    Check if the third byte echoes back to ensure that the device is in Programming mode (this will be fixed in rev. C).

**ATmega169 Rev C**
- **High Current Consumption In Power Down when JTAGEN is Programmed**
- **LCD Contrast Control**
- **Some Data Combinations Can Result in Dim Segments on the LCD**
- **LCD Current Consumption**

4.  **High Current Consumption In Power Down when JTAGEN is Programmed**

    The input buffer on TDO (PF6) is always enabled and the pull-up is always disabled when JTAG is programmed. This can leave the output floating.

    **Problem Fix/Workaround**

    Add external pull-up to PF6.

    Unprogram the JTAGEN Fuse before shipping out the end product.

3.  **LCD Contrast Control**

    The contrast control is not working properly when using synchronous clock (chip clock) to obtain an LCD clock, and the chip clock is 125 kHz or faster.

    **Problem Fix/Workaround**

    Use a low chip clock frequency (32 kHz) or apply an external voltage to the LCD-CAP pin.

2.  **Some Data Combinations Can Result in Dim Segments on the LCD**

    All segments connected to a common plane might be dimmed (lower contrast) when a certain combination of data is displayed.

    **Problem Fix/Workaround**

    Default waveform: If there are any unused segment pins, loading one of these with a 1 nF capacitor and always write '0' to this segment eliminates the problem.

    Low power waveform: Add a 1 nF capacitor to each common pin.

1.  **LCD Current Consumption**

    In an interval where $V_{CC}$ is within the range VLCD -0.2V to VLCD + 0.4V, the LCD current consumption is up to three times higher than expected. This will only be an issue in Power-save mode with the LCD running as the LCD current is negligible compared to the overall power consumption in all other modes of operation.

    **Problem Fix/Workaround**

    No known workaround.

## Data Sheet Change Log for ATmega169

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

**Changes from Rev. 2514A-08/02 to Rev. 2514B-09/02**

1. Canged the Endurance on the Flash to 10,000 Write/Erase Cycles.

**Changes from Rev. 2514B-09/02 to Rev. 2514C-11/02**

1. Added "Errata" on page 17.

2. Added Information for the 64-pad MLF Package in "Ordering Information" on page 14 and "Packaging Information" on page 15.

3. Changed Temerature Range and Removed Industrial Ordering Codes in "Packaging Information" on page 15.

**Changes from Rev. 2514C-11/02 to Rev. 2514D-01/03**

1. Added TCK frequency limit in "Programming via the JTAG Interface" on page 284.

2. Added Chip Erase as a first step in "Programming the Flash" on page 294 and "Programming the EEPROM" on page 295.

3. Added the section "Unconnected Pins" on page 56.

4. Added tips on how to disable the OCD system in "On-chip Debug System" on page 35.

5. Corrected interrupt addresses. ADC and ANA_COMP had swapped places.

6. Improved the table in "SPI Timing Characteristics" on page 299 and removed the table in "SPI Serial Programming Characteristics" on page 284.

7. Changed "will be ignored" to "must be written to zero" for unused Z-pointer bits in "Performing a Page Write" on page 260.

8. Corrected "LCD Frame Complete" to "LCD Start of Frame" in the LCDCRA Register description on page 220.

9. Changed OUT to STS and IN to LDS in USI code examples, and corrected $f_{SCKmax}$. The USI I/O Registers are in the extended I/O space, so IN and OUT cannot be used. LDS and STS take one more cycle when executed, so $f_{SCKmax}$ had to be changed accordingly.

10. Removed TOSKON and TOSCK from Table 103 on page 239, and g10 and g20 from Figure 114 on page 241 and Table 105 on page 242, because these signals do not exist in boundary scan.

11. Changed from 4 to 16 MIPS and MHz in the device Features list.

12. Corrected Port A to Port F in "AVCC" on page 6 under "Pin Descriptions" on page 5.

13. **Corrected 230.4 Mbps to 230.4 kbps in "Examples of Baud Rate Setting" on page 174.**

14. **Corrected placing of falling and rising XCK edges in Table 78, "UCPOL Bit Settings," on page 173.**

15. **Removed reference to Multipurpose Oscillator Application Note, which does not exist.**

16. **Corrected Number of Calibrated RC Oscillator Cycles in Table 1 on page 19 from 8,448 to 67,584.**

17. **Various minor Timer1 corrections.**

18. **Added information about PWM symmetry for Timer0 and Timer2.**

19. **Corrected the contents of DIDR0 and DIDR1.**

20. **Made all bit names in the LCDDR Registers unique by adding the COM number digit in front of the two digits already there, e.g. SEG304.**

21. **Changed Extended Standby to ADC Noise Reduction mode under "Asynchronous Operation of Timer/Counter2" on page 139.**

22. **Added note about Port B having better driving capabilities than the other ports. As a consequence the table, "DC Characteristics" on page 297 was corrected as well.**

23. **Added note under "Filling the Temporary Buffer (Page Loading)" on page 260 about writing to the EEPROM during an SPM page load.**

24. **Removed ADHSM completely.**

25. **Updated "Packaging Information" on page 15.**

**Changes from Rev. 2514D-01/03 to Rev. 2514E-02/03**

1. **Updated the section "Features" on page 1 with information regarding ATmega169 and ATmega169L.**

2. **Removed all references to the PG5 pin in Figure 1 on page 2, Figure 2 on page 3, "Port G (PG4..PG0)" on page 6, "Alternate Functions of Port G" on page 71, and "Register Description for I/O-Ports" on page 73.**

3. **Updated Table 118, "Extended Fuse Byte," on page 267.**

4. **Added Errata for "ATmega169 Rev C" on page 18, including "Significan Data Sheet Changes".**

5. **Updated the "Ordering Information" on page 14 to include the new speed grade for ATmega169L and the new 16 MHz ATmega169.**

**Changes from Rev.
2514E-02/03 to Rev.
2514F-04/03**

1. Renamed ICP to ICP1 in whole document.

2. Removed note on "Crystal Oscillator Operating Modes" on page 25.

3. XTAL1/XTAL2 can be used as timer oscillator pins, described in chapter "Calibrated Internal RC Oscillator" on page 27.

4. Switching between prescaler settings in "Switching Time" on page 31.

5. Updated DC and ACD Characteristics in chapter "Electrical Characteristics" on page 297 are updated. Removed TBDs from Table 16 on page 37, Table 19 on page 41, Table 133 on page 299.

6. Updated Figure 22 on page 52, Figure 25 on page 57 and Figure 109 on page 238 regarding WRITE PINx REGISTER.

7. Updated "Alternate Functions of Port F" on page 69 regarding JTAG.

8. Replaced Timer0 Overflow with Timer/Counter0 Compare Match in "Universal Serial Interface – USI" on page 178. Also updated "Start Condition Detector" on page 184 and "USI Control Register – USICR" on page 186.

9. Updated Features for "Analog to Digital Converter" on page 192 and Table 88 on page 205.

10. Added notes on Figure 117 on page 259 and Table 118 on page 267.

**Changes from Rev.
2514F-04/03 to Rev.
2514G-04/03**

1. Updated "ATmega169 Typical Characteristics – Preliminary Data" on page 303.

2. Updated typo in "Ordering Information" on page 14.

3. Updated Figure 45 on page 109, Table 18 on page 39, and Table 100 on page 233.

**Changes from Rev.
2514G-04/03 to Rev.
2514H-05/03**

1. Updated typo in Figure 145, Figure 165, and Figure 192.

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