

## SYNCHRONOUS-BUCK PWM CONTROLLER WITH NMOS LDO CONTROLLER

### FEATURES

- **Switching Mode Step-Down dc-to-dc Controller With Fast LDO Controller**
- **Input Voltage Range**  
     Switcher: 4.5 V to 28 V  
     LDO: 1.1 V to 3.6 V
- **Output Voltage Range**  
     Switcher: 0.9 V to 3.5 V  
     LDO: 0.9 V to 2.5 V
- **Synchronous for High Efficiency**
- **Precision  $V_{REF}$  ( $\pm 1\%$ )**
- **PWM Mode Control: Max. 500-kHz Operation**
- **High-Speed Error Amplifier**
- **Overcurrent Protection With Temperature Compensation Circuit**
- **Overvoltage and Undervoltage Protection**
- **Programmable Short-Circuit Protection**

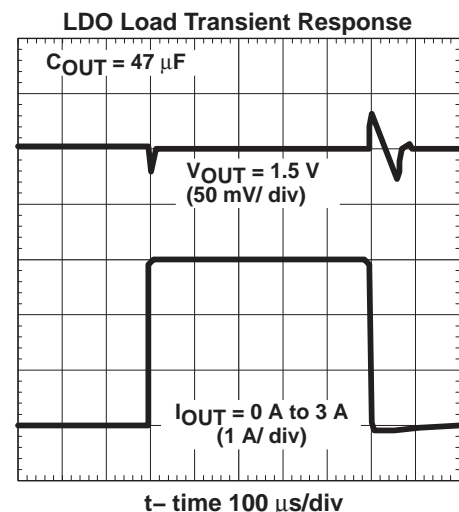
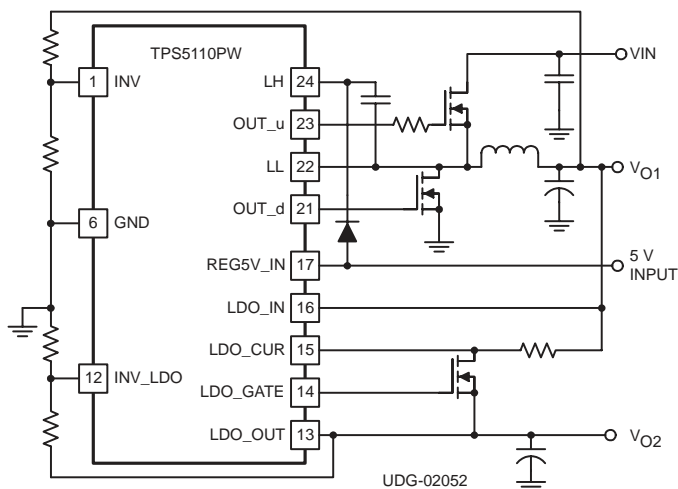
### APPLICATIONS

- **Notebook PCs, PDAs**
- **Consumer Game Systems**
- **DSP Application**

### DESCRIPTION

The TPS5110 provides one PWM-mode synchronous buck regulator controller (SBRC) and one low drop-out (LDO) regulator controller. The TPS5110 supports a low-voltage/high-current power supply for I/O and other peripherals in modern digital systems. The SBRC of the TPS5110 automatically adjusts from PWM mode to SKIP mode to maintain high efficiency under all load conditions. The LDO controller drives an external N-channel power MOSFET that realizes fast response and ultra-low dropout voltage. A unique overshoot protection circuit prevents a voltage hump at fast load decreasing transients. The current protection circuit for SBRC detects the drain-to-source voltage drop across the low-side and high-side power MOSFET while it is conducting. Also, the current protection circuit has a temperature coefficient to compensate for the  $R_{DS(on)}$  variation of the MOSFET. This resistor-less current protection simplifies the system design and reduces the external parts count. The LDO controller includes current-limit protection. Other features, such as undervoltage lockout, power good, overvoltage, undervoltage, and programmable short-circuit protection promote system reliability.

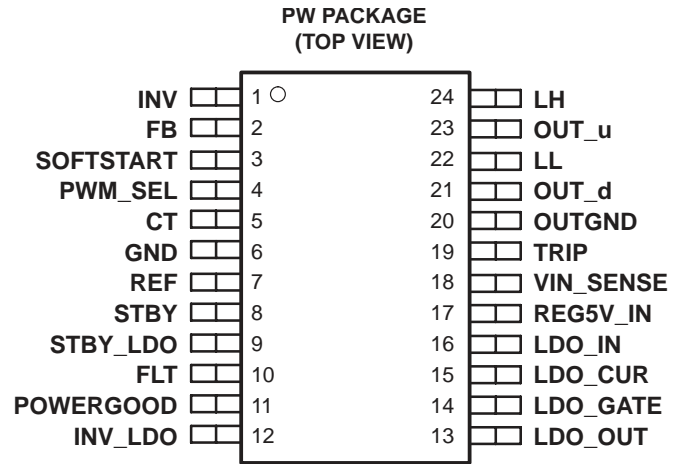
### SIMPLIFIED APPLICATION



## ORDERING INFORMATION

TA	PACKAGED DEVICES <sup>(1)</sup>
	PLASTIC TSSOP (PW)
-40°C to 85°C	TPS5110PW (24)

(1) The PW package is also available taped and reeled. Add an R suffix to the device type (i.e. TPS5110PWR)



**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

		TPS5110	UNIT
Input voltage range, V <sub>I</sub>	VIN_SENSE, STBY, STBY_LDO, TRIP, LL	-0.3 to 30	V
	INV, SOFTSTART, PWM_SEL, CT, FLT, INV_LDO, LDO_OUT, LDO_CUR, LDO_IN, REG5V_IN	-0.3 to 7	
	LH	-0.3 to 35	
Output voltage range, V <sub>O</sub>	REF	-0.3 to 3	V
	FB, POWERGOOD, OUT_d	-0.3 to 7	V
	LDO_GATE	-0.3 to 9	V
	OUT_u	-0.3 to 35	V
Continuous total power dissipation		See dissipation rating table	
Operating ambient temperature range, T <sub>A</sub>		-40 to 85	°C
Storage temperature range, T <sub>stg</sub>		-55 to 150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
Supply voltage	REG5V_IN	4.5		5.5	V
Supply voltage	LDO_IN	1.1		3.6	
Input voltage, V <sub>I</sub>	VIN_SENSE	4.5		28	
	INV, INV_LDO, CT, PWM_SEL, SOFTSTART, FLT	-0.1		6	
	POWERGOOD, FB, OUT_d	-0.1		5.5	
	LDO_CUR, LDO_OUT	-0.1		3.5	
	STBY, STBY_LDO, LL	-0.1		28	
	OUT_u, LH	-0.1		33	
	TRIP	-0.1		28	
	LDO_GATE	-0.1		8	
Oscillator frequency, f <sub>OSC</sub>			300	500	kHz
Operating free-air temperature, T <sub>A</sub>		-40		85	°C

**DISSIPATION RATINGS (THERMAL RESISTANCE = °C/W)**

PACKAGE(1)	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
24-PW	11.24 mW/°C	1404 mW	730 mW

(2) These devices are mounted on a JEDEC high-k board (2 oz. traces on surface, 2-layer 1-oz plane inside). (Assume the maximum junction temperature is 150°C)

**ELECTRICAL CHARACTERISTICS**

Over recommended free-air temperature range,  $V_{VIN\_SENSE} = 12\text{ V}$  and  $V_{REG5V\_IN} = 5\text{ V}$  (unless otherwise specified).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT SECTION</b>					
$I_{CC}$ Supply current	REG5V_IN current, $T_A = 25^\circ\text{C}$ , $V_{LDO\_IN} = 3.6\text{ V}$ , $V_{CT} = V_{INV} = V_{INV\_LDO} = V_{PWM\_SEL} = 0\text{ V}$		0.9	1.4	mA
$I_{CC(S)}$ Shutdown current	REG5V_IN current, $V_{STBY} = V_{STBY\_LDO} = 0\text{ V}$		0.001	10.00	$\mu\text{A}$
<b>UNDERVOLTAGE LOCKOUT SECTION</b>					
$V_{(TLH)}$ Low-to-high threshold voltage	REG5V_IN voltage	3.6		4.2	V
$V_{(TLL)}$ High-to-low threshold voltage	REG5V_IN voltage	3.5		4.1	
$V_{HYS}$ Hysteresis	REG5V_IN voltage	30		200	mV
<b>REFERENCE VOLTAGE SECTION</b>					
$V_{REF}$ Reference voltage			0.85		V
$V_{REF(tol)}$ Reference voltage tolerance	$T_A = 25^\circ\text{C}$ , $I_{REF} = 50\ \mu\text{A}$	-1%		1%	
	$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , $I_{REF} = 50\ \mu\text{A}$	-1.5%		1.5%	
	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , $I_{REF} = 50\ \mu\text{A}$	-2%		2%	
Reg(line) Line regulation	$I_{REF} = 50\ \mu\text{A}$ , $4.5\text{ V} \leq V_{(REG5V\_IN)} \leq 5.5\text{ V}$		0.05	5	mV
Reg(load) Load regulation	$0.1\ \mu\text{A} \leq I_{REF} \leq 1\text{ mA}$		0.15	5	mV
<b>CONTROL SECTION</b>					
$V_{IH}$ High-level input voltage	STBY, STBY_LDO, PWM_SEL	2.2			V
$V_{IL}$ Low-level input voltage	STBY, STBY_LDO, PWM_SEL			0.3	
<b>OUTPUT VOLTAGE MONITOR SECTION</b>					
OVP comparator threshold voltage	SBRC, LDO	0.91	0.95	0.99	V
UVP comparator threshold voltage	SBRC, LDO	0.51	0.55	0.59	
Powergood comparator 1, 4 threshold voltage		0.75	0.79	0.81	
Powergood comparator 2, 3 threshold voltage		0.88	0.91	0.94	
Powergood propagation delay from INV and INV_LDO to POWERGOOD	POWERGOOD high-to-low		1.2		$\mu\text{s}$
	POWERGOOD low-to-high		4		
Timer latch current source	UVP protection	-1.5	-2.3	-3.1	$\mu\text{A}$
	OVP protection	-80	-125	-180	
<b>OSCILLATOR SECTION</b>					
$f_{OSC}$ Oscillator frequency	PWM mode, $T_A = 25^\circ\text{C}$ $C_{CT} = 44\text{ pF}$		300		kHz
$V_{OH}$ CT high-level output voltage	dc	1.0	1.1	1.2	V
	$f_{OSC} = 300\text{ kHz}$		1.17		
$V_{OL}$ CT low-level output voltage	dc	0.4	0.5	0.6	
	$f_{OSC} = 300\text{ kHz}$		0.43		

**ELECTRICAL CHARACTERISTICS**

Over recommended free-air temperature range,  $V_{VIN\_SENSE} = 12\text{ V}$  and  $V_{REG5V\_IN} = 5\text{ V}$  (unless otherwise specified).

<b>SBRC ERROR AMPLIFIER SECTION</b>						
$V_{IO}$	Input offset voltage	$T_A = 25^\circ\text{C}$	2	10	mV	
	Open loop voltage gain		50		dB	
	Unity gain bandwidth		2.5		MHz	
$I_{SNK}$	Output sink current	$V_{FB} = 1\text{ V}$	0.2	0.7	mA	
$I_{SRC}$	Output source current	$V_{FB} = 1\text{ V}$	-0.2	-0.9		
<b>DUTY CONTROL SECTION</b>						
DUTY	Maximum duty control	$f_{OSC} = 300\text{ kHz}$ , $V_{INV} = 0\text{ V}$	82%			
<b>OUTPUT DRIVERS SECTION</b>						
	OUT_u sink current	$V_{OUT\_u} - V_{LL} = 3\text{ V}$	1.2		A	
	OUT_u source current	$V_{LH} - V_{OUT\_u} = 3\text{ V}$	-1.2			
	OUT_d sink current	$V_{OUT\_d} = 3\text{ V}$	1.5			
	OUT_d source current	$V_{OUT\_d} = 2\text{ V}$	-1.5			
	LDO_GATE sink current	$V_{LDO\_GATE} = 2\text{ V}$	1.5		mA	
	LDO_GATE source current	$V_{LDO\_GATE} = 2\text{ V}$	-1.4			
$I_{TRIP}$	TRIP current	$T_A = 25^\circ\text{C}$	11.5	13.0	14.5	$\mu\text{A}$
<b>SOFT-START SECTION</b>						
$I_{SOFT}$	Soft-start current		-1.6	-2.3	-2.9	$\mu\text{A}$
<b>LDO ERROR AMPLIFIER SECTION</b>						
$V_{IO}$	Input offset voltage	$T_A = 25^\circ\text{C}$ , $V_{LDO\_IN} = 3.3\text{ V}$	2	10	mV	
	Open loop voltage gain	$V_{LDO\_IN} = 3.3\text{ V}$	50		dB	
	Unity-gain bandwidth	$V_{LDO\_IN} = 3.3\text{ V}$ , $C_{LOAD} = 2000\text{ pF}$	1.4		MHz	
<b>LDO CURRENT LIMIT SECTION</b>						
	Current limit comparator threshold voltage	$V_{LDO\_IN} = 3.3\text{ V}$	40	50	60	mV
<b>LDO OVERTHROTTLE PROTECTION SECTION</b>						
	LDO_OUT sink current	$V_{LDO\_OUT} = V_{LDO\_GATE} = 1.5\text{ V}$	25		mA	

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CT	5	I/O	External capacitor from CT to GND adjusts frequency of the triangle oscillator.
FB	2	O	Feedback output of error amplifier
FLT	10	I/O	Fault latch timer pin. An external capacitor is connected between FLT and GND to set the FLT enable time up.
GND	6	–	Signal GND
INV	1	I	Inverting input of the SBRC error amplifier, skip comparator, OVP/UVP comparators and POWERGOOD comparator
INV_LDO	12	I	Inverting input of the LDO regulator, OVP/UVP comparators and POWERGOOD comparator
LDO_CUR	15	I	Current sense input of the LDO regulator.
LDO_GATE	14	O	Gate control output of an external MOSFET for LDO
LDO_OUT	13	I/O	LDO regulator's output connection. If output voltage causes an over shoot at output current changes high to low quickly, it pulls out electrical charge from this pin.
LDO_IN	16	I	Input of LDO regulator and current sense input of LDO regulator
LH	24	I/O	Bootstrap capacitor connection for high-side gate driver
LL	22	I/O	High side gate driving return. Connect this pin to the junction of the high side and low side MOSFET(s) for floating drive configuration. This pin also is an input terminal for current comparator.
OUT_d	21	O	Gate drive output for low-side MOSFET(s)
OUT_u	23	O	Gate drive output for high-side MOSFET(s).
OUTGND	20	–	Ground for FET drivers. It is connected to the current limiting comparator's negative input.
POWERGOOD	11	O	Power good open-drain output. PG comparators monitor both SBRC's and LDO's over voltage and under voltage. The threshold is $\pm 7\%$ . When either output is beyond this condition, POWERGOOD output goes low. When STBY or STBY_LDO goes high, the POWERGOOD pin's output starts with high. POWERGOOD also monitors REG5V_IN's UVLO output.
PWM_SEL	4	I	PWM or auto PWM/SKIP modes select. H: auto PWM/SKIP L: PWM fixed
REF	7	O	0.85-V reference voltage output. This 0.85-V reference voltage is used for setting the output voltage and the voltage protections. This reference voltage is regulated from REG5V_IN power supply.
REG5V_IN	17	I	External 5-V input. This input is a supply voltage for internal circuits.
SOFTSTART	3	I/O	External capacitor between SOFTSTART and GND sets SBRC soft-start time.
STBY	8	I	Standby control input for SBRC. SBRC can be switched into standby mode by grounding the STBY pin.
STBY_LDO	9	I	Standby control input for LDO regulator. LDO regulator can be switched into standby mode by grounding the STBY_LDO pin.
TRIP	19	I	External resistor connection for SBRC's output current protection control.
VIN_SENSE	18	I	SBRC supply voltage monitor. Input range is 4.5 V to 28 V. This pin is for reference of current limit.

FUNCTIONAL BLOCK DIAGRAM

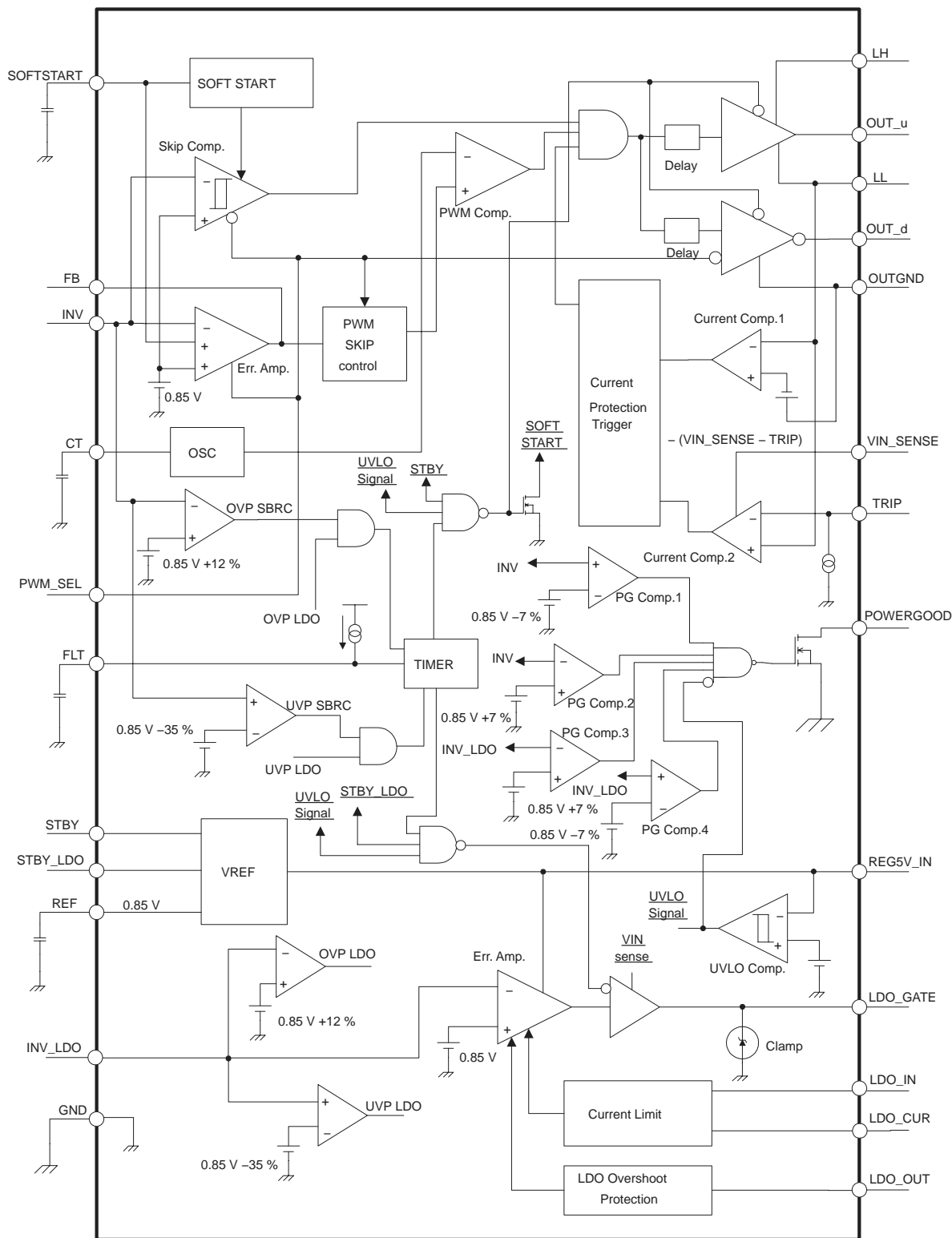


Figure 1. Block Diagram

## DETAILED DESCRIPTION

### PWM operation

The SBRC block has a high-speed error amplifier to regulate the output voltage of the synchronous buck converter. The output voltage of the SBRC is fed back to the inverting input (INV) of the error amplifier. The noninverting input is internally connected to a 0.85 V precise band gap reference circuit. The unity-gain bandwidth of the amplifier is 2.5 MHz. This decreases the amplifier delay during fast-load transients and contributes to a fast response. Loop gain and phase compensation is programmable by an external C, R network between the FB and INV pins. The output signal of the error amplifier is compared with a triangular wave to achieve the PWM control signal. The oscillation frequency of this triangular wave sets the switching frequency of the SBRC and is determined by the capacitor connected between the CT and GND pins. The PWM mode is used for the entire load range if the PWM\_SEL pin is set LOW, or used in high-output current condition if auto PWM/SKIP mode is selected by setting the same pin to HIGH.

### SKIP mode operation

The PWM\_SEL pin selects either the auto PWM/SKIP mode or fixed PWM mode. If this pin is lower than 0.3 V, the SBRC operates in the fixed PWM mode. If 2.5 V (min.) or higher is applied, it operates in auto PWM/SKIP mode. In the auto PWM/SKIP mode, the operation changes from constant frequency PWM mode to an energy-saving SKIP mode automatically in accordance with load conditions. Using a MOSFET with ultra-low  $R_{DS(on)}$  if the auto SKIP function is implemented is not recommended. The SBRC block has a hysteretic comparator to regulate the output voltage of the synchronous buck converter during SKIP mode. The delay from the comparator input to the driver output is typically 1.2  $\mu$ s. In the SKIP mode, the frequency varies with load current and input voltage.

### high-side driver

The high-side driver is designed to drive high current and low  $R_{DS(on)}$  N-channel MOSFET(s). The current rating of the driver is 1.2 A at source and sink. When configured as a floating driver a 5-V bias voltage is delivered from external REG5V\_IN supply. The instantaneous-drive current is supplied by the flying capacitor between the LH and LL pins since a 5-V power supply does not usually have low impedance. It is recommended to add a 5- $\Omega$  to 10- $\Omega$  resistor between the gate of the high-side MOSFET(s) and the OUT\_u pin to suppress noise. The maximum voltage that can be applied between the LH and OUTGND pins is 33 V. When selecting the high-current rating MOSFET(s), it is important to pay attention to both gate-drive power dissipation and the rise/fall time against the dead-time between high-side and low-side drivers. The gate-drive power is dissipated from the controller device and it is proportional to the gate charge at  $V_{gs} = 5$  V, PWM switching frequency and the numbers of all MOSFETs used for low-side and high-side switches. This gate drive loss should not exceed the maximum power dissipation of the device.

### low-side driver

The low-side driver is designed to drive high-current and low  $R_{DS(on)}$  N-channel MOSFET(s). The maximum drive voltage is 5 V from REG5V\_IN pin. The current rating of the driver is typically 1.5 A at source and sink. Gate resistance is not necessary for the low-side MOSFET for switching noise suppression since it turns on after the parallel diode is turned on (ZVS). It needs the same dissipation consideration when using high-current rating MOSFET(s). Another issue that needs precaution is the gate threshold voltage. Even though the OUT\_d pin is shorted to the OUTGND pin with low resistance when the low-side MOSFET(s) is OFF, high  $dv/dt$  at the LL pin during turnon of the high side arm generates voltage peak at the OUT\_d pin through the drain to gate capacitance,  $C_{dg}$ , of the low-side MOSFET(s). To prevent a short period shoot-through during this switching event, the application designer should select MOSFET(s) with adequate threshold voltage.



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## DETAILED DESCRIPTION

### dead time

The internally defined dead-time prevents shoot-through current flowing through the main power MOSFETs during switching transitions. Typical value of the dead-time is 100 ns.

### standby

The SBRC and the LDO controller can be switched into standby mode separately by grounding the STBY pin and/or SYBY\_LDO pins. The standby-mode current, when both controllers are off, can be as low as 1 nA.

**Table 1. Standby Logic ( $V_{REG5V\_IN} > 4\text{ V}$ )†**

STBY	STBY_LDO	SBRC	LDO	POWERGOOD
L	L	OFF	OFF	OFF
L	H	OFF	ON	OFF
H	L	ON	OFF	OFF
H	H	ON	ON	ON

### soft start

Soft-start ramp up of the SBRC is controlled by the SOFTSTART pin voltage. After the STBY pin is raised to a HIGH level, an internal current source charges up an external capacitor connected between the SOFTSTART and GND pins. The output voltage ramps up as the SOFTSTART pin voltage increases from 0 V to 0.85 V. The soft-start time is easily calculated by the supply current and the capacitance value (see application information). The soft-start timing circuit for the LDO is integrated into the device. The soft-start time is fixed and can be as short as 600  $\mu\text{s}$ . This is observed when the LDO is turned on separately from the SBRC. Simultaneous start up of the two outputs is also possible. Tie the LDO input to the SBRC's output and let both STBY\_LDO and STBY voltages rise to the HIGH level simultaneously, then the LDO's output follows the ramp of the SBRC's output.

### over current protection

Over current protection (OCP) is achieved by comparing the drain-to-source voltage of the high-side and low-side MOSFET to a set-point voltage, which is defined by both the internal current source,  $I_{TRIP}$ , and the external resistor connected between the VIN\_SENSE and TRIP pins.  $I_{TRIP}$  has a typical value of 13  $\mu\text{A}$  at 25°C. When the drain-to-source voltage exceeds the set-point voltage during low-side conduction, the high-side current comparator becomes active, and the low-side pulse is extended until this voltage comes back below the threshold. If the set-point voltage is exceeded during high-side conduction in the following cycle, the current-limit circuit terminates the high-side driver pulse. Together this action has the effect of decreasing the output voltage until the under voltage protection circuit is activated to latch both the high-side and low-side drivers OFF. In the TPS5110, trip current  $I_{TRIP}$  also has a temperature coefficient of 3400 ppm/°C in order to compensate for temperature drift of the MOSFET on-resistance.

**DETAILED DESCRIPTION**

**OCP for the LDO**

To achieve the LDO current limit, a sense resistor must be placed in series with the N-channel MOSFET drain, connected between the LDO\_IN and LDO\_CUR pins (see reference schematic). If the voltage drop across this sense resistor exceeds 50 mV, the output voltage is reduced to approximately 22% of the nominal value, thus activates UVP to start the FLT latch timer. When the time is up, the LDO\_GATE pin is pulled LOW to makes the LDO regulator shutdown. Note that the SBRC is also latched OFF at the same time since the LDO and the SBRC share the same FLT capacitor.

**overvoltage protection**

For over voltage protection (OVP), the TPS5110 monitors the INV and INV\_LDO pin voltages. When the INV or INV\_LDO pin voltage is higher than 0.95 V (0.85 V +12%), the OVP comparator output goes low and the FLT timer starts to charge an external capacitor connected to FLT pin. After a set time, the FLT circuit latches the high-side and low-side MOSFET drivers and the LDO. The latched state of each block is summarized in Table 2. The timer-source current for the OVP latch is 125 μA(typ.), and the time-up voltage is 1.185 V (typ.). The OVP timer is designed to be 50 times faster than the undervoltage protection timer described below.

**Table 2. Overvoltage Protection Logic**

OVP OCCURS AT	HIGH-SIDE MOSFET DRIVER	LOW-SIDE MOSFET DRIVER	LDO
SBRC	OFF	ON	OFF
LDO	OFF	OFF	OFF

**undervoltage protection**

For under voltage protection (UVP), the TPS5110 monitors the INV and INV\_LDO pin voltages. When the INV or INV\_LDO pin voltage is lower than 0.55 V (0.85 V – 35 %), the UVP comparator output goes low, and the FLT timer starts to charge the external capacitor connected to FLT pin. Also, when the current comparator triggers the OCP, the UVP comparator detects the under-voltage output and starts the FLT capacitor charge, too. After a set time, the FLT circuit latches all of the MOSFET drivers to the OFF state. The timer-latch source current for UVP is 2.3 μA (typ.), and the time-up voltage is also 1.185 V (typ.). The UVP function of the LDO controller is disabled when voltage across the pass transistor is less than 0.23 V (typ.).

**FLT**

When an OVP or UVP comparator output goes low, the FLT circuit starts to charge the FLT capacitor. If the FLT pin voltage goes beyond a constant level, the TPS5110 latches the MOSFET drivers. At this time, the state of MOSFET is different depending on the OVP alert and the UVP alert, see Table 2. The enable time used to latch the MOSFET drivers is decided by the value of the FLT capacitor. The charging constant current value depends on whether it is an OVP alert or a UVP alert as shown in the following equation:

$$FLT_{source\ current\ (OVP)} = FLT_{source\ current\ (UVP)} \times 50$$

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## DETAILED DESCRIPTION

### undervoltage lockout (UVLO)

When the REG5V\_IN voltage decreases below about 4 V, the output stages of both the SBRC and the LDO are turned off. This state is not latched and the operation recovers immediately after the input voltage becomes higher than the turn-on value again. The typical hysteresis voltage is 100 mV.

### UVLO for LDO

The LDO\_IN voltage is monitored with a hysteretic comparator. When this voltage is less than 1 V, the UVLO circuit disables the UVP/OVP comparators that monitor the INV\_LDO voltage. In case the SBRC over current protection is activated prior to that of the LDO's, this protection function may also be observed.

### LDO control

The LDO controller can drive an external N-channel MOSFET. This realizes a fast response as well as an ultra-low dropout voltage regulator. For example, it is easy to configure both a 1.8-V and a 1.5-V high-current power supply for core and I/O of modern digital processors, one from the SBRC and the other from the LDO. The LDO\_IN voltage range is from 1.1 V to 3.6 V, and the output voltage is adjustable from 0.9 V to 2.5 V by an external resistor divider. Gain and phase of the high-speed error amplifier for this LDO control is internally compensated and is connected to the 0.85-V band-gap reference circuit. The gate driver buffer is supplied by VIN\_SENSE voltage. In the relatively high-output voltage applications, make sure that output voltage plus threshold voltage of the pass transistor is less than the minimum VIN. More precisely,

$$V_{VIN\_SENSE} - 0.7\text{ V} \geq V_{THN} + V_{LDO\_OUT}$$

where  $V_{THN}$  is the threshold voltage of N-channel MOSFET.

The LDO controller is also equipped with OVP, UVP, over current limit and overshoot protection functions.

### overshoot protection – LDO

In the event that load current changes from high to low very quickly, the LDO regulator output voltage may start to overshoot. In order to resist this phenomenon, the LDO controller has an overshoot protection function. If the LDO regulator output overshoots, the controller draws electrical charge out from LDO\_OUT pin to hold it stable.

DETAILED DESCRIPTION

powergood

A single powergood circuit monitors the SBRC output voltage, LDO output voltage and REF5V\_IN voltage. The POWERGOOD pin is an open-drain output. When INV or INV\_LDO voltage go beyond +/- 7% of 0.85 V or the REG5V\_IN voltage is lower than 4 V, the POWERGOOD pin is pulled down to the LOW level. POWERGOOD propagation delay is minimal, 1 μs to 4 μs.

Table 3. Powergood Logic†

STBY	STBY_LDO	$0.79\text{ V} \leq V_{INV} \leq 0.91\text{ V}$	$0.79\text{ V} \leq V_{INV\_LDO} \leq 0.91\text{ V}$	$V_{REG5V\_IN} > 4\text{ V}$	POWER GOOD
L	L	X	X	X	L
H	L	X	X	X	L
L	H	X	X	X	L
H	H	FALSE	X	X	L
H	H	X	FALSE	X	L
H	H	X	X	FALSE‡	L
H	H	TRUE	TRUE	TRUE	H

† X = True OR False

‡ The logic circuit is under normal operation

TYPICAL CHARACTERISTICS

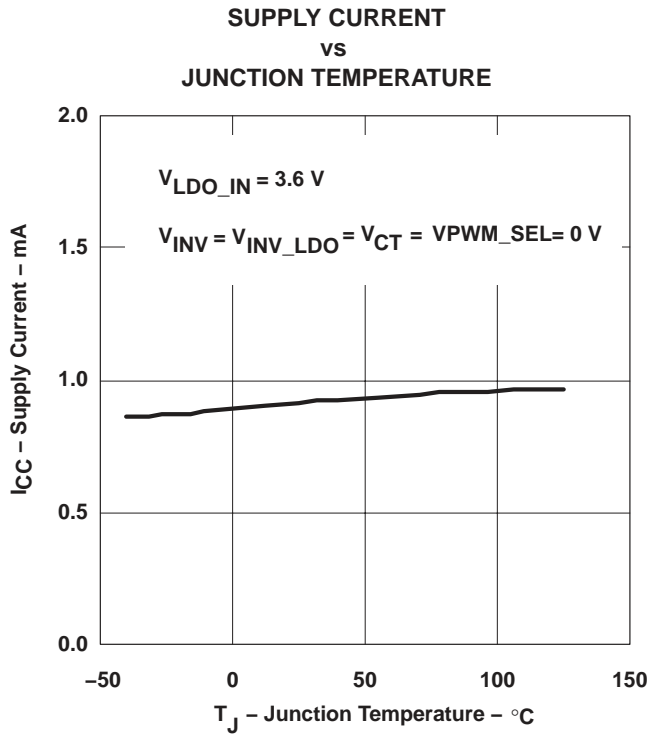


Figure 2

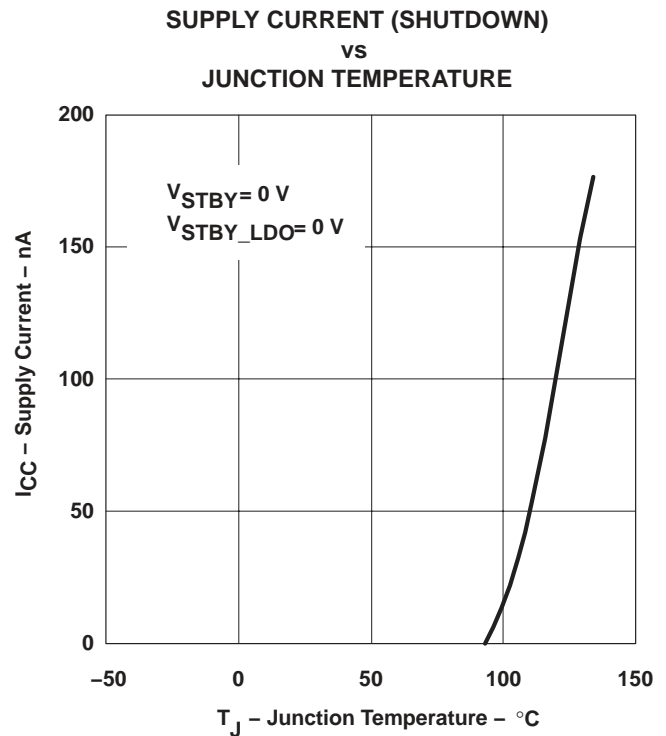


Figure 3

NOTE:  $V_{VIN\_SENSE} = 12\text{ V}$ ,  $V_{REG5V\_IN} = 5\text{ V}$  unless otherwise noted.

TYPICAL CHARACTERISTICS

FLT (OVP) SOURCE CURRENT  
vs  
JUNCTION TEMPERATURE

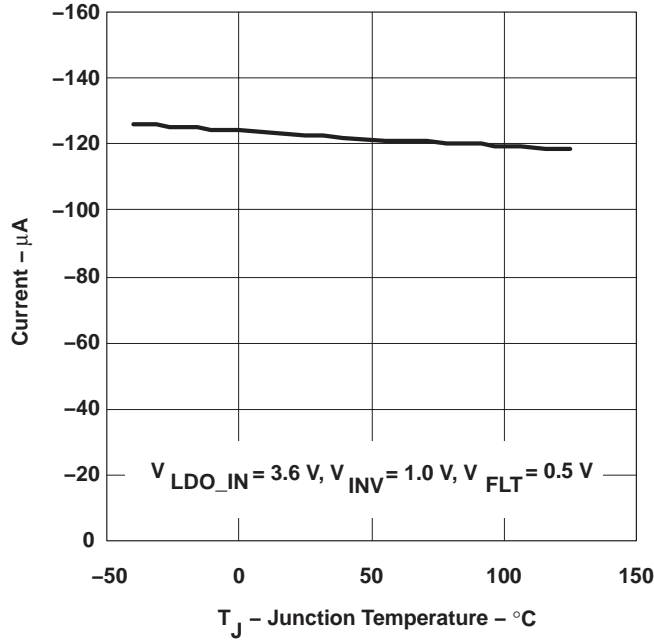


Figure 4

FLT (UVP) SOURCE CURRENT  
vs  
JUNCTION TEMPERATURE

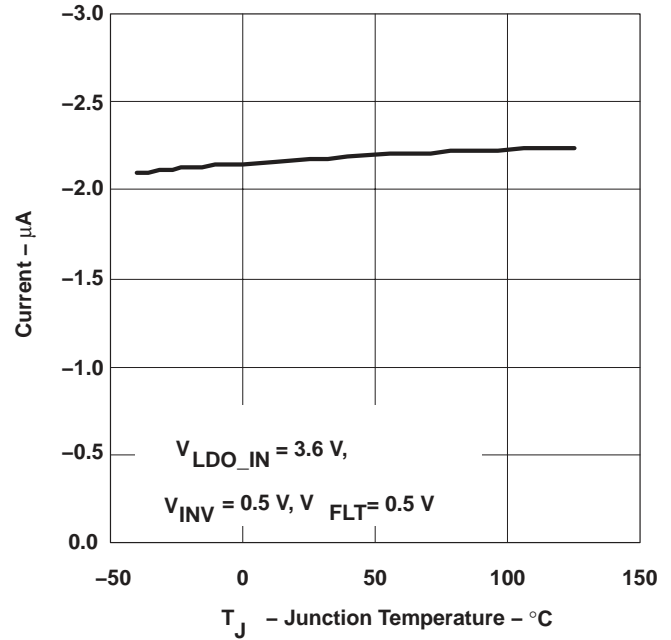


Figure 5

TRIP CURRENT  
vs  
JUNCTION TEMPERATURE

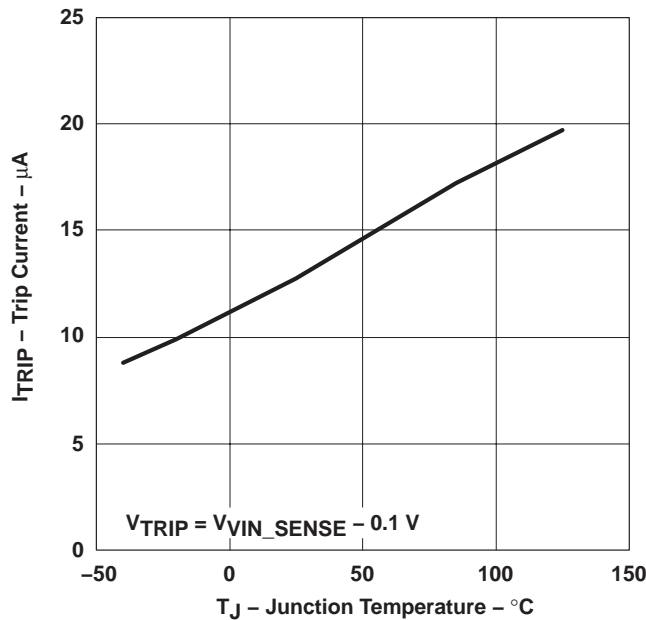


Figure 6

LDO\_GATE SINK CURRENT  
vs  
OUTPUT VOLTAGE

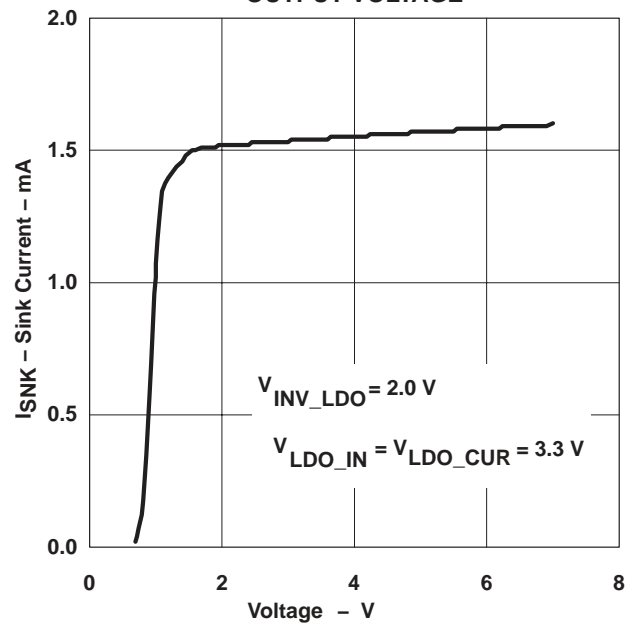


Figure 7

NOTE: VIN\_SENSE = 12 V, VREG5V\_IN = 5 V unless otherwise noted.

TYPICAL CHARACTERISTICS

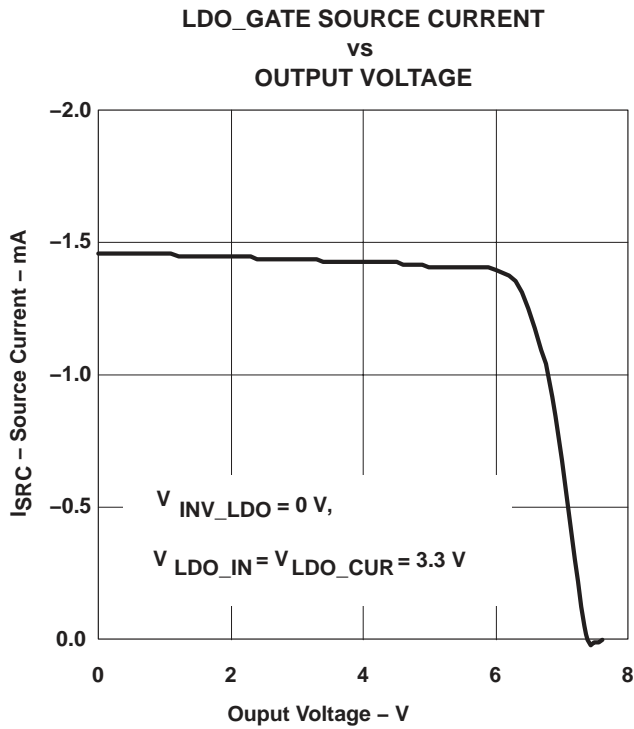


Figure 8

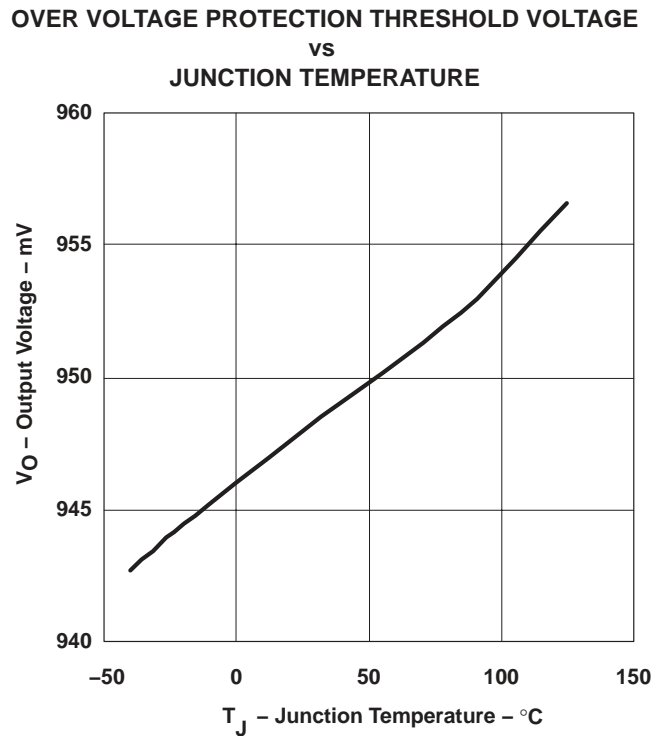


Figure 9

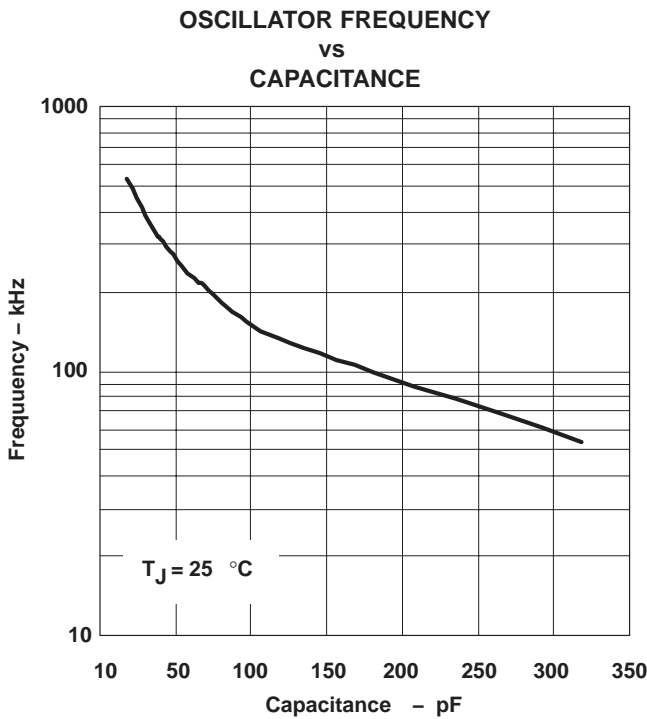


Figure 10

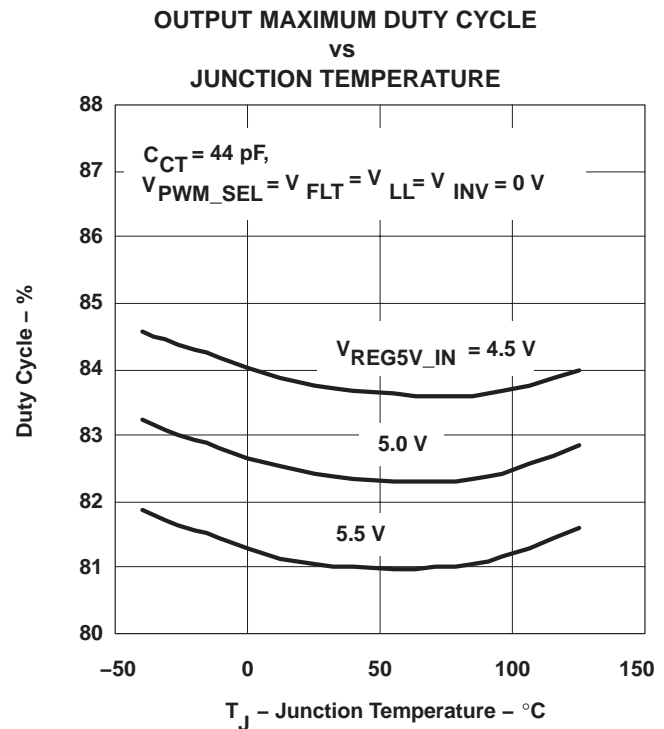


Figure 11

NOTE:  $V_{VIN\_SENSE} = 12\text{ V}$ ,  $V_{REG5V\_IN} = 5\text{ V}$  unless otherwise noted.

TYPICAL CHARACTERISTICS

FLT DELAY TIME (OVP)  
vs  
CAPACITANCE

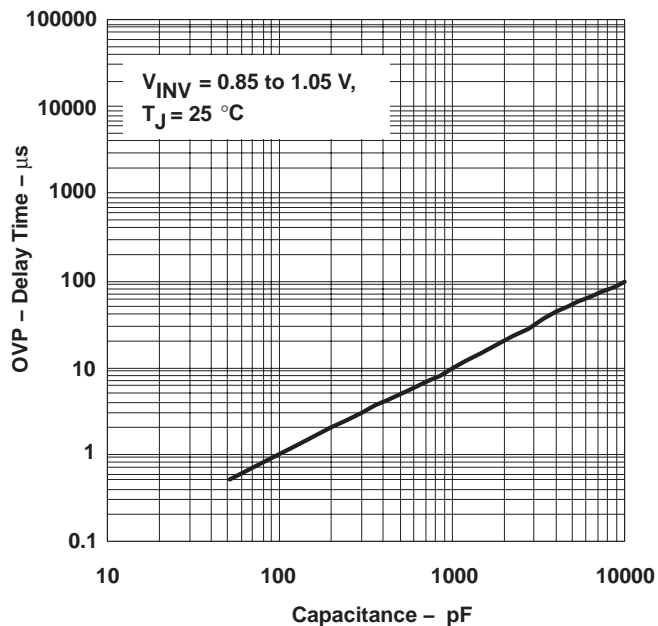


Figure 12

FLT DELAY TIME (UVP)  
vs  
CAPACITANCE

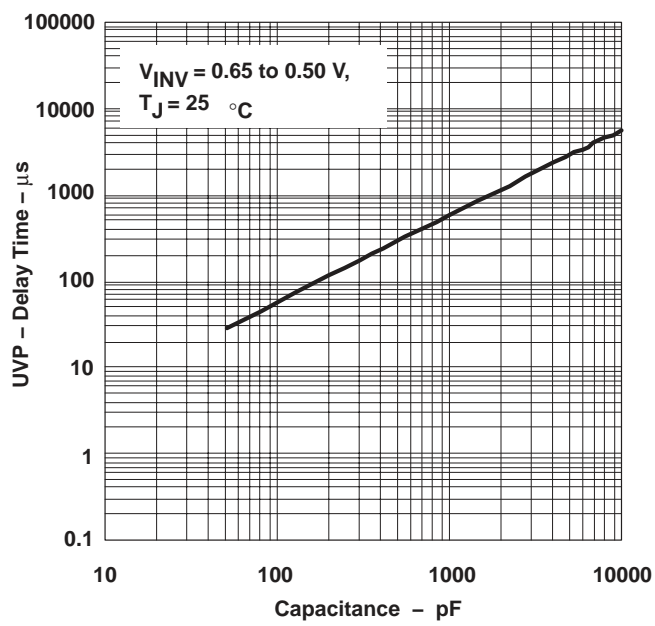


Figure 13

SOFT-START TIME  
vs  
CAPACITANCE

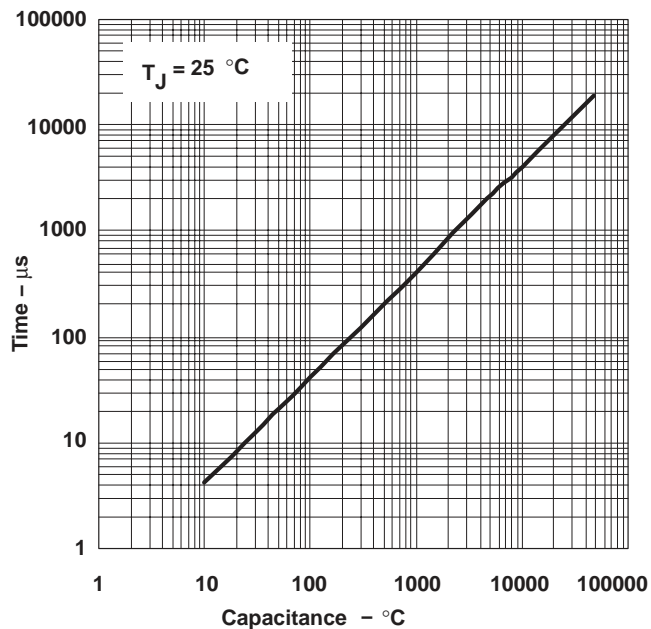


Figure 14

LDO CURRENT LIMIT THRESHOLD VOLTAGE  
vs  
JUNCTION TEMPERATURE

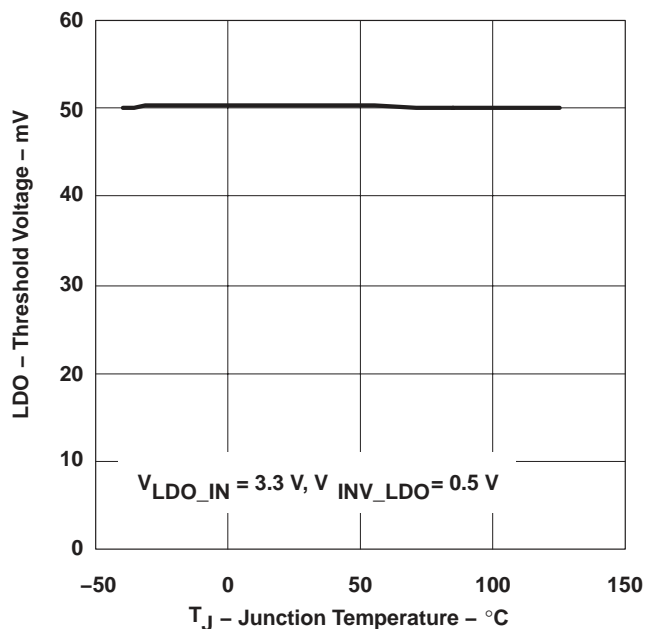
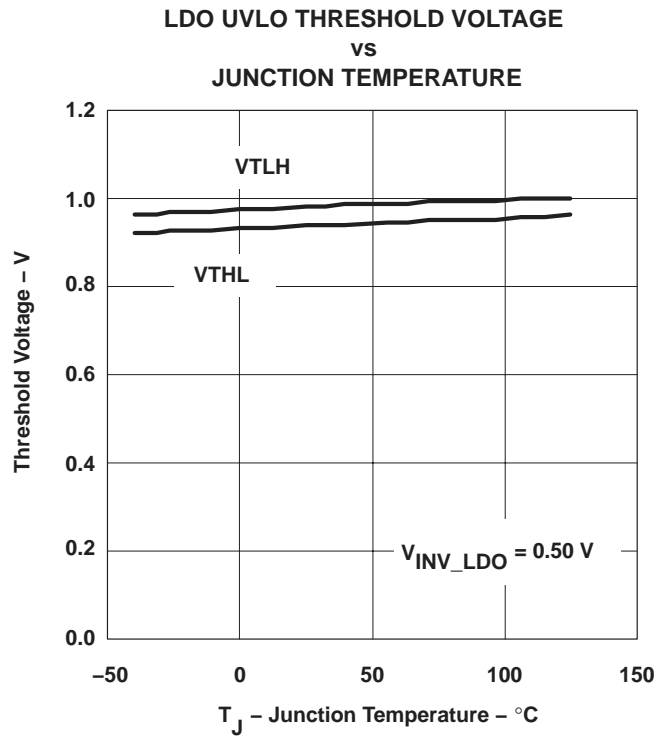


Figure 15

NOTE:  $V_{VIN\_SENSE} = 12$  V,  $V_{REG5V\_IN} = 5$  V unless otherwise noted.

TYPICAL CHARACTERISTICS



NOTE: V<sub>VIN\_SENSE</sub> = 12 V, V<sub>REG5V\_IN</sub> = 5 V unless otherwise noted.

APPLICATION INFORMATION

The design shown in this application information is a reference design for a notebook PC application. An evaluation module (EVM) is available for customer testing and evaluation. This information allows a customer to fully evaluate the given design using the plug-in EVM shown in Figure 17. For subsequent board revisions, the EVM design can be copied onto the system PCB to shorten the design cycle.

The following key design procedures aid in the design of the notebook PC power supply using TPS5110. An optional circuit composed of Q04, R16, R22 and R24 can be used to increase temperature coefficient of the trip current, which is at the top in the page 18.



APPLICATION INFORMATION

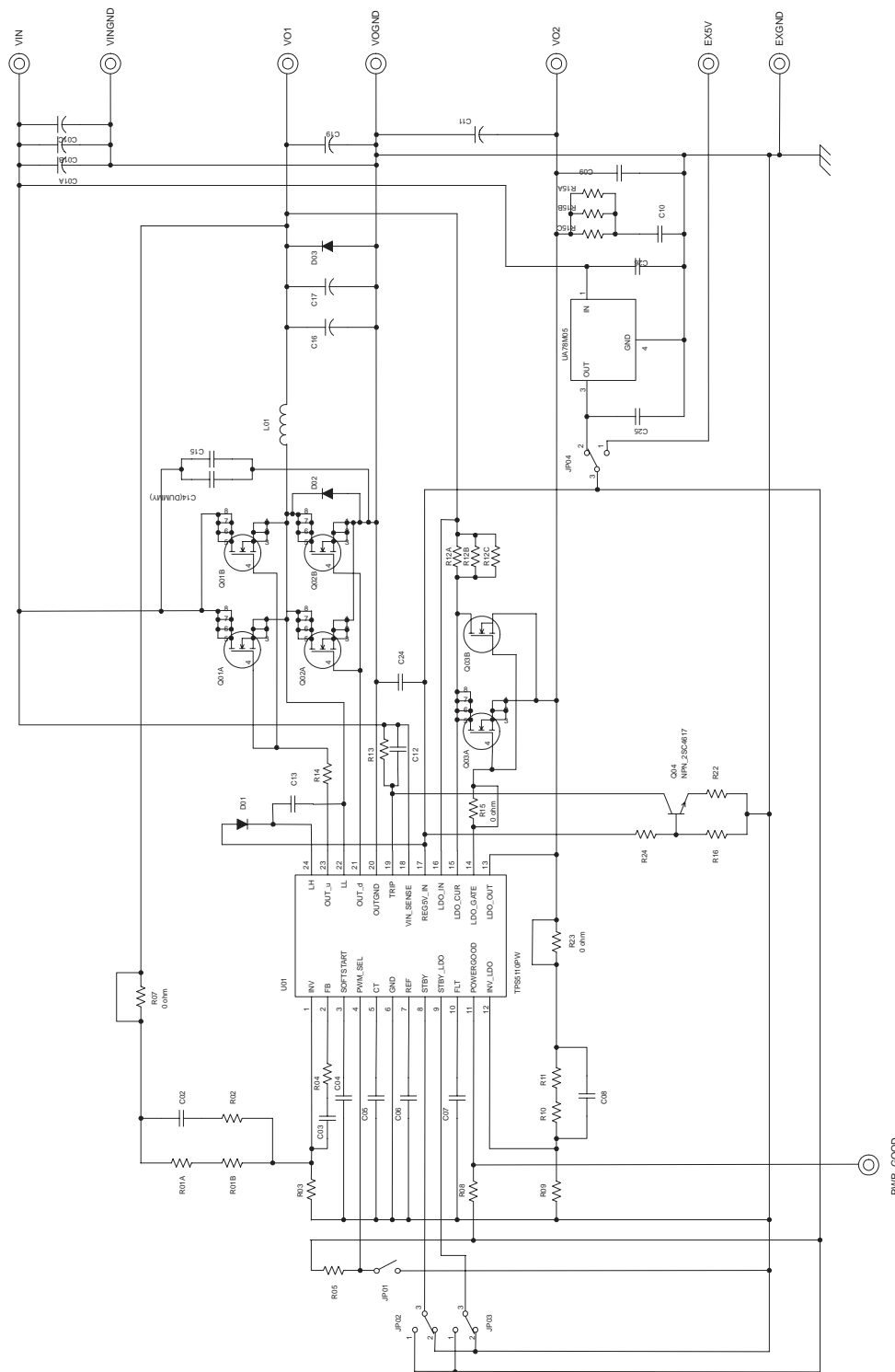


Figure 17. EVM Typical Design

APPLICATION INFORMATION

Table 4. EVM Input and Outputs

VIN†	REG5V_IN	Vo1 (SBRC)	Io1 (SBRC)	Vo2 (LDO)	Io2 (LDO)
8 V to 20 V	5 V	1.8 V	6 A	1.5 V	3 A

† Recommended operation voltage for the EVM

output voltage setpoint calculation

The reference voltage and the voltage divider set the output voltage. In the TPS5110, the reference voltage is 0.85 V, and the divider is composed of three resistors in the EVM design that are R01A, R01B and R03 for switching regulator output; R10, R11 and R09 for LDO regulator output.

$$V_O = \frac{R1 \times V_{REF}}{R2} + V_{REF} \text{ or } R2 = \frac{R1 \times V_{REF}}{V_O - V_{REF}}$$

where R1 is the top resistor (kΩ) (R01A + R01B or R10 + R11); R2 is the bottom resistor (kΩ) (R03 or R09); V<sub>O</sub> is the required output voltage (V); V<sub>REF</sub> is the reference voltage (0.85 V in TPS5110). The value for R1 is set as a part of the compensation circuit and the value of R2 may be calculated to achieve the desired output voltage. In the EVM design, the value of R1 was determined as R01A = R01B = 10 kΩ for V<sub>O1</sub>, and R10 = 6.8 kΩ and R11 = 820 Ω for V<sub>O2</sub> considering stability. For V<sub>O1</sub>:

$$R03 = \frac{20 \text{ k}\Omega \times 0.85}{1.8 - 0.85} = 17.89 \text{ k}\Omega$$

Use 18 kΩ.

For V<sub>O2</sub>:

$$R09 = \frac{(6.8 \text{ k}\Omega + 820) \times 0.85}{1.5 - 0.85} = 9.96 \text{ k}\Omega$$

Use 10 kΩ.

The values of R01A, R01B, R10 and R11 are chosen so that the calculated values of R03 and R09 are those of standard value resistor and the V<sub>O</sub> setpoint maintains the highest precision. This can be best accomplished by combining two resistor values. If a standard value resistor can not be applied such as R10 and R11, use a value for R10 that is just slightly less than the desired total. A small value resistor in the range of tens or hundreds of ohms for R11 can then be added to generate the desired final value.

---

## APPLICATION INFORMATION

### output inductor selection

The required value for the output-filter inductor can be calculated by using the equation:

$$L_{OUT} = \frac{(V_{IN} - V_O)}{k \times I_{OUT}} \times \frac{V_O}{V_{IN}} \times \frac{1}{f_S}$$

Where  $L_{OUT}$  is output filter inductor value (H),  $V_{IN}$  is the input voltage (V),  $I_{OUT}$  is the maximum output current (A),  $f_S$  is the switching frequency (Hz). Constant value  $k$ , a ratio of ripple current to output current, is typically in the range 0.2 to 0.3. For  $V_{O1}$ , the calculation for the maximum input voltage of 20 V, yields a value for  $L_{O1}$  of 3.03  $\mu$ H, and for minimum input voltage of 8 V, 2.58  $\mu$ H. For the EVM, a value of 2.8  $\mu$ H is used for  $L_{O1}$ .

### output inductor ripple current

The output-inductor current can affect not only the efficiency, but also the output voltage ripple. The equation is exhibited below:

$$I_{RIPPLE} = \frac{V_{IN} - V_O - I_O \times (R_{DS(on)} + R_L)}{L_{OUT}} \times \frac{V_O}{V_{IN}} \times \frac{1}{f_S}$$

where  $I_{RIPPLE}$  is the peak-to-peak ripple current (A) through the inductor;  $I_O$  is the output current;  $R_{DS(on)}$  is the on-time resistance of MOSFET ( $\Omega$ );  $R_L$  is the inductor dc resistance ( $\Omega$ ). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value. For the EVM design, the worst-case output ripple occurs with  $V_{IN} = 20$  V:

Example:  $V_{IN} = 20$  V;  $V_O = 1.8$  V;  $I_O = 6$  A;  $R_{DS(on)} = 25$  m $\Omega$ ;  $R_L = 10$  m $\Omega$ ;  $f_S = 300$  kHz;  $L_{OUT} = 2.8$   $\mu$ H.

Then, the ripple current  $I_{RIPPLE} = 1.93$  A

### output capacitor selection (SBRC)

Selection of the output capacitor is basically dependent on the amount of peak-to-peak ripple voltage allowed on the output and the ability of the capacitor to dissipate the RMS ripple current. Assuming that the ESR of the output filter sees the entire inductor-ripple current then:

$$V_{PP} = I_{RIPPLE} \times R_{ESR}$$

And a suitable capacitor must be chosen so that the peak-to-peak output ripple is within the limits allowable for the application.

## APPLICATION INFORMATION

### output capacitor RMS current (SBRC)

Assuming the inductor-ripple current totally goes through the output capacitor to ground, the RMS current in the output capacitor can be calculated as:

$$I_{O(rms)} = \frac{I_{RIPPLE}}{\sqrt{12}}$$

where  $I_{O(rms)}$  is maximum RMS current in the output capacitor (A);  $I_{RIPPLE}$  is the peak-to-peak inductor-ripple current (A).

Example:  $I_{RIPPLE} = 1.93$  A, therefore,  $I_{O(rms)} = 0.56$  A

### input capacitor RMS current (SBRC)

Assuming the input current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$I_{i(rms)} = \sqrt{I_O^2 \times D \times (1 - D) + \frac{1}{12} D \times I_{RIPPLE}^2}$$

where  $I_{i(rms)}$  is the input RMS current in the input capacitor (A);  $I_O$  is the output current (A);  $I_{RIPPLE}$  is the peak-to-peak output inductor-ripple current;  $D$  is the duty cycle and defined as  $V_O/V_I$  in this case. From the equation, it can be seen that the highest input RMS current usually occurs at the lowest input voltage, so it is the worst case design for input capacitor ripple current.

Example:  $I_O = 6$  A;  $D = 22.5\%$ ;  $I_{RIPPLE} = 1.6$  A then,  $I_{i(rms)} = 2.5$  A

The input capacitors must be chosen so that together they can safely handle the input-ripple current. Depending on the input filtering and the dc input voltage source, not all the ripple current flows through the input capacitors, but some may be present on the input leads to the EVM.

### soft start

The soft-start timing can be adjusted by selecting the soft-start capacitor value. The equation is;

$$C_{SOFT} = 2.3 \times 10^{-6} \times \frac{T_{SOFT}}{0.85}$$

where  $C_{SOFT}$  is the soft-start capacitor ( $\mu$ F) (C04 in EVM design);  $T_{SOFT}$  is the start-up time (s).

Example:  $T_{SOFT} = 5$  ms, therefore,  $C_{SOFT} = 0.0135$   $\mu$ F.

## APPLICATION INFORMATION

### current protection (SBRC)

The current limit in TPS5110 is set using an internal current source and an external resistor (R13). The current limit protection circuit compares the drain-to-source voltage of the high-side and low-side drivers with respect to the set-point voltage. If the voltage up exceeds the limit during high-side conduction, the current-limit circuit terminates the high-side driver pulse. If the set point voltage is exceeded during low-side conduction, the low-side pulse is extended through the next cycle. Together this action has the effect of decreasing the output voltage until the under voltage protection circuit is activated and the fault latch is set and both the high and low-side MOSFET drivers are shut off. The equation below should be used for calculating the external resistor value for current protection set point:

$$R_{CL} = \frac{R_{DS(on)} \times \left( I_{TRIP} + \frac{I_{RIPPLE}}{2} \right)}{13 \times 10^{-6}}$$

where  $R_{CL}$  is the external current limit resistor (R13);  $R_{DS(on)}$  is the low-side MOSFET(Q02) on-time resistance.  $I_{TRIP}$  is the required current limit.

Example:  $R_{DS(on)} = 25 \text{ m}\Omega$ ,  $I_{TRIP} = 6 \text{ A}$ ,  $I_{RIPPLE} = 1.93 \text{ A}$ , therefore,  $R_{CL} = 13.4 \text{ k}\Omega$ .

It should be noted that  $R_{DS(on)}$  of a FET is highly dependent on temperature, so to insure full output at maximum operating temperature, the value of  $R_{DS(on)}$  in the above equation should be adjusted. For maximum stability, it is recommended that the high-side MOSFET(s) has same, or slightly higher  $R_{DS(on)}$  than the low-side MOSFET(s). If the low-side MOSFET(s) has a higher  $R_{DS(on)}$ , in certain low duty cycle applications it may be possible for the device to regulate at an output current higher than that set by the above equation by increasing the high side conduction time to compensate for the missed conduction cycle caused by the extension of the previous low-side pulse.

### timer latch

The TPS5110 includes fault latch function with a user adjustable timer to latch the MOSFET drivers in case of a fault condition. When either the OVP or UVP comparator detect a fault condition, the timer starts to charge FLT capacitor (C07), which is connected with FLT pin 10. The circuit is designed so that for any value of FLT capacitor, the under-voltage latch time  $t_{(uvplatch)}$  is about 50 times larger than the over-voltage latch time  $t_{(ovplatch)}$ . The equations needed to calculate the required value of the FLT capacitor for the desired over and under-voltage latch delay times are:

$$C_{LAT} = 2.3 \times 10^{-6} \times \frac{t_{(uvplatch)}}{1.185} \quad \text{and} \quad C_{LAT} = 125 \times 10^{-6} \times \frac{t_{(ovplatch)}}{1.185}$$

where  $C_{LAT}$  is the external capacitor,  $t_{(uvplatch)}$  is the time from UVP detection to latch.  $t_{(ovplatch)}$  is the time from OVP detection to latch.

For the EVM,  $t_{(uvplatch)} = 5 \text{ ms}$  and  $t_{(ovplatch)} = 0.1 \text{ ms}$ , so  $C_{LAT} = 0.01 \text{ }\mu\text{F}$

If the voltage on the FLT pin reaches 1.185 V, the fault latch is set, and the MOSFET drivers are set as follows:

### under-voltage protection

The under-voltage comparator circuit continually monitors the voltage at the INV and INV\_LDO pins. If the voltage at either pin falls below 65% of the 0.85-V reference, the timer begins to charge the FLT capacitor. If the fault condition persists beyond the time  $t_{(uvplatch)}$ , the fault latch is set and both the high side and low-side drivers, and LDO regulator drivers are forced OFF.

## APPLICATION INFORMATION

### short circuit protection

The short circuit protection circuitry uses the UVP circuit to latch the MOSFET drivers. When the current-limit circuit limits the output current, then the output voltage goes below the target-output voltage and UVP comparator detects a fault condition as described above.

### over voltage protection

The over-voltage comparator circuit continually monitors the voltage at the INV and INV\_LDO pins. If the voltage at either pin rises above 112% of the 0.85-V reference, the timer begins to charge the FLT capacitor. If the fault condition persists beyond the time  $t_{(ovplatch)}$ , the fault latch is set and the high-side drivers are forced OFF, while the low-side drivers are forced ON, and LDO regulator drivers are forced OFF.

**CAUTION:** Do not set the FLT pin to a lower voltage (or GND) while the device is timing out an OVP or UVP event. If the FLT pin is manually set to a lower voltage during this time, output overshoot may occur. The TPS5110 must be reset by grounding STBY and STBY\_LDO, or dropping down REG5V\_IN.

### disablement of the protection function

If it is necessary to inhibit the protection functions of the TPS5110 for troubleshooting or other purposes, the OCP, OVP and UVP circuits may be disabled.

- OCP(SBRC): Remove the current-limit resistors R13 to disable the current limit function.
- OCP(LDO): Short-circuit R12 to disable the current limit function.
- OVP, UVP: Grounding the FLT pin can disable OVP and UVP.

### output capacitor selection for LDO

To keep stable operation of the LDO, capacitance of more than 33  $\mu$ F and  $R_{ESR}$  of more than 30 m $\Omega$  are recommended for the output capacitor.

### power MOSFET selection for LDO

Also, to keep stable operation of the LDO, lower input capacitance is recommended for the external power MOSFET. However, too small input capacitance may lead the feedback loop into unstable region. In such a case, the gate resistor of several hundred ohms keeps the LDO operation in the stable state.

### current protection for LDO

If excess output current flows through sense resistor (R12) and the voltage drop exceeds 50 mV, the output voltage is reduced to approximately 22% of the nominal value, thus activates UVP to start the FLT latch timer.

When the set current is 4 A, the value of R12 is 12.5 m $\Omega$ .

APPLICATION INFORMATION

layout guidelines

Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milli-amps to tens of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, parallel the low-level components. Below are specific points to consider before the layout of a TPS5110 design begins.

- A four-layer PCB design is recommended for design using the TPS5110. For the EVM design, the top layer contains the interconnection to the TPS5110, plus some additional signal traces. Layer 2 is fully devoted to the DRVGND plane. Layer 3 mainly has wide VIN and V<sub>O1</sub> pattern. The bottom layer is almost devoted to other GND plane including ANAGND, and the rest is to wide signal trace for V<sub>O2</sub>.
- All sensitive analog components such as INV, REF, CT, GND, FLT and SOFTSTART should be reference to ANAGND.
- Ideally, all of the area directly under the TPS5110 chip should also be ANAGND.
- ANAGND and DRVGND should be isolated as much as possible, with a single point connection between them.

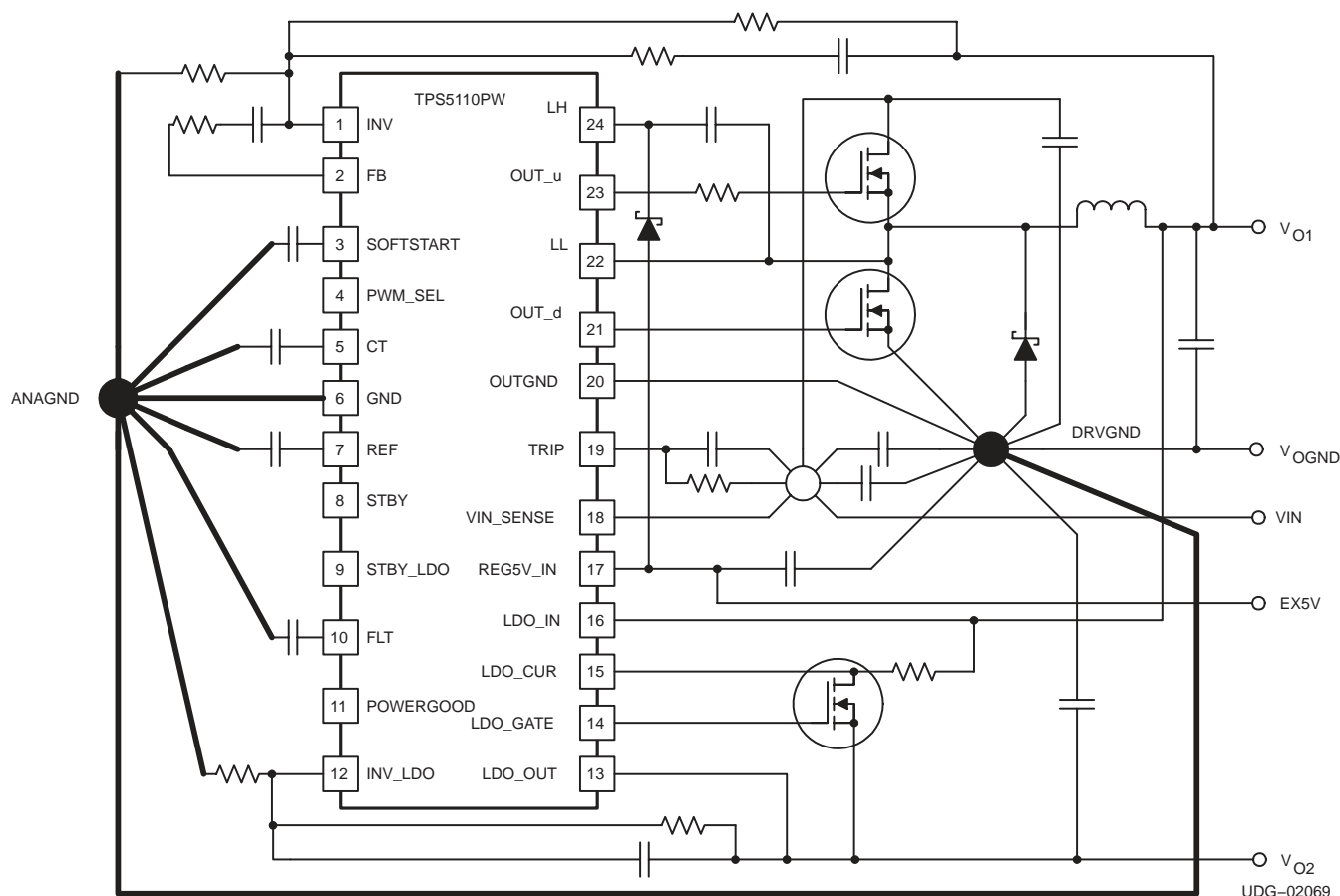


Figure 18. Four-Layer PCB Diagram

APPLICATION INFORMATION

low-side MOSFET(s)

- The source of low-side MOSFET(s) should be referenced to DRVGND, otherwise ANAGND is subject to the noise of the outputs.
- DRVGND should be connected to the main ground plane close to the source of the low-side FET.
- OUTGND should be placed close to the source of low-side MOSFET(s).
- The Schottky diode anode, the returns for the high-frequency bypass capacitor for the MOSFETs, and the source of the low-side MOSFET(s) traces should be routed as close together as possible.

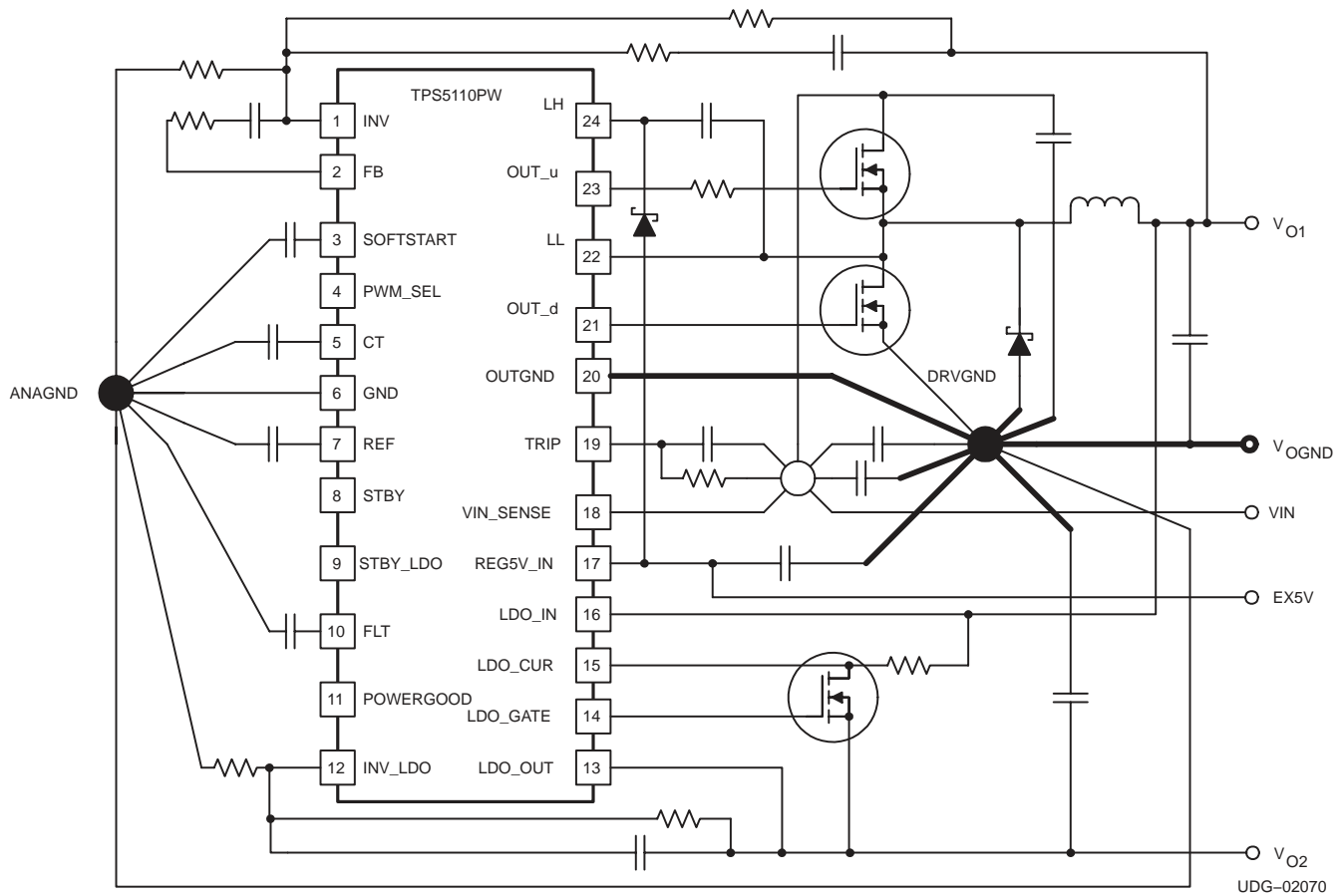


Figure 19. Low-Side MOSFETs Diagram



APPLICATION INFORMATION

connections

- Connections from the drivers to the gate of the power MOSFETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used. In addition, as for the current limit noise issue, use of a gate resistor on the high-side MOSFET(s) considerably reduce the noise at the LL node, improving the performance of the current limit function.
- The connection from LL to the power MOSFETs should be as short and wide as possible.

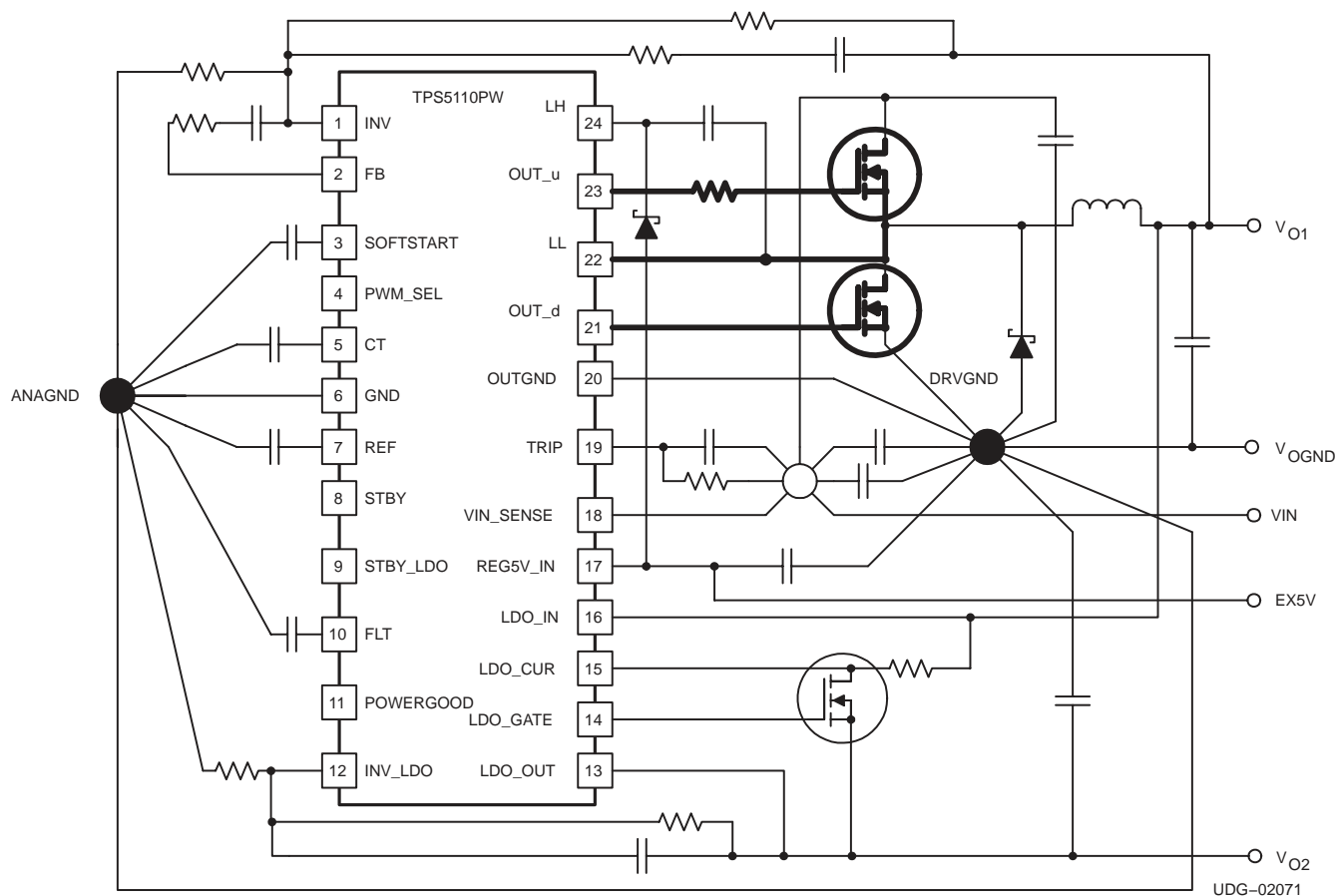


Figure 20. Connections From the Drivers to the Gate Diagram

APPLICATION INFORMATION

bypass capacitor

- The bypass capacitor for VIN\_SENSE should be placed close to the TPS5110.
- The bulk-storage capacitors across VIN should be placed close to the power MOSFETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side MOSFET(s) and to the source of the low-side MOSFET(s).
- For aligning phase between the drain of high-side MOSFET(s) and the TRIP pin, and for noise reduction, a 0.1- $\mu$ F capacitor should be placed in parallel with the trip resistor.

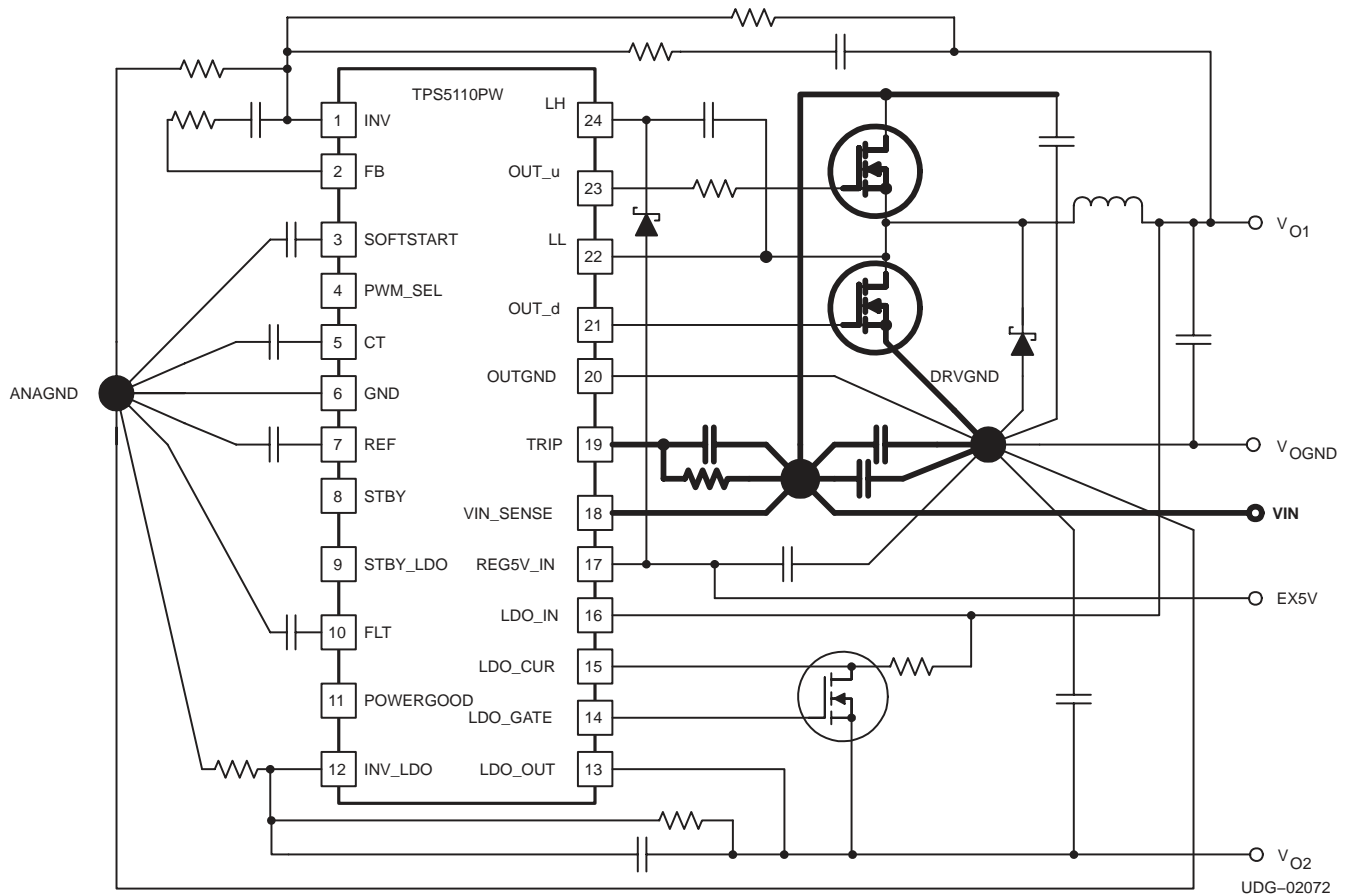


Figure 21. Bypass Capacitor Diagram

APPLICATION INFORMATION

bootstrap capacitor

- The bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5110.
- LH and LL should be routed close to each other to minimize differential-mode noise coupling to these traces.
- LH and LL should not be routed near the control pin area (ex. INV, FB, REF, etc.).

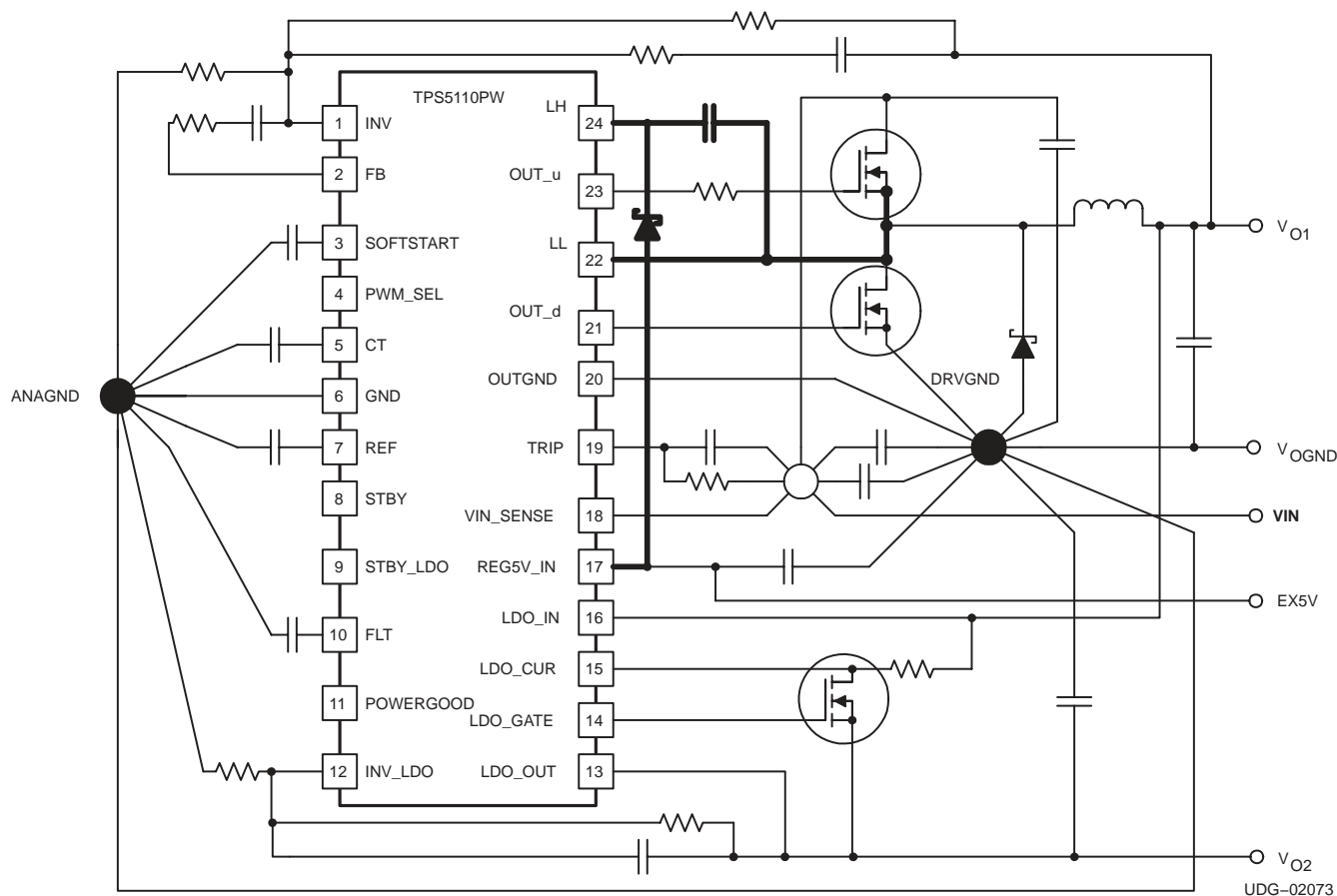


Figure 22. Bootstrap Capacitor Diagram

APPLICATION INFORMATION

output voltage

- The output voltage sensing trace should be isolated by either ground plane.
- The output voltage sensing trace should not be placed under the inductors on same layer.
- The feedback components should be isolated from output components, such as, MOSFETs, inductors, and output capacitors. Otherwise the feedback signal line is susceptible to output noise.
- The resistors for set up output voltage should be referenced to ANAGND.
- The INV trace should be as short as possible.

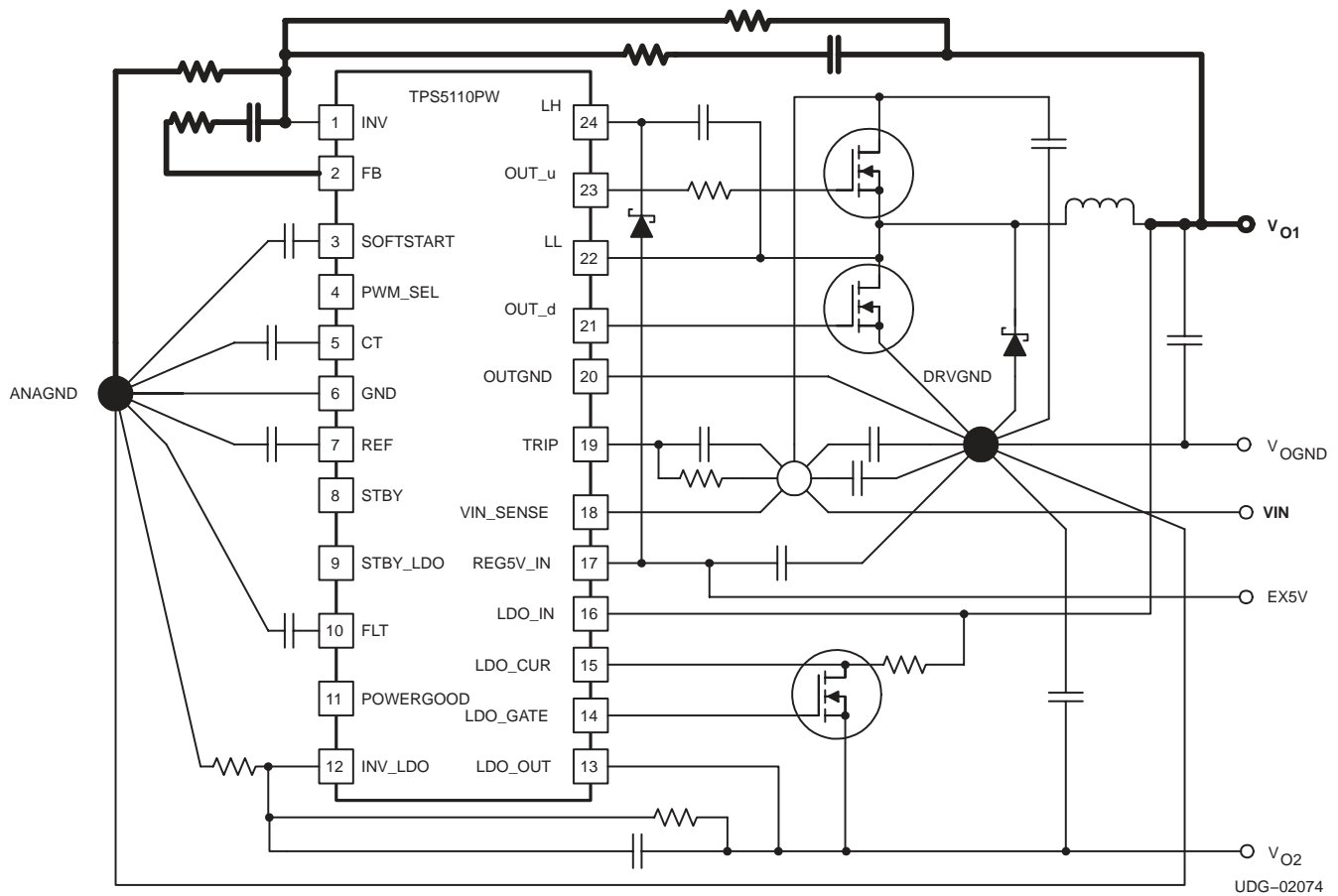


Figure 23. Output Voltage Diagram

APPLICATION INFORMATION

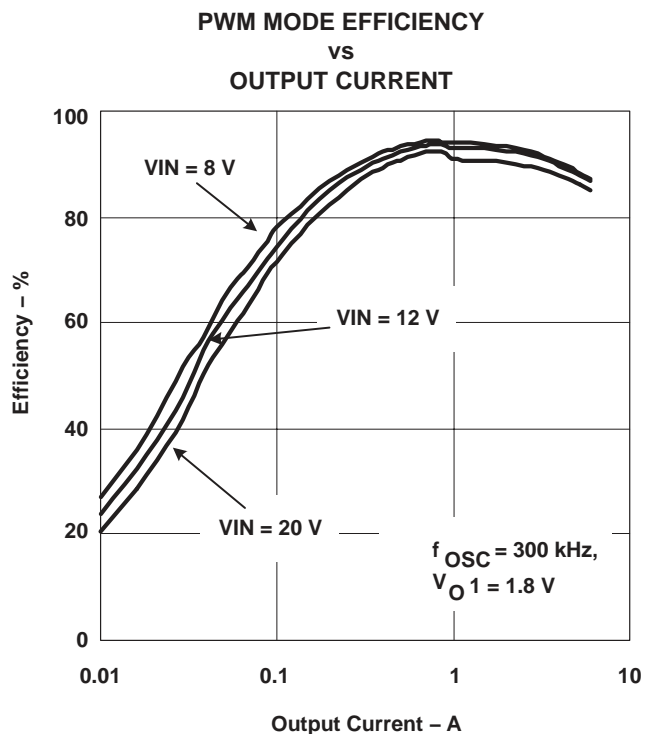


Figure 24

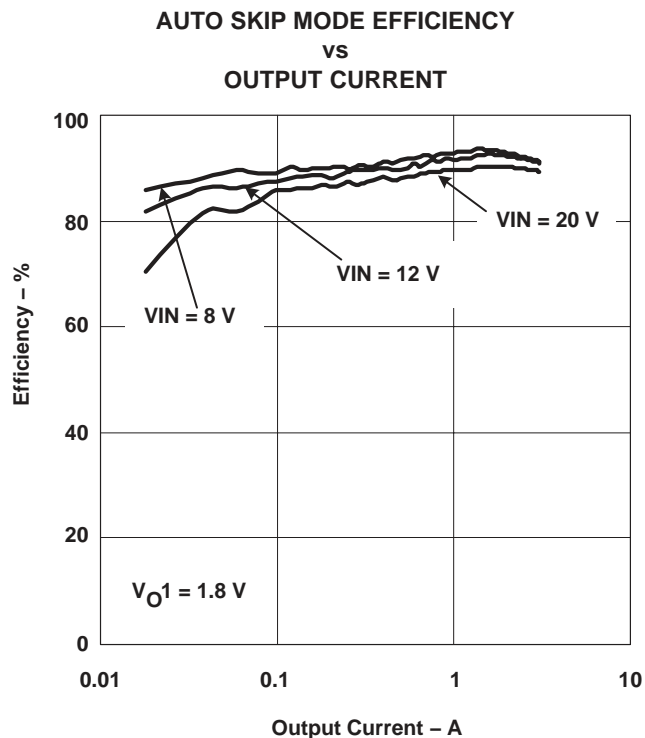


Figure 25

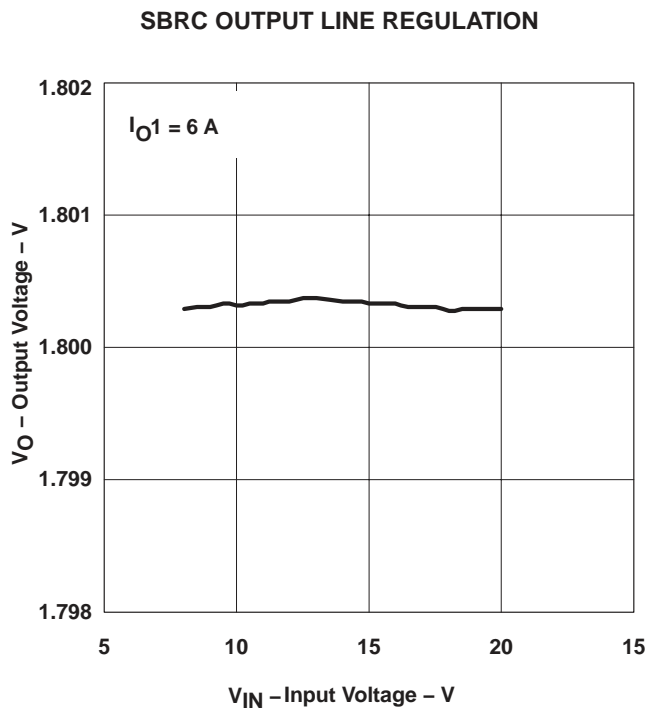


Figure 26

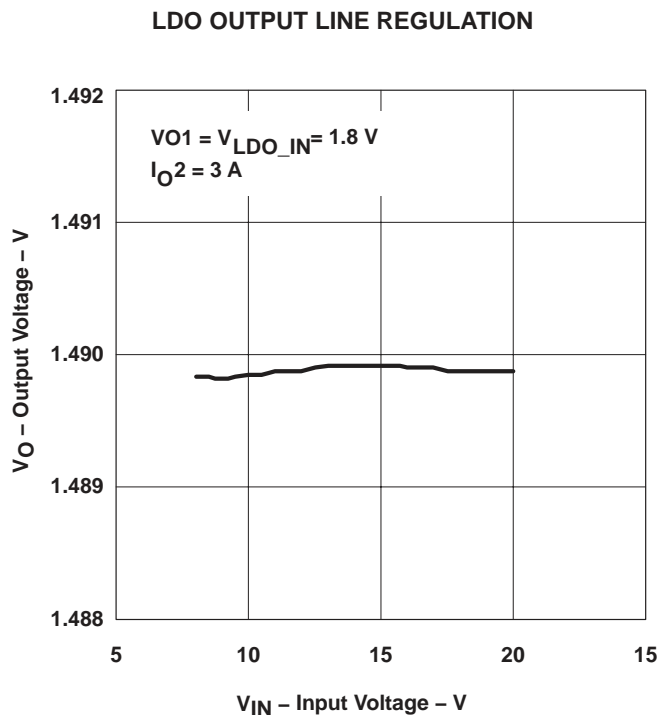


Figure 27

APPLICATION INFORMATION

SBRC OUTPUT LOAD REGULATION

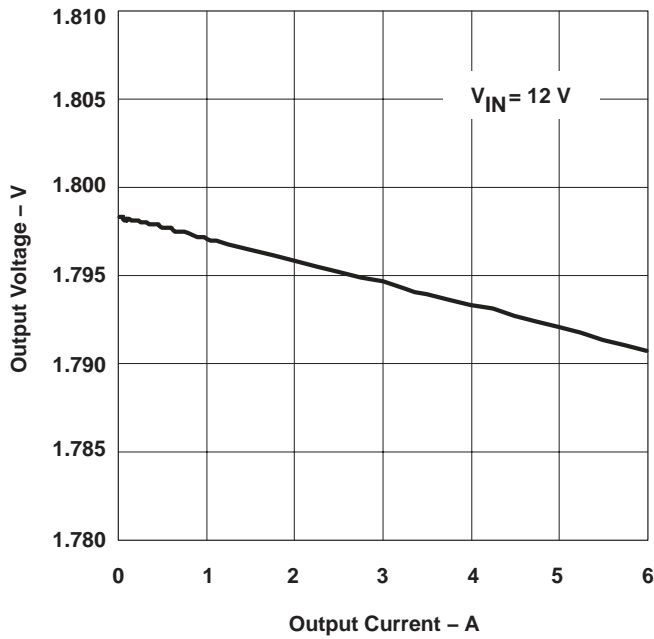


Figure 28

LDO OUTPUT LOAD REGULATION

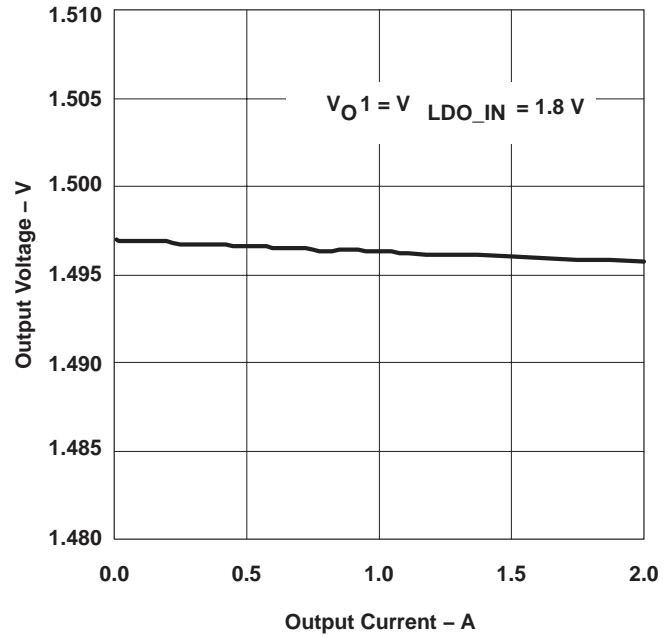
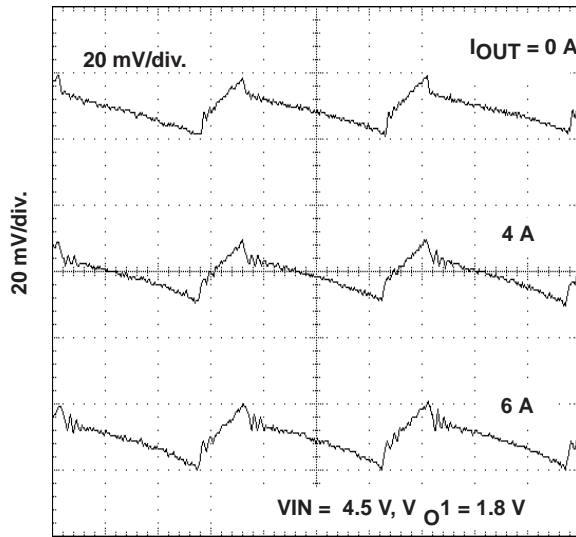


Figure 29

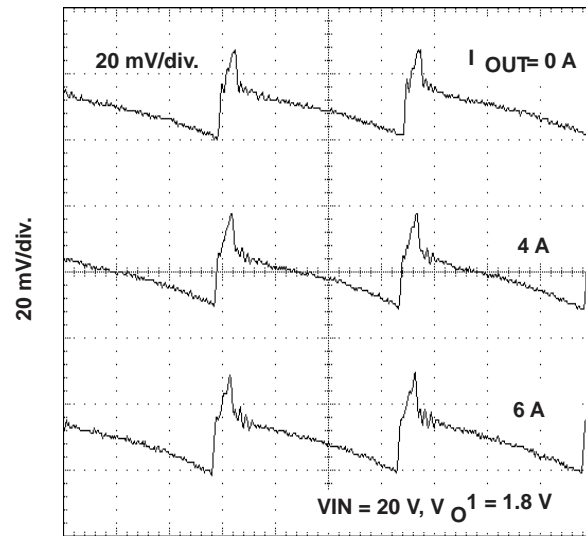
SBRC OUTPUT VOLTAGE RIPPLE



t - time - 1  $\mu$ s/div.

Figure 30

SBRC OUTPUT VOLTAGE RIPPLE

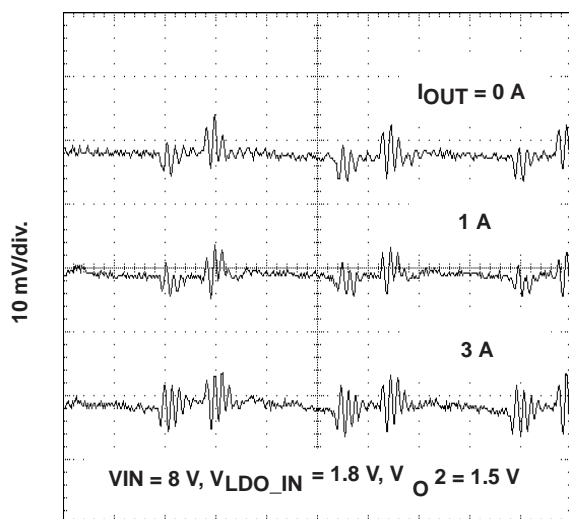


t - time - 1  $\mu$ s/div.

Figure 31

APPLICATION INFORMATION

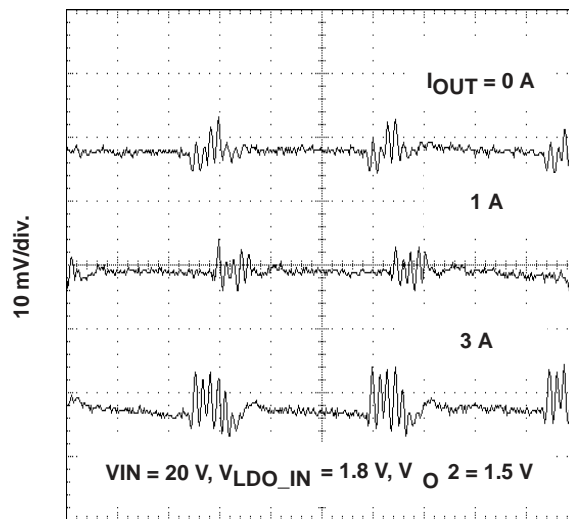
LDO OUTPUT VOLTAGE RIPPLE



t – time – 1  $\mu\text{s}/\text{div.}$

Figure 32

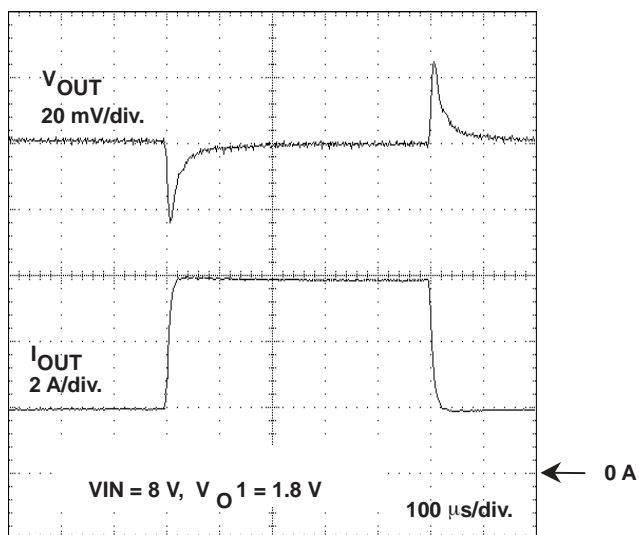
LDO OUTPUT VOLTAGE RIPPLE



t – time – 1  $\mu\text{s}/\text{div.}$

Figure 33

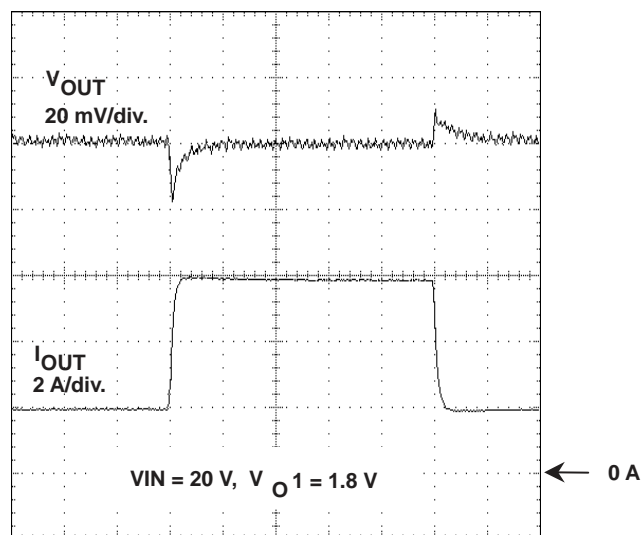
SBRC LOAD TRANSIENT RESPONSE



t – time – 100  $\mu\text{s}/\text{div.}$

Figure 34

SBRC LOAD TRANSIENT RESPONSE

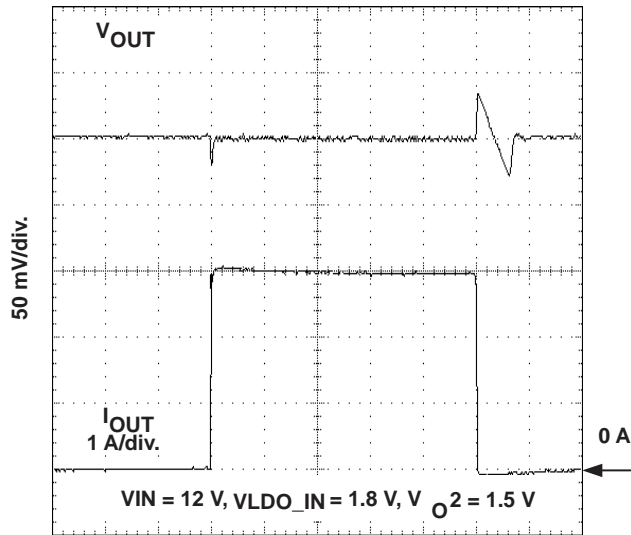


t – time – 100  $\mu\text{s}/\text{div.}$

Figure 35

APPLICATION INFORMATION

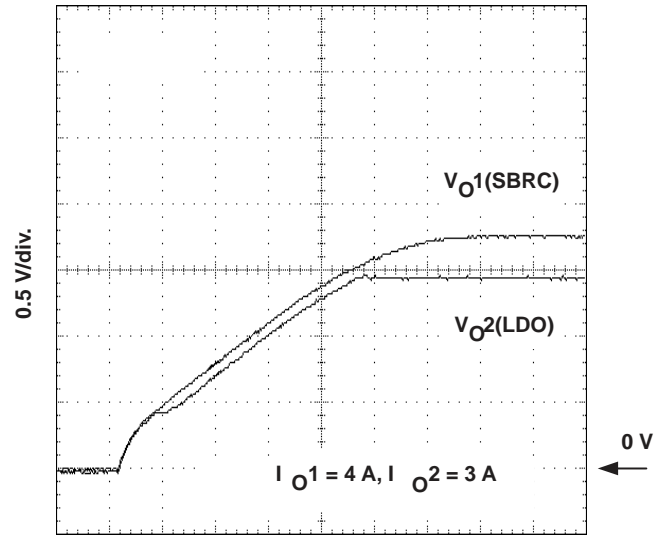
LDO LOAD TRANSIENT RESPONSE



t – time – 100  $\mu$ s/div.

Figure 36

SBRC-LDO SIMULTANEOUS START-UP



t – time – 1  $\mu$ s/div.

Figure 37

SBRC GAIN AND PHASE

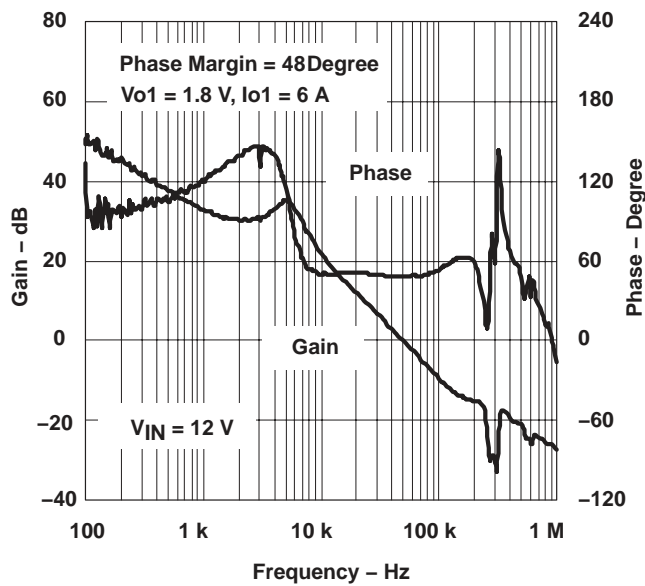


Figure 38

LDO GAIN AND PHASE

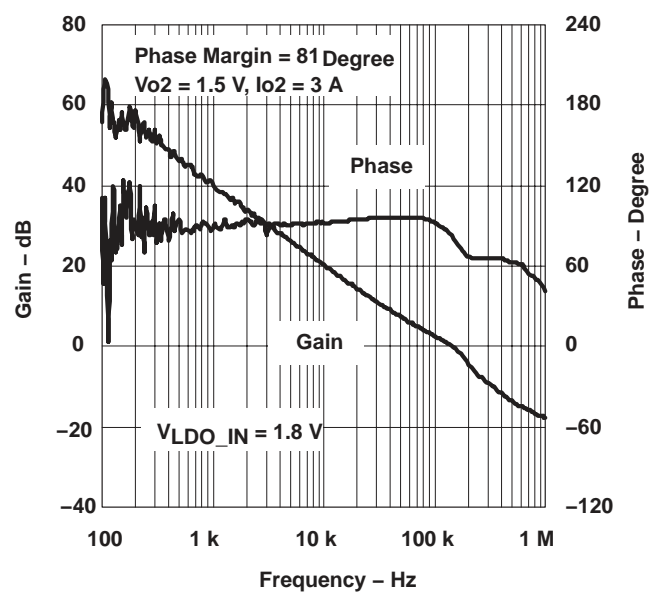


Figure 39



## APPLICATION INFORMATION

Table 5. Bill of Materials

	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C01A	1	SP-VCAP, 22 $\mu$ F, 27 V, 8.3x8.3mm	Panasonic	EEFWA27220P
	C02, C03	2	Ceramic, 4700 pF, 10%, 2.0x1.25mm		
	C05	1	Ceramic, 47 pF, 5%, 2.0x1.25mm		
	C04, C07	2	Ceramic, 0.01 $\mu$ F, 2.0x1.25mm		
	C09	1	SPCAP, 47 $\mu$ F, 6.3 V, 7.3x4.3mm	Panasonic	EEFCD0J470R
	C01B, C06, C11, C12, C13, C19	6	Ceramic, 0.1 $\mu$ F, 2.0x1.25mm		
	C15	1	2.2 $\mu$ F, 35 V, 3.2x2.5mm	Taiyo-Yuden	GMK325BJ225MN-B
	C16, C17	2	SPCAP, 150 $\mu$ F, 2.5 V, 7.4x4.3mm	Panasonic	EEFUD0E151R
	C24	1	Ceramic, 10 $\mu$ F, 25 V	Taiyo-Yuden	TMK325BJ106MM
	C01C, C08, C10, C14, C25, C26		Removed		
Resistor	R01A, R01B, R09	1	10 k $\Omega$ , 1%, 2.0x1.25mm		
	R02	1	1.2 k $\Omega$ , 2.0x1.25mm		
	R03	1	18 k $\Omega$ , 1%, 2.0x1.25mm		
	R04	1	4.7 k $\Omega$ , 2.0x1.25mm		
	R05, R08	2	100 k $\Omega$ , 2.0x1.25mm		
	R10	1	6.8 k $\Omega$ , 1%, 2.0x1.25mm		
	R11	1	820 $\Omega$ , 1%, 2.0x1.25mm		
	R12A, R12B	2	22 m, 5%, 2.0x1.25mm	Susumu	RL1220T-R022-J
	R13	1	10 k $\Omega$ , 2.0x1.25mm		
	R14	1	10 $\Omega$ , 2.0x1.25mm		
	R12C, R15A, R15B, R15C, R16, R22, R24		Removed		
Inductor	L01	1	2.8 $\mu$ H, 12.5X12.5mm	Sumida	CEP125-2R8MC-H
Diode	D01	1	2.5x1.25mm	Hitachi	HSU119
	D02		Removed		
	D03	1	2.6x4.5mm	Rohm	RB160L-40
Nch MOSFET	Q01B	1	30 V, SOT-8	Fairchild	FDS6612A
	Q02B	1	30 V, SOT-8		FDS6690S*
	Q03A	1	30 V, SOT-8		FD6612A
	Q01A, Q02A, Q03B, Q04		Removed		

APPLICATION INFORMATION

Bill of Materials (continued)

IC	IC01	1	SSOP-24	TI	TPS5110PW
	IC02		Removed		
Jumper	JP01	1	Header, straight, 2-pin	Morex	22-28-4023
			Jumper, shunt		15-29-1025
	JP02, JP03	2	SW, 7x4.5mm	Nikkai	G-12AP
	JP04	1	Header, straight, 3-pin	Morex	22-28-4033
Jumper, shunt			15-29-1025		
Contact	EX5V, EXGND	4		Phoenix	MKDS1.5/2-5.08
	VIN, VINGND				
	VO1, VO2, VOGND	3			MKDS1.5/3-5.08

NOTE: Since the FDS6690S (Q02B) includes an integrated Schottky diode, D02 can be removed.

test setup

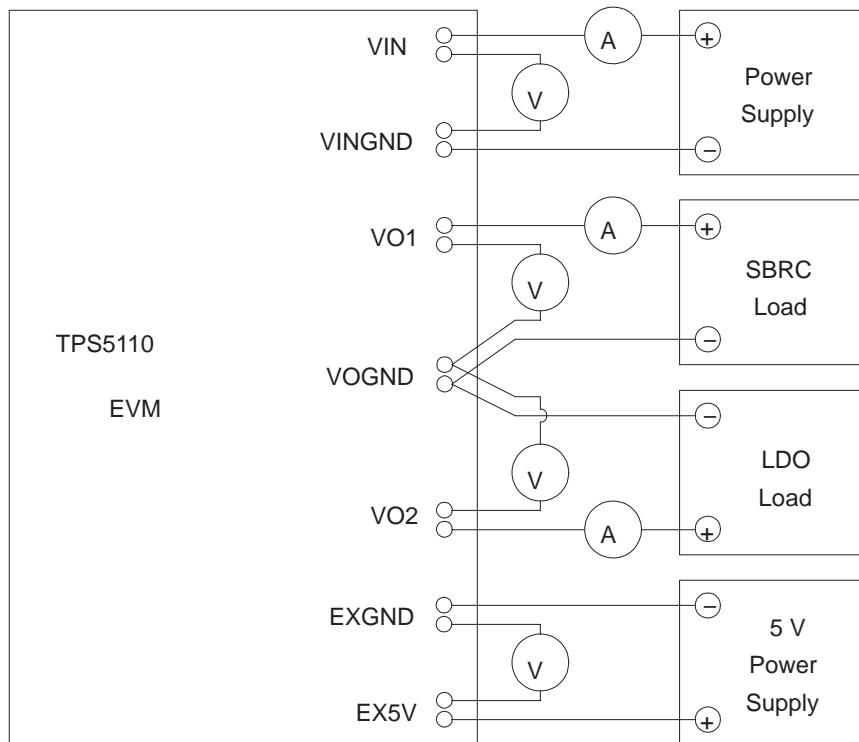


Figure 40. Schematic Diagram of the Test Setup

APPLICATION INFORMATION

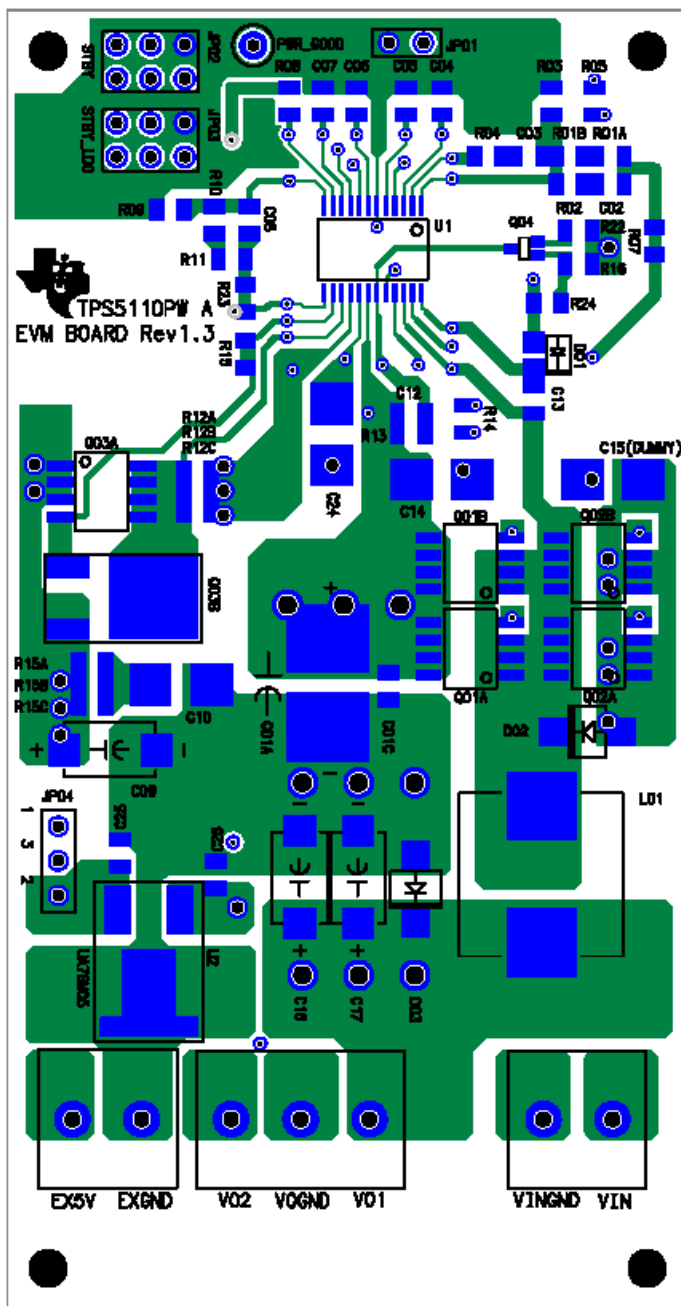


Figure 41. EVM Board Top Layer

APPLICATION INFORMATION

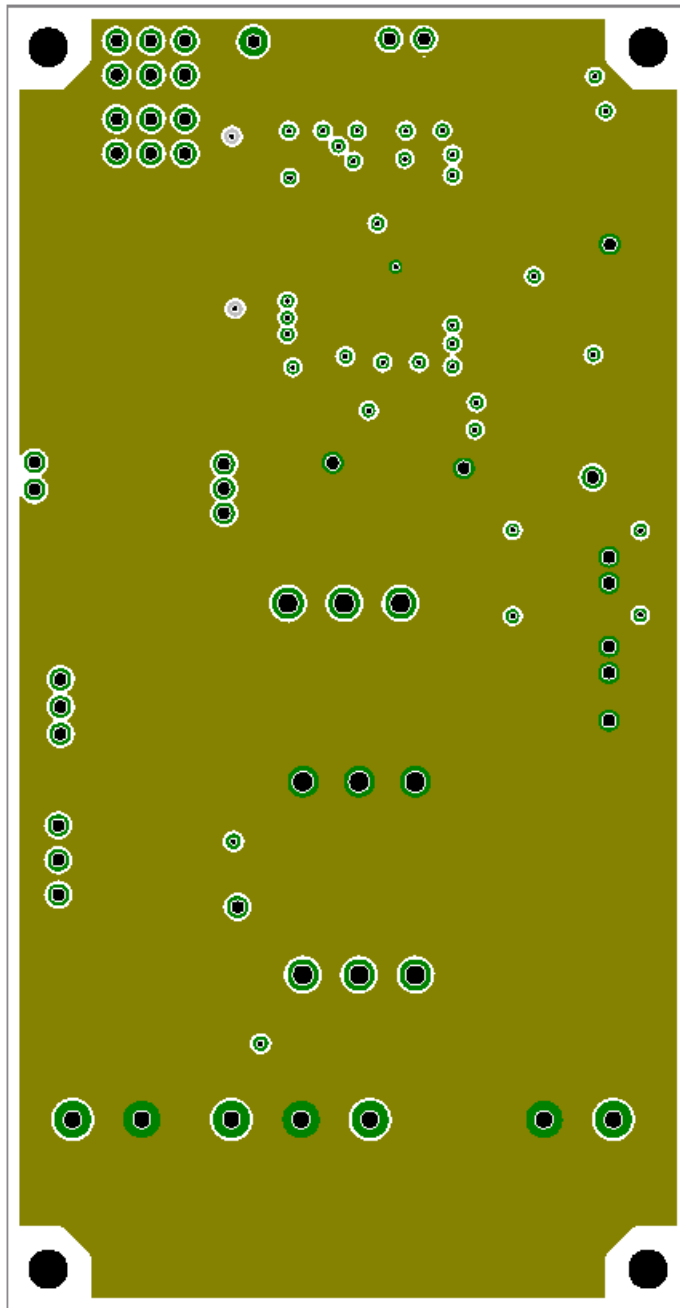


Figure 42. EVM Board Second Layer

## APPLICATION INFORMATION

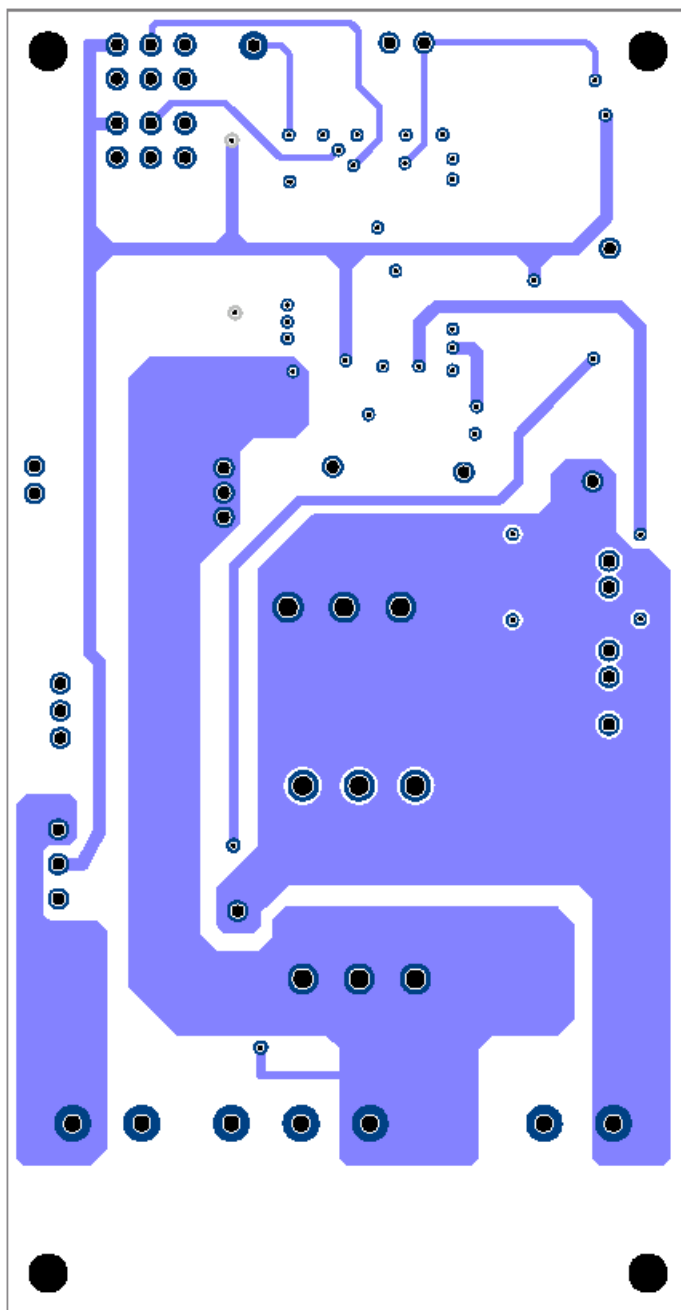


Figure 43. EVM Board Third Layer

APPLICATION INFORMATION

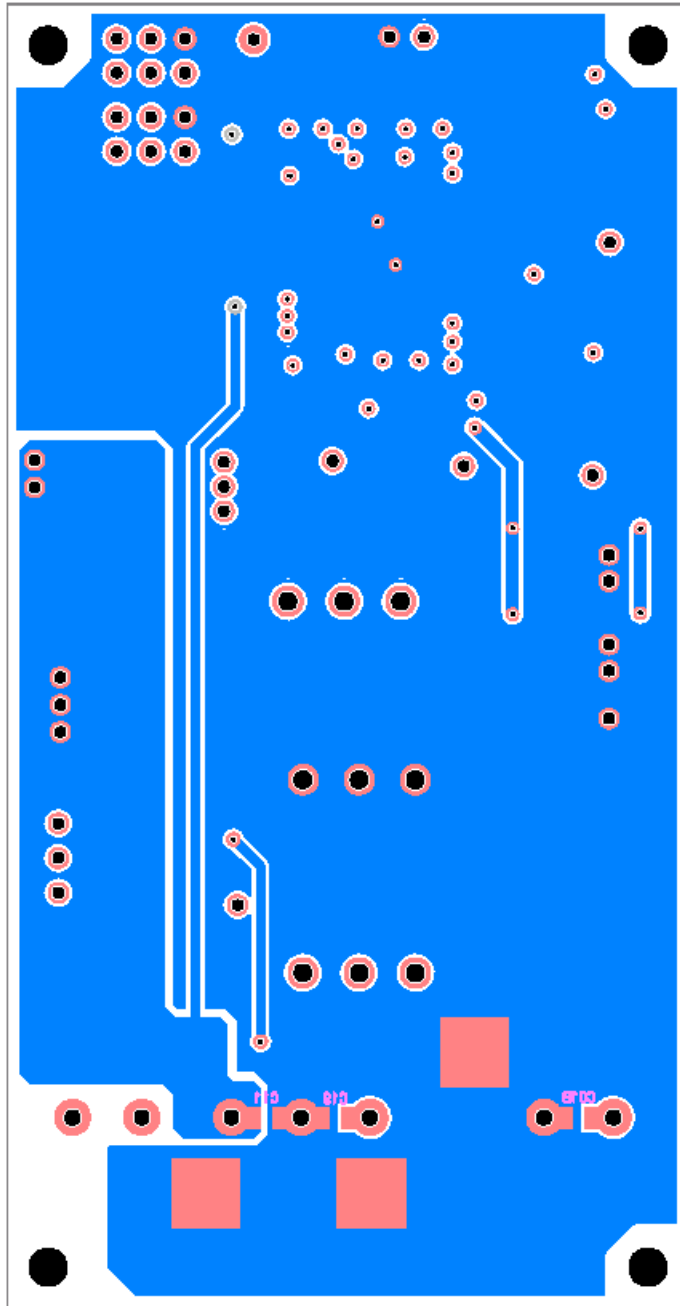


Figure 44. EVM Board Bottom Layer

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5110PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS5110	<a href="#">Samples</a>
TPS5110PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS5110	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

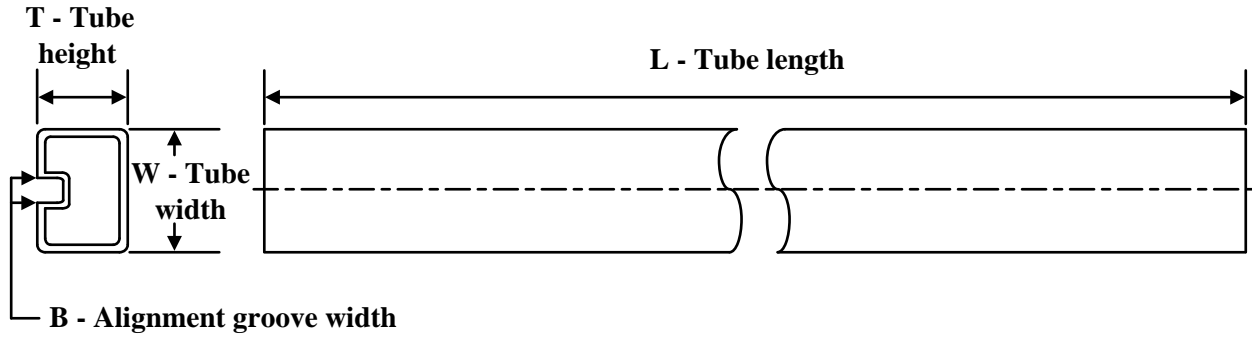

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5110PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5110PWR	TSSOP	PW	24	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS5110PW	PW	TSSOP	24	60	530	10.2	3600	3.5

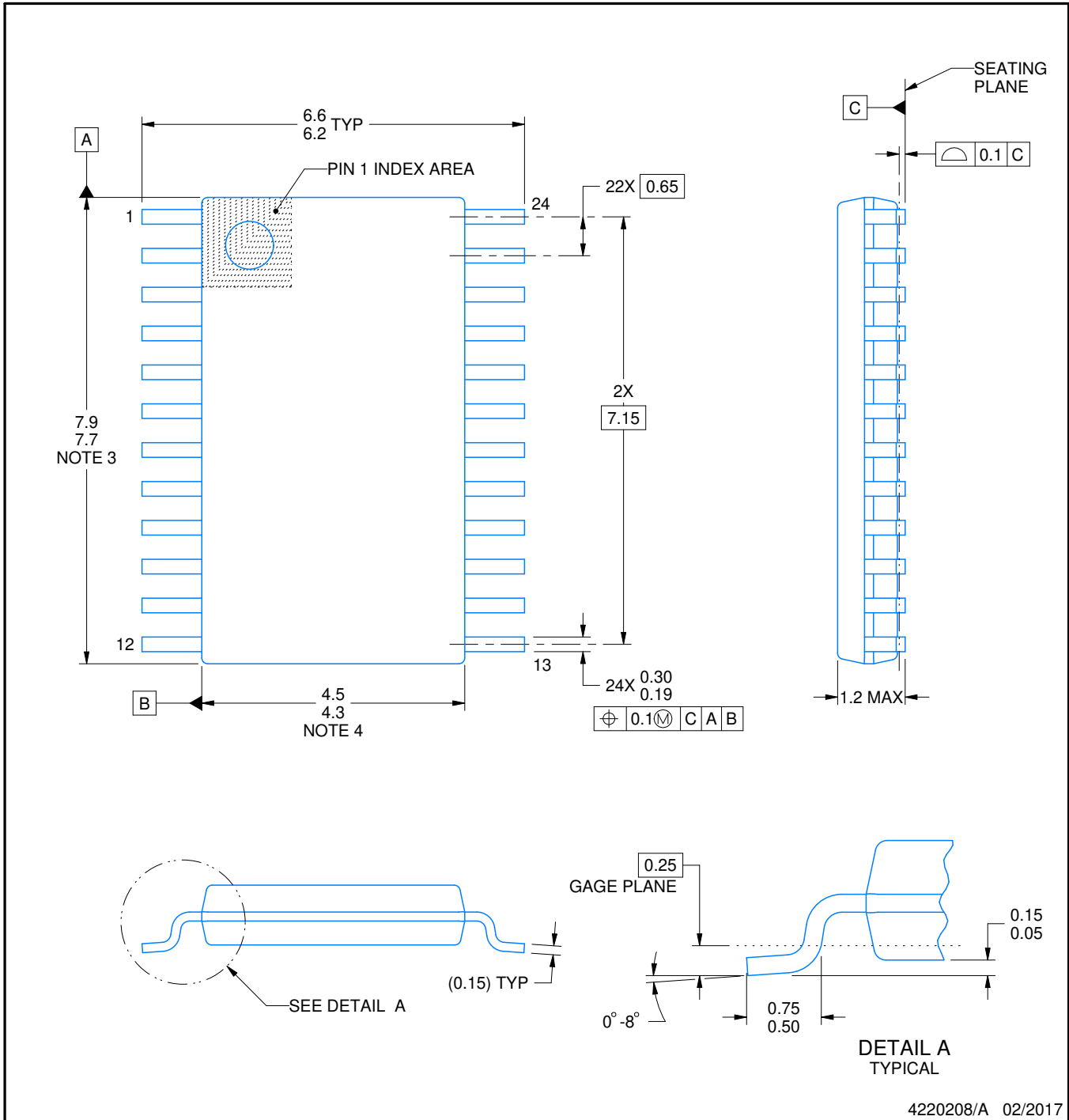
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

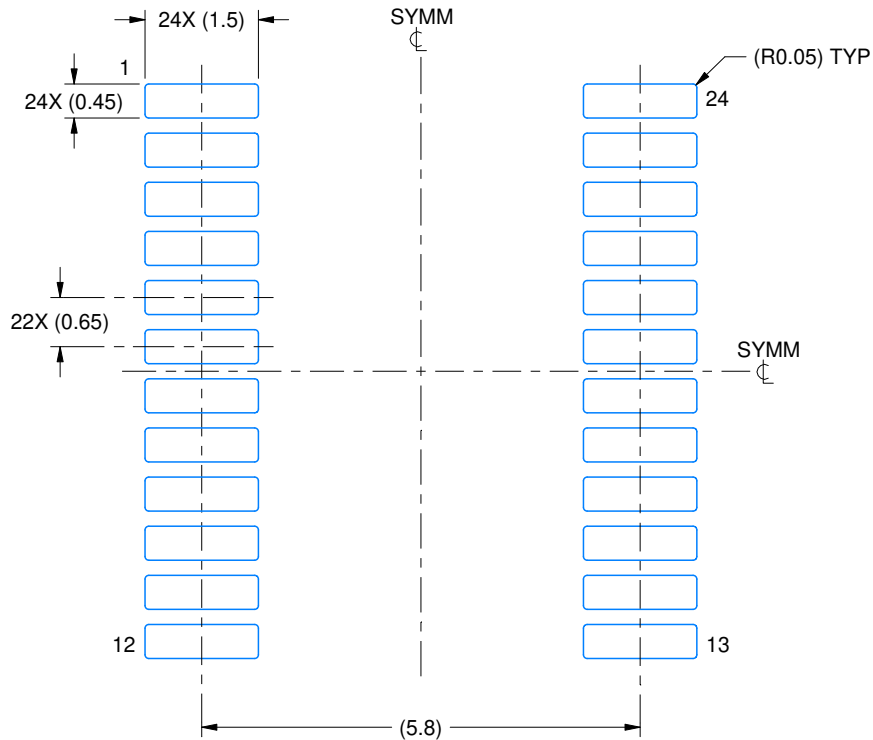
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

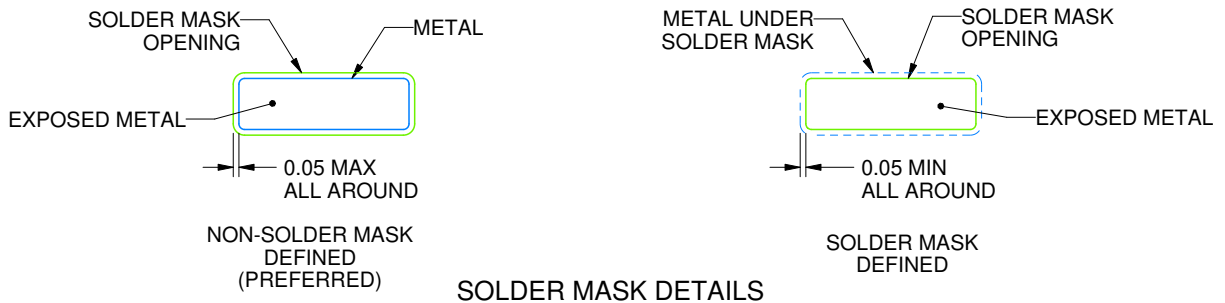
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

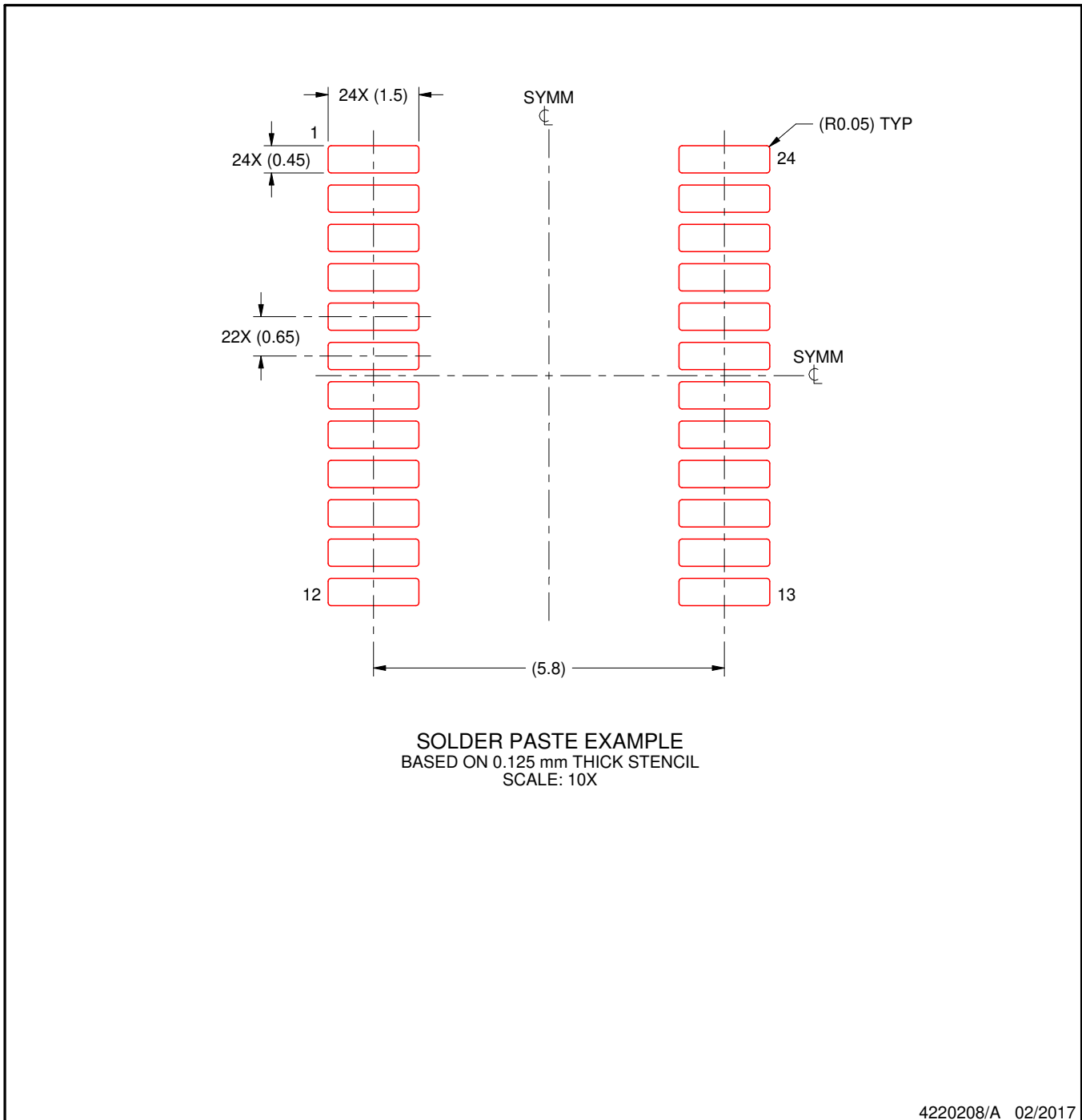
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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