

Easy Evaluation for the SP6125EK1 24V Input, 0 to 3A Output Non-Synchronous Buck **Converter**

- Precision $0.60V \pm 1\%$ High -Accuracy Reference.
- **Small form factor**
- current protection with auto-restart, on/off internal compensation **Feature Rich: Single supply operation, Over**function, Preset internal soft start, Type-II

SP6125, 3A Evaluation Board Manual

SP6125EB SCHEMATIC

* R(10k) is optional. It helps keep the output capacitor discharged under no-load condition.

USING THE EVALUATION BOARD

1) Powering Up the SP6125EB Circuit

Connect the SP6125 Evaluation Board to an external +24V power supply. Connect with short leads directly to the "VIN" and "GND" posts. Connect a Load between the "VOUT" and "GND" posts, again using short leads to minimize inductance and voltage drop.

2) Measuring Output Load Characteristics

It's best to GND reference scope and digital meters using the Star GND post near the output of the board. VOUT ripple can best be seen touching probe tip to the pad for COUT and scope GND collar touching Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP6125 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP6125 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin FB, which is set to an internal reference voltage of 0.60V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$
R2 = \frac{R1}{\left(\frac{Vout}{Vref} - 1\right)}
$$

Where R1 = 300k Ω . For Vout = 0.60V setting, simply remove R2 from the board.

Note that since the SP6125 Evaluation Board design was optimized for 24V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section.

Using the SHDN (ON/OFF function)

Feedback pin serves a dual role of ON/OFF control. The MOSFET driver is disabled when a voltage greater than 1V is applied at FB pin. Maximum voltage rating of this pin is 5.5V. The controlling signal should be applied through a small signal diode as shown on page 1. Under no-load condition an optional 10kOhm bleeding resistor across the output helps keep the output capacitor discharged.

POWER SUPPLY DATA

The SP6125EB is designed with an accurate 2% reference over line, load and temperature. Figure 1 data shows a typical SP6125 Evaluation Board efficiency plot, with efficiencies to 82% and output currents to 3A. SP6125 Load Regulation in Figure 2 shows little change in output voltage from no load to 3A load. Figures 3 and 4 show the transient response and Overcurrent. Figures 5 and 6 show a controlled start-up with no load and 3A load when power is applied where the input current rises smoothly as the soft-start ramp increases. Figures 7 and 8 show the output ripple under no load and 3A load.

Typical Performance Characteristics

Figure 5- Startup no load, ch1: Vin Figure 6- Start up 3A, ch1: Vin ch2: Vout, ch3: Iout ch2: Vout, ch3: Iout

Typical Performance Characteristics

LOOP COMPENSATION

The SP6125 includes Type-II internal compensation components for loop compensation. External compensation components are not required for systems with tantalum or aluminum electrolytic output capacitors with sufficiently high ESR. Use the condition below as a guideline to determine whether or not the internal compensation is sufficient for your design.

Type-II internal compensation is sufficient if the following condition is met:

DBPOLEESRZERO < *ff* ………………. (1)

where:

$$
f_{ESRZERO} = \frac{1}{2\pi R_{ESR} . C_{OUT}} \dots \dots \dots \tag{2}
$$

$$
f_{DBPOLE} = \frac{1}{2 \pi \sqrt{L \cdot C_{OUT}}} \dots \dots \dots \dots \tag{3}
$$

Creating a Type-III compensation Network

The above condition requires the ESR zero to be at a lower frequency than the doublepole from the LC filter. If this condition is not met, Type-III compensation should be used and can be accomplished by placing a series RC combination in parallel with R1 as shown below. The value of CZ can be calculated as follows and RZ selected from table 1.

$$
CZ = \frac{\sqrt{L \cdot C}}{1.3 \times R1} \dots \dots \dots \dots \dots \tag{4}
$$

f _{ESRZERO} /f _{DBPOLE}	RZ
1 X	50K
2Χ	40K
ЗX	30K
5Χ	10K
$>= 10X$	2K

Table1- Selection of RZ

Figure 9- RZ and CZ in conjunction with internal compensation components form a Type-III compensation

Loop Compensation for the SP6125EB

 $L = 8.2$ uH, $C = 2x22$ uF/5mOhm ceramic capacitor

From equation (2) $f_{ESRZERO} = 1.45 MHz$. From equation (3) $f_{DBPOLE} = 8.4$ kHz. Since the condition specified in (1) is not met, Type-III compensation has to be used by adding external components RZ and CZ. Using equation (4) CZ is calculated 48.7pF (use $47pF$). Following the guideline given in table 1, a $2k\Omega$ RZ was used.

PCB LAYOUT DRAWINGS

Figure 10. SP6125EB Component Placement

Figure 11. SP6125EB PCB Layout Top Side

Figure 12. SP6125EB PCB Layout Bottom Side

Table 2- SP6125EB List of Materials

Table 3- SP6125EB Suggested Components and Vendor Lists

ORDERING INFORMATION

