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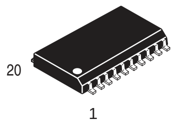
Low Skew CMOS PLL 68060 Clock Driver

MC88LV926

LOW SKEW CMOS PLL
68060 CLOCK DRIVER



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D

The MC88LV926 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The RST_IN/RST_OUT(LOCK) pins provide a processor reset function designed specifically for the MC68/EC/LC030/040/060 microprocessor family. To support the 68060 processor, the 88LV926 operates from a 3.3V as well as a 5.0V supply.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88LV926 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.

- 2X_Q Output Meets All Requirements of the 50 and 66MHz 68060 Microprocessor PCLK Input Specifications
- Low Voltage 3.3V V_{CC}
- Three Outputs (Q0–Q2) With Output–Output Skew <500ps
- CLKEN Output for Half Speed Bus Applications
- The Phase Variation From Part–to–Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the T_{PD} Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5MHZ to 2X_Q F_{Max}/4
- All Outputs Have ±36mA Drive (Equal High and Low) CMOS Levels
- Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible with V_{CC} = 3.3V
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing

Three 'Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output is ideal for 68060 systems which require a 2X processor clock input, and it meets the tight duty cycle spec of the 50 and 66MHz 68060. The QCLKEN output is designed to drive the CLKEN input of the 68060 when the bus logic runs at half of the microprocessor clock rate. The QCLKEN output is skewed relative to the 2X_Q output to ensure that CLKEN setup and hold times of the 68060 are satisfied. A Q/2 frequency is fed back internally, providing a fixed 2X multiplication from the 'Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed. The Q3 output provides an inverted clock output to allow flexibility in the clock tree design.

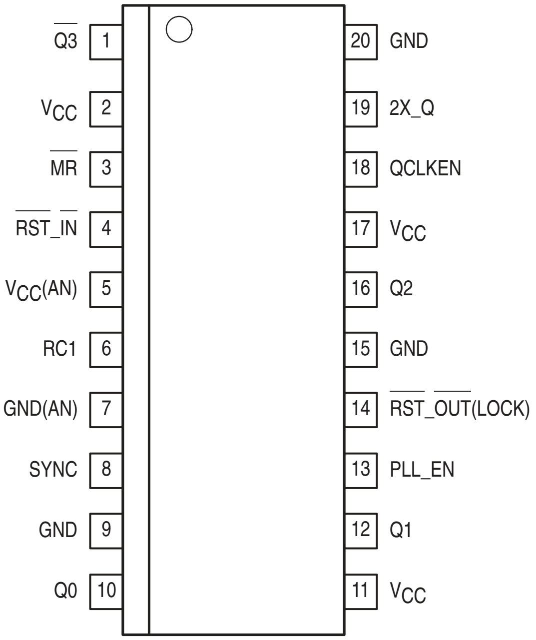
In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV926 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

The RST_OUT(LOCK) pin doubles as a phase–lock indicator. When the RST_IN pin is held high, the open drain RST_OUT pin will be pulled actively low until phase–lock is achieved. When phase–lock occurs, the RST_OUT(LOCK) is released and a pull–up resistor will pull the signal high. To give a processor reset signal, the RST_IN pin is toggled low, and the RST_OUT(LOCK) pin will stay low for 1024 cycles of the 'Q' output frequency after the RST_IN pin is brought back high.

Description of the RST_IN/RST_OUT(LOCK) Functionality

The RST_IN and RST_OUT(LOCK) pins provide a 68030/040/060 processor reset function, with the RST_OUT pin also acting as a lock indicator. If the RST_IN pin is held high during system power–up, the RST_OUT pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 'Q' output cycles after phase–lock is achieved the RST_OUT(LOCK) pin will go into a high impedance state, allowing it to be pulled high by an external pull–up resistor (see the AC/DC specs for the characteristics of the RST_OUT(LOCK) pin). If the RST_IN pin is held low during power–up, the RST_OUT(LOCK) pin will remain low.

Pinout: 20–Lead Wide SOIC Package (Top View)



Description of the RST_IN/RST_OUT(LOCK) Functionality (continued)

After the system start–up is complete and the 88LV926 is phase–locked to the SYNC input signal (RST_OUT high), the processor reset functionality can be utilized. When the RST_IN pin is toggled low (min. pulse width=10nS), RST_OUT(LOCK) will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the RST_OUT(LOCK) is actively pulled low, all the 88LV926 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040/060 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle RST_OUT(LOCK) goes back to the high impedance state to be pulled high by the resistor.

Power Supply Ramp Rate Restriction for Correct 030/040 Processor Reset Operation During System Start–up

Because the RST_OUT(LOCK) pin is an indicator of phase–lock to the reference source, some constraints must be placed on the power supply ramp rate to make sure the RST_OUT(LOCK) signal holds the processor in reset during system start–up (power–up). With the recommended loop filter values (see Figure 6.) the lock time is approximately 10ms. The phase–lock loop will begin attempting to lock to a reference source (if it is present) when VCC reaches 2V. If the V_{CC} ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing RST_OUT(LOCK) to go high before the 88LV926 and '030/040 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the RST_IN pin to be held high during power–up, the V_{CC} ramp rate must be less than 10mS for proper 68030/040/060 reset operation.

This ramp rate restriction can be ignored if the RST_IN pin can be held low during system start–up (which holds RST_OUT low). The RST_OUT(LOCK) pin will then be pulled back high 1024 cycles after the RST_IN pin goes high.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5*	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40*	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output* 90mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output* 225mW/Device	mW	V_{CC} = 5.0V T = 25°C

* Value at V_{CC} = 3.3V TBD.

MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ±0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1500	V

DC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V)[4]

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage[4]	3.0 3.3	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.2 2.5	V	V_{IN} = V_{IH} or V_{IL} I_{OH} –24mA –24mA
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.55 0.55	V	V_{IN} = V_{IH} or V_{IL} I_{OH} +24mA[1] +24mA
I_{IN}	Maximum Input Leakage Current	3.3	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	3.3	2.0 [2]	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	3.3	50	mA	V_{OLD} = 1.25V Max
I_{OHD}		3.3	–50	mA	V_{OHD} = 2.35 Min
I_{CC}	Maximum Quiescent Supply Current	3.3	750	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the $\overline{\text{RST}}$_$\overline{\text{OUT}}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.
4. The MC88LV926 can also be operated from a 5.0V supply. V_{OH} output levels will vary 1:1 with V_{CC}, input levels and current specs will be unchanged, except V_{IH}; when V_{CC} > 4.0 volts, V_{IH} minimum level is 2.7 volts.

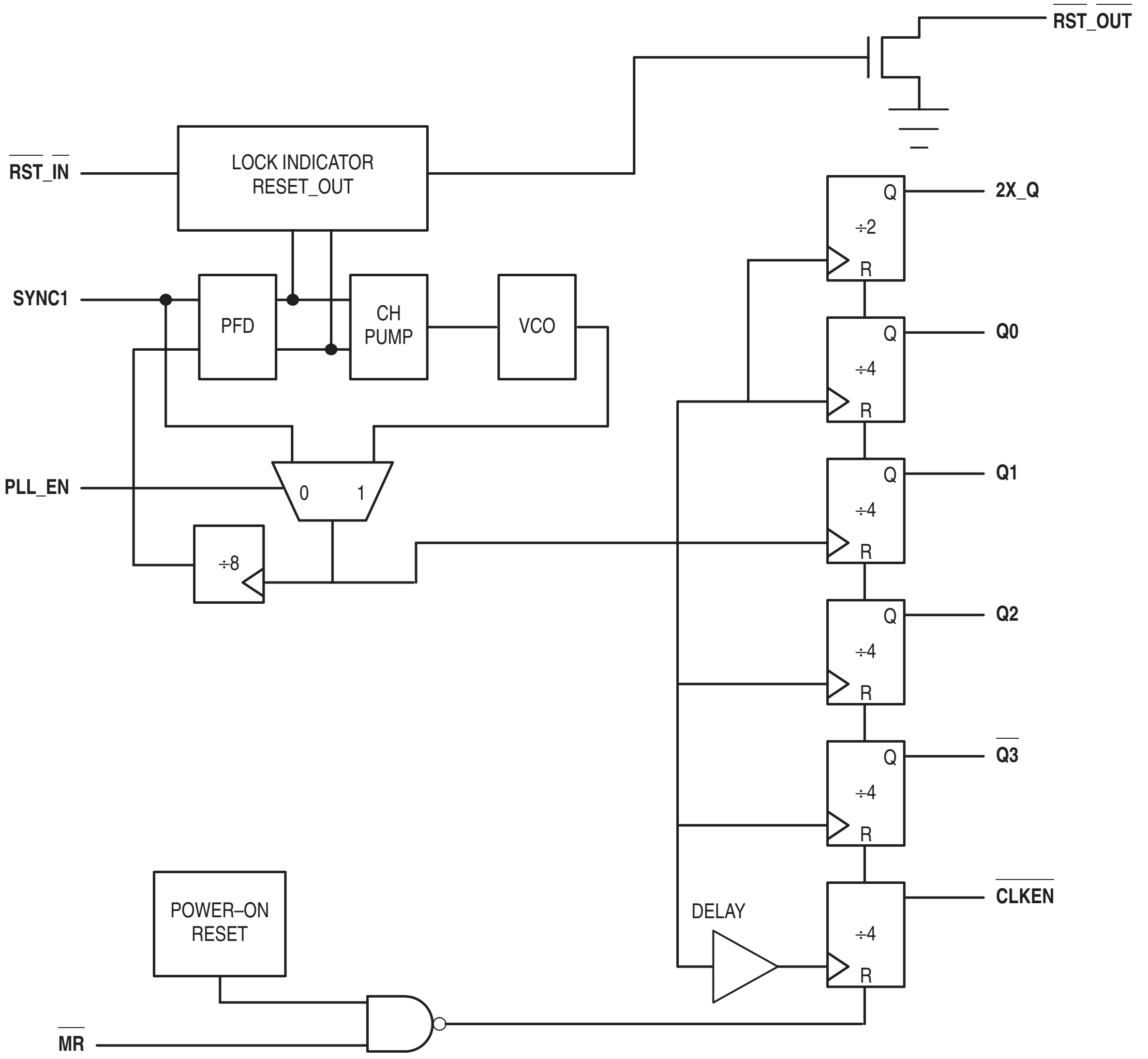


Figure 1. MC88LV926 Logic Block Diagram

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input[1]	$\frac{1}{f_{2X\_Q}/4}$	200[1]	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

1. When V_{CC} > 4.0 volts, Maximum SYNC Input Period is 125ns.

FREQUENCY SPECIFICATIONS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V or 5.0V ±5%)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	66	MHz
Fmax (‘Q’)	Maximum Operating Frequency, Q0–Q3 Outputs	33	MHz

Maximum Operating Frequency is guaranteed with the 88LV926 in a phase–locked condition.

AC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V or 5.0V ±5%)

Symbol	Parameter	Mimimum	Maximum	Unit	Condition
$t_{RISE/FALL}$ All Outputs	Rise/Fall Time, into 50Ω Load	0.3	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time into a 50Ω Load	0.5	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, Q3)	Output Pulse Width Q0, Q1, Q2, Q3 at 1.65V	$0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
$t_{pulse\ width(b)}$[1] (2X_Q Output)	Output Pulse Width 2X_Q at 1.65V	$0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
t_{SKEWr}[2] (Rising)	Output–to–Output Skew Between Outputs Q0–Q2 (Rising Edge Only)	—	500	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
t_{SKEWf}[2] (Falling)	Output–to–Output Skew Between Outputs Q0–Q2 (Falling Edge Only)	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
$t_{SKEWall}$[2]	Output–to–Output Skew 2X_Q, Q0–Q2, Q3	—	750	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
t_{SKEW} QCLKEN[1,2]	Output–to–Output Skew QCLKEN to 2X_Q 2X_Q = 50MHz 2X_Q = 66MHz	 9.7[6] 7.0[6]	—	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
t_{LOCK}[3]	Phase–Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
t_{PHL} $\overline{\text{MR}}$ – Q[1]	Propagation Delay, MR to Any Output (High–Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{REC}, $\overline{\text{MR}}$ to SYNC[5, 1]	Reset Recovery Time rising $\overline{\text{MR}}$ edge to falling SYNC edge	9	—	ns	
t_W, $\overline{\text{MR}}$ LOW[5, 1]	Minimum Pulse Width, $\overline{\text{MR}}$ input Low	5	—	ns	
t_W, $\overline{\text{RST}}$_$\overline{\text{IN}}$ LOW[1]	Minimum Pulse Width, $\overline{\text{RST}}$_$\overline{\text{IN}}$ Low	10	—	ns	When in Phase–Lock
t_{PZL}[1]	Output Enable Time RST_IN Low to RST_OUT Low	1.5	16.5	ns	See Application Note 5
t_{PLZ}[1]	Output Enable Time RST_IN High to RST_OUT High Z	1016 ‘Q’ Cycles (508 Q/2 Cycles)	1024 ‘Q’ Cycles (512 Q/2 Cycles)	ns	See Application Note 5

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered–on: t_{CLOCK} Max is with C1 = 0.1µF; t_{LOCK} Min is with C1 = 0.01µF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Specification is valid only when the PLL_EN pin is low.
6. Guaranteed that QCLKEN will meet the setup and hold time requirement of the 68060.

Application Notes

1. Several specifications can only be measured when the MC88LV926 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88LV926 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. Response Surface Modeling (RSM) techniques were used to relate IC performance to the CMOS transistor properties over operation voltage and temperature. IC performance to each specification and fab variation were used in conjunction with Yield Surface Modeling™ (YSM™) methodology to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. A 470KΩ resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 2., is required to ensure no jitter is present on the MC88LV926 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 2. for a graphical description.
3. Two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output, see AC Specifications) guarantee that the MC88LV926 meets the 33MHz and 66MHz 68060 P–Clock input specification.

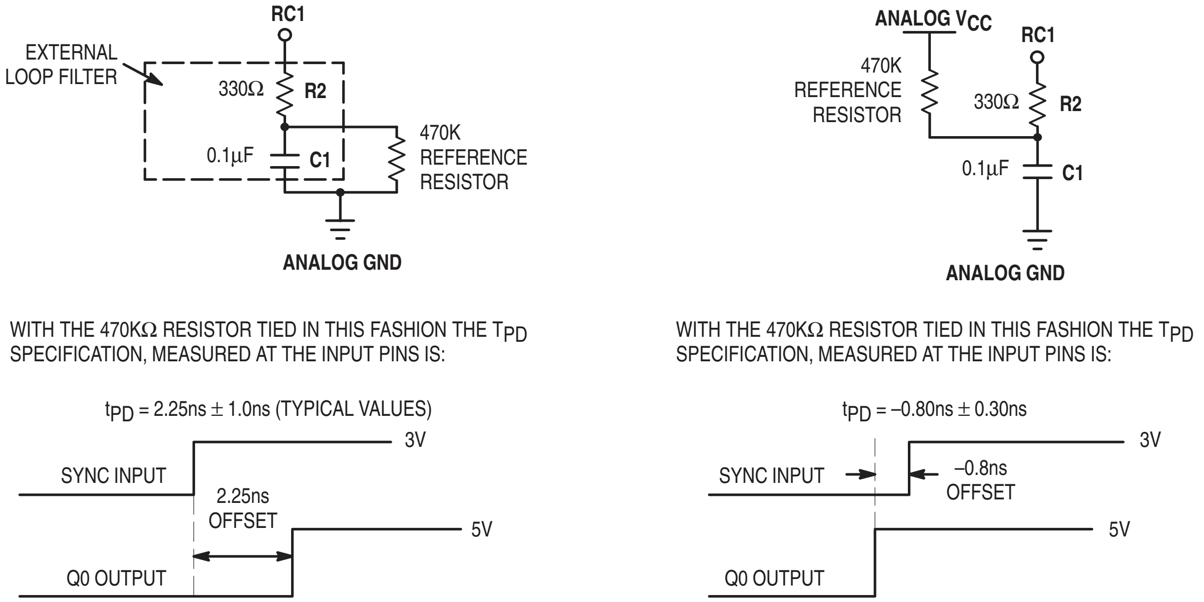


Figure 2. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 470KΩ Resistor Is Tied to V_{CC} or Ground

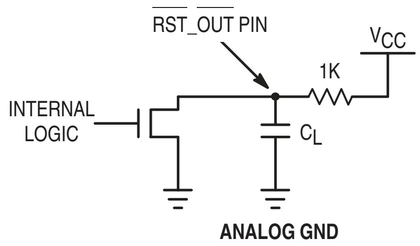


Figure 3. RST_OUT Test Circuit

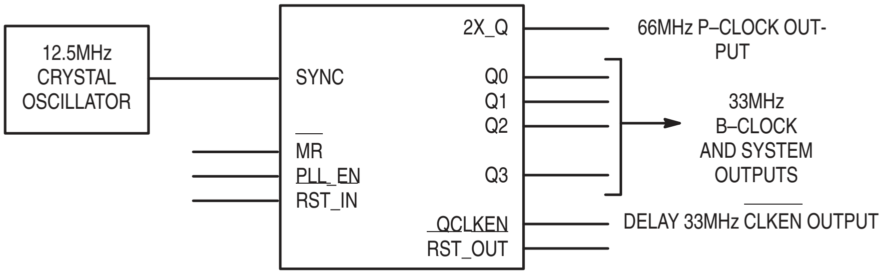


Figure 4. Logical Representation of the MC88LV926 With Input/Output Frequency Relationships

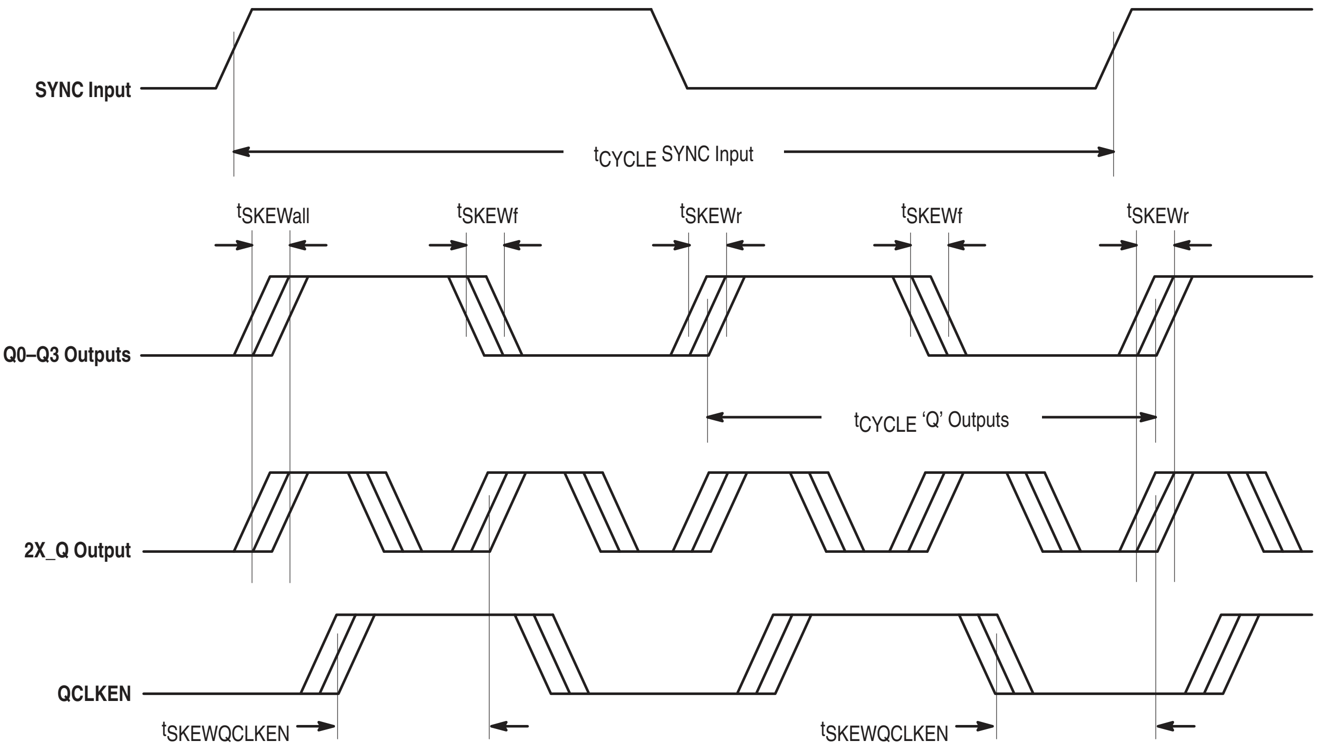


Figure 5. Output/Input Switching Waveforms and Timing Relationships

Timing Notes

1. The MC88LV926 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 3.0V to 3.3V. If the ΔT and ΔV_{CC} is a given system are less than the specification limits, the t_{PD} spec window will be reduced. The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

5. The $\overline{\text{RST}}$_$\overline{\text{OUT}}$ pin is an open drain N–Channel output. Therefore an external pull–up resistor must be provide to pull up the RST_OUT pin when it goes into the high impedance state (after the MC88LV926 is phase–locked to the reference input with RST_IN held high or 1024 ‘Q’ cycles after the RST_IN pin goes high when the part is locked). In the t_{PLZ} and t_{PZL} specifications, a 1KΩ resistor is used as a pull–up as shown in Figure 3.

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 6. shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

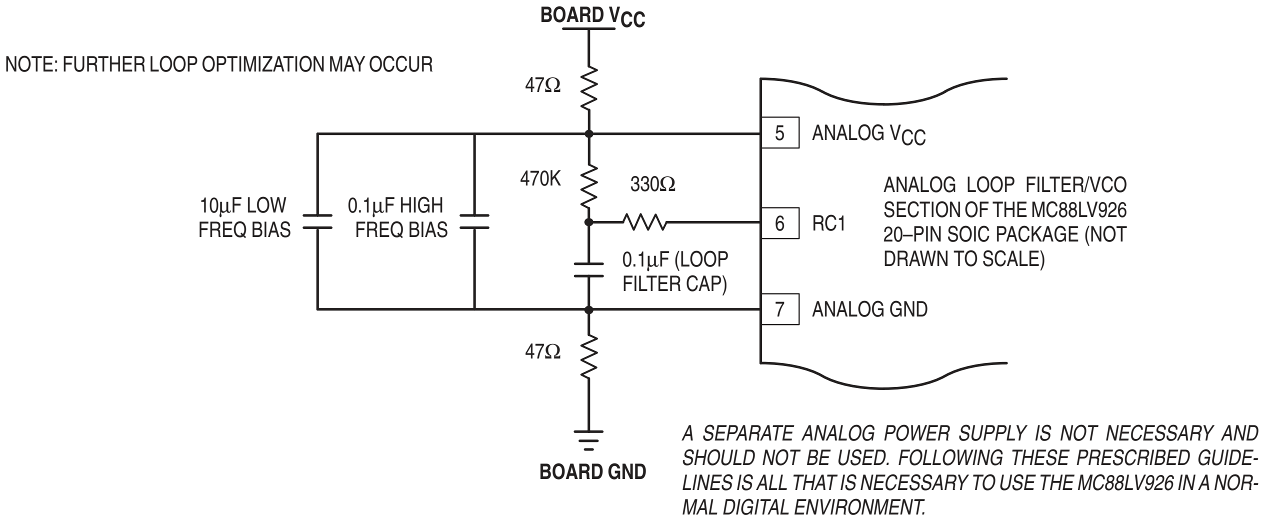
1b. The 47Ω resistors, the 10µF low frequency bypass capacitor, and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will make the 88LV926 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88LV926 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25µF bypass capacitor is used (instead of 10µF) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV926’s digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 6. is to give the 88LV926 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 470K reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 470K resistor provides the correct amount of current injection into the charge pump (2–3µA). If the VCO is running below 40MHz, a 1MΩ reference resistor should be used (instead of 470K).

2. In addition to the bypass capacitors used in the analog filter of Figure 6., there should be a 0.1µF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV926 outputs, in addition to reducing potential for noise in the ‘analog’ section of the chip. These bypass capacitors should also be tied as close to the 88LV926 package as possible.



A SEPARATE ANALOG POWER SUPPLY IS NOT NECESSARY AND SHOULD NOT BE USED. FOLLOWING THESE PRESCRIBED GUIDELINES IS ALL THAT IS NECESSARY TO USE THE MC88LV926 IN A NORMAL DIGITAL ENVIRONMENT.

Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV926

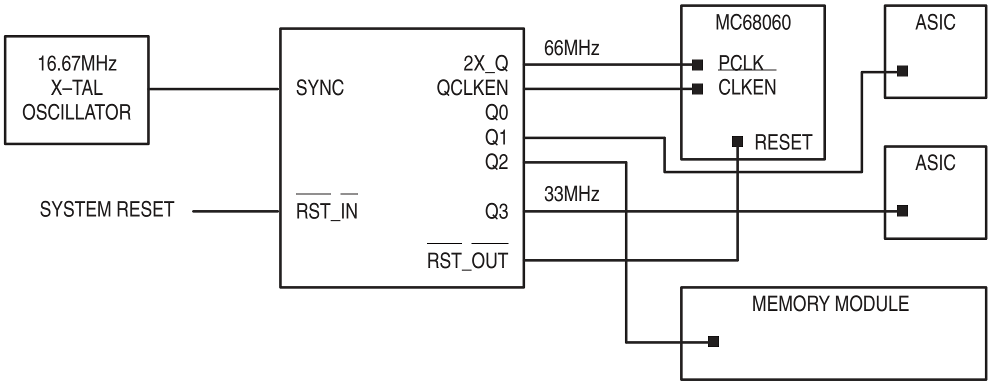


Figure 7. Typical MC88LV926/MC68060 System Configuration

OUTLINE DIMENSIONS

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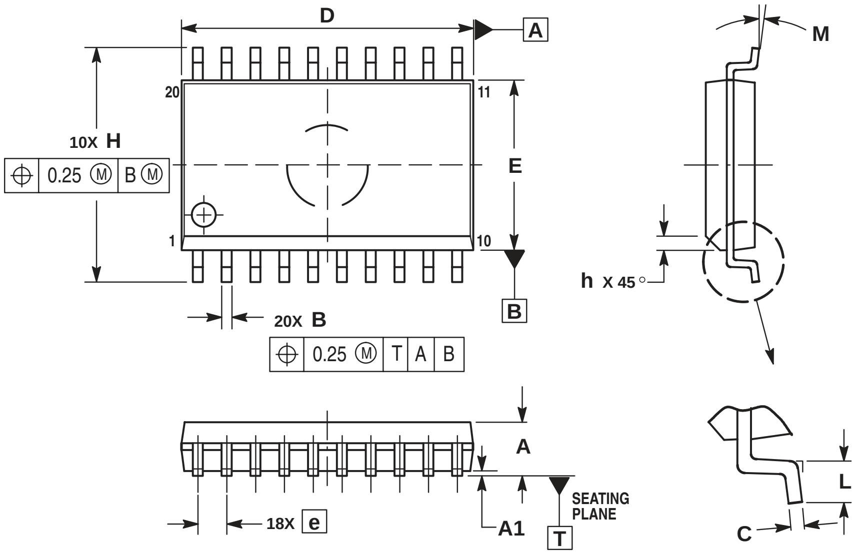
SOIC PACKAGE
CASE 751D-06
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.40	1.00
θ	0°	7°

NOTES

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