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## 74AC541, 74ACT541 Octal Buffer/Line Driver with 3-STATE Outputs

### Features

- I<sub>CC</sub> and I<sub>OZ</sub> reduced by 50%
- 3-STATE outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24mA
- 74AC541 is a non-inverting option of the 74AC540
- 74ACT541 has TTL-compatible inputs

## **General Description**

The 74AC541 and 74ACT541 are octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/ receivers.

These devices are similar in function to the 74AC244 and 74ACTC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

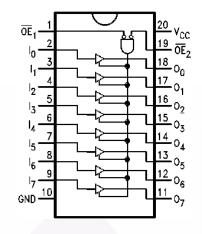
## **Ordering Information**

Order Number	Package Number	Package Description
74AC541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC541PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

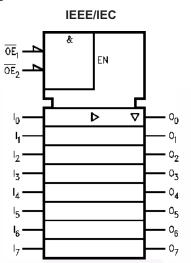
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

## **Connection Diagram**



Logic Symbol



## **Truth Table**

	Inputs						
OE <sub>1</sub>	$\overline{OE}_2$	I	Outputs				
L	L	Н	Н				
Н	Х	Х	Z				
Х	Н	Х	Z				
L	L	L	L				

H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

Z = High Impedance

## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V <sub>CC</sub>	Supply Voltage	-0.5V to +7.0V
I <sub>IK</sub>	DC Input Diode Current	
	$V_{I} = -0.5V$	–20mA
	$V_{I} = V_{CC} + 0.5$	+20mA
VI	DC Input Voltage	-0.5V to V <sub>CC</sub> + 0.5V
I <sub>OK</sub>	DC Output Diode Current	
	$V_{O} = -0.5V$	–20mA
	$V_{O} = V_{CC} + 0.5V$	+20mA
Vo	DC Output Voltage	-0.5V to V <sub>CC</sub> + 0.5V
Io	DC Output Source or Sink Current	±50mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current per Output Pin	±50mA
T <sub>STG</sub>	Storage Temperature	-65°C to +150°C
TJ	Junction Temperature	140°C

## **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating			
V <sub>CC</sub>	Supply Voltage				
	AC	2.0V to 6.0V			
	ACT	4.5V to 5.5V			
VI	Input Voltage	0V to V <sub>CC</sub>			
Vo	Output Voltage	0V to V <sub>CC</sub>			
T <sub>A</sub>	Operating Temperature	_40°C to +85°C			
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices:	125mV/ns			
	$\rm V_{IN}$ from 30% to 70% of $\rm V_{CC}, \rm V_{CC}$ @ 3.3V, 4.5V, 5.5V				
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices:				
	V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> @ 4.5V, 5.5V				

				<b>T</b> <sub>A</sub> = -	⊦25°C	$T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol	Parameter	V <sub>CC</sub> (V) Condition		Typ. Gu		uaranteed Limits	Units
V <sub>IH</sub>	Minimum HIGH Level	3.0	$V_{OUT} = 0.1V \text{ or}$	1.5	2.1	2.1	V
	Input Voltage	4.5	V <sub>CC</sub> – 0.1V	2.25	3.15	3.15	1
		5.5		2.75	3.85	3.85	1
V <sub>IL</sub>	Maximum LOW Level	3.0	$V_{OUT} = 0.1V$ or	1.5	0.9	0.9	V
	Input Voltage	4.5	0 1\/		1.35	1.35	
			-	2.75	1.65	1.65	
V <sub>OH</sub>	Minimum HIGH Level	3.0	Ι <sub>ΟUT</sub> = –50μΑ	2.99	2.9	2.9	V
	Output Voltage	4.5	-	4.49	4.4	4.4	
		5.5	-	5.49	5.4	5.4	
		3.0	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -12\text{mA}$		2.56	2.46	-
		4.5	$V_{IN} = V_{IL}$ or $V_{IH}$ , $I_{OH} = -24 \text{mA}$		3.86	3.76	
	5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24 \text{mA}^{(1)}$		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level	3.0	Ι <sub>ΟUT</sub> = 50μΑ	0.002	0.1	0.1	V
	Output Voltage	4.5	-	0.001	0.1	0.1	
		5.5	-	0.001	0.1	0.1	
			$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 12 \text{mA}$		0.36	0.44	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}^{(1)}$		0.36	0.44	
I <sub>IN</sub> <sup>(2)</sup>	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$ , GND		±0.1	±1.0	μΑ
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5			±0.25	±2.5	μA
I <sub>OLD</sub>	Minimum Dynamic	5.5	V <sub>OLD</sub> = 1.65V Max.			75	mA
I <sub>OHD</sub>	Output Current <sup>(3)</sup>	5.5	V <sub>OHD</sub> = 3.85V Min.			-75	mA
I <sub>CC</sub> <sup>(2)</sup>	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

## **DC Electrical Characteristics for AC**

#### Notes:

1. All outputs loaded; thresholds on input associated with output under test.

2.  $I_{\rm IN}$  and  $I_{\rm CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\rm CC}.$ 

3. Maximum test duration 2.0ms, one output loaded at a time.

				$T_A = -$	+ <b>25°C</b>	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Тур.	o. Guaranteed Limits		Units
V <sub>IH</sub>	Minimum HIGH Level	4.5	$V_{OUT} = 0.1V$ or	1.5	2.0	2.0	V
	Input Voltage	5.5	V <sub>CC</sub> – 0.1V	1.5	2.0	2.0	
V <sub>IL</sub>	Maximum LOW	4.5	$V_{OUT} = 0.1V$ or	1.5	0.8	0.8	V
	Level Input Voltage 5.5 V <sub>CC</sub>		V <sub>CC</sub> – 0.1V	1.5	0.8	0.8	
V <sub>OH</sub>	Minimum HIGH Level	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4	V
	Output Voltage	5.5	-	5.49	5.4	5.4	
	4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24 \text{mA}$		3.86	3.76		
	5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24 \text{mA}^{(4)}$		4.86	4.76		
V <sub>OL</sub>	Maximum LOW	4.5	Ι <sub>ΟUT</sub> = 50μΑ	0.001	0.1	0.1	V
	Level Output Voltage	5.5	-	0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24 \text{mA}^{(4)}$		0.36	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	$V_I = V_{CC}, \text{ GND}$		±0.1	±1.0	μA
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5	$V_{I} = V_{IL}, V_{IH};$ $V_{O} = V_{CC}, \text{ GND}$		±0.25	±2.5	μA
I <sub>сст</sub>	Maximum I <sub>CC</sub> /Input	5.5	$V_{I} = V_{CC} - 2.1V$	0.6		1.5	mA
I <sub>OLD</sub>	Minimum Dynamic	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I <sub>OHD</sub>	Output Current <sup>(5)</sup>	5.5	V <sub>OHD</sub> = 3.85V Min.			-75	mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

#### Notes:

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0ms, one output loaded at a time.

Note:

		C	<sub>A</sub> = +25° C <sub>L</sub> = 50p	C, F	$\begin{vmatrix} T_{A} = -40^{\circ}C \\ C_{L} = \end{vmatrix}$	50pF	
Parameter	V <sub>CC</sub> (V) <sup>(7)</sup>	Min.	Тур.	Max.	Min	Max	Units
Propagation Delay,	5.0	2.0	4.5	7.0	2.0	7.5	ns
Data to Output		2.0	5.5	7.0	2.0	7.5	
Output Enable Time	5.0	2.0	5.0	9.0	2.0	9.5	ns
		2.0	6.5	9.0	2.0	9.5	
Output Disable Time	5.0	1.5	5.5	7.5	1.5	8.0	ns
		1.5	5.5	7.5	1.5	8.0	
	Propagation Delay, Data to Output Output Enable Time	Propagation Delay, Data to Output5.0Output Enable Time5.0	ParameterV <sub>CC</sub> (V) <sup>(7)</sup> Min.Propagation Delay, Data to Output5.0 2.02.0Output Enable Time5.0 2.02.0Output Disable Time5.01.5	Parameter V <sub>CC</sub> (V) <sup>(7)</sup> Min. Typ.   Propagation Delay, Data to Output 5.0 2.0 4.5   Output Enable Time 5.0 2.0 5.0   Output Disable Time 5.0 2.0 6.5   Output Disable Time 5.0 1.5 5.5	Parameter V <sub>CC</sub> (V) <sup>(7)</sup> Min. Typ. Max.   Propagation Delay, Data to Output 5.0 2.0 4.5 7.0   Output Enable Time 5.0 2.0 5.5 7.0   Output Disable Time 5.0 2.0 6.5 9.0   Output Disable Time 5.0 1.5 5.5 7.5	Parameter V <sub>CC</sub> (V) <sup>(7)</sup> Min. Typ. Max. Min   Propagation Delay, Data to Output 5.0 2.0 4.5 7.0 2.0   Output Enable Time 5.0 2.0 5.5 7.0 2.0   Output Disable Time 5.0 2.0 5.5 9.0 2.0   Output Disable Time 5.0 1.5 5.5 7.5 1.5	Parameter V <sub>CC</sub> (V) <sup>(7)</sup> Min. Typ. Max. Min Max.   Propagation Delay, Data to Output 5.0 2.0 4.5 7.0 2.0 7.5   Output Enable Time 5.0 2.0 5.0 9.0 2.0 9.5   Output Disable Time 5.0 1.5 5.5 7.5 9.0 9.5

Note:

7. Voltage range 5.0 is  $5.0V \pm 0.5V$ .

## Capacitance

Symbol	Parameter	Conditions	Тур.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN	4.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance for AC	$V_{CC} = 5.0V$	30.0	pF
	Power Dissipation Capacitance for ACT		70.0	

6. Voltage range 3.3 is 3.3V  $\pm$  0.3V. Voltage range 5.0 is 5.0V  $\pm$  0.5V.

**AC Electrical Characteristics for ACT** 

			$\begin{array}{l} T_{A}=+25^{\circ}C,\\ C_{L}=50pF \end{array}$		$ \begin{array}{c} T_A = -40^\circ C \text{ to } +85^\circ C,\\ C_L = 50 p F \end{array} $			
Symbol	Parameter	$V_{CC} (V)^{(6)}$	Min.	Тур.	Max.	Min.	Max.	Units
t <sub>PLH</sub>	Propagation Delay,	3.3	2.0	5.5	8.0	1.5	9.0	ns
	Data to Output	5.0	1.5	4.0	6.0	1.0	6.5	
t <sub>PHL</sub>	Propagation Delay,	3.3	2.0	5.5	8.0	1.5	8.5	ns
	Data to Output	5.0	1.5	4.0	6.0	1.0	6.5	
t <sub>PZH</sub>	Output Enable Time	3.3	3.0	8.0	11.5	3.0	12.5	ns
		5.0	2.0	6.0	8.5	1.5	9.5	
t <sub>PZL</sub>	Output Enable Time	3.3	2.5	7.0	10.0	2.5	11.5	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t <sub>PHZ</sub>	Output Disable Time	3.3	3.5	9.0	12.5	2.5	14.0	ns
		5.0	2.0	7.0	9.5	1.0	10.5	
t <sub>PLZ</sub>	Output Disable Time	3.3	2.5	6.5	9.5	2.0	10.5	ns
		5.0	2.0	5.5	7.5	1.0	8.5	

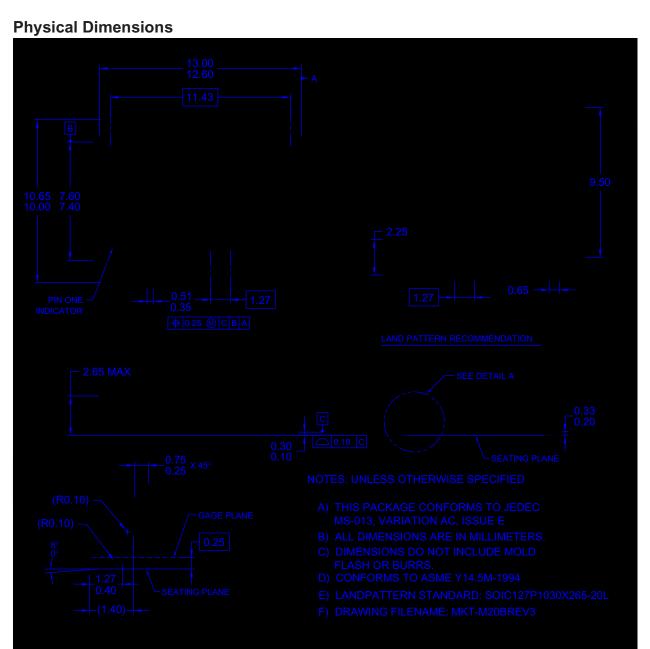


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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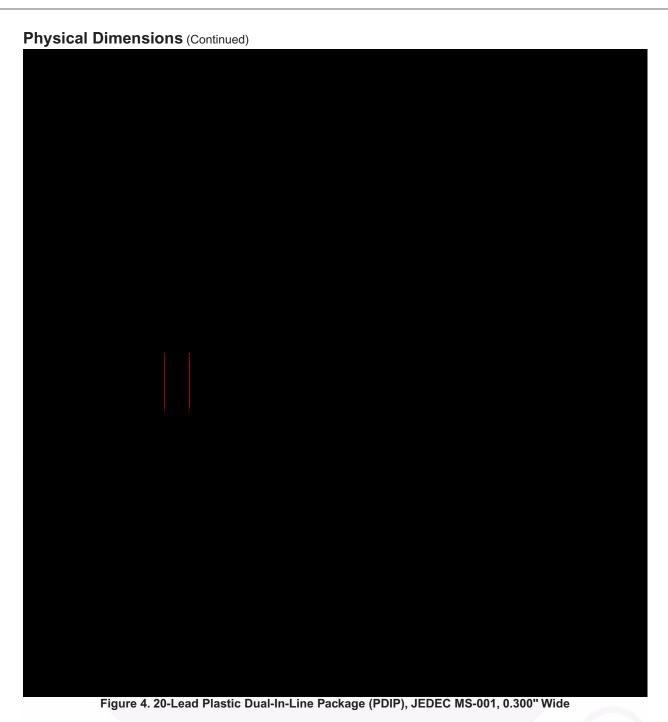
Physical Dimensions (Continued)

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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